

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT652

**Octal bus transceiver/register;
3-state**

Product specification
File under Integrated Circuits, IC06

September 1993

Octal bus transceiver/register; 3-state

74HC/HCT652

FEATURES

- Multiplexed real-time and stored data
- Independent register for A and B buses
- Independent enables for A and B buses
- 3-state
- Output capability: Bus driver
- Low power consumption by CMOS technology
- I_{CC} category: MSI.

APPLICATIONS

- Bus interfaces.

DESCRIPTION

The 74HC/HCT652 are high-speed SI-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in

compliance with Jedec standard no. 7A.

The 74HC/HCT652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and central circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropriate clock pins (CP_{AB} or CP_{BA}) regardless of the select pins (S_{AB} and S_{BA}) or output enable (OE_{AB} and OE_{BA}) control pins. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the output enable pins this operating mode permits. The output enable pins OE_{AB} and OE_{BA} determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is

possible and when OE_{BA} is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA}. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high-impedance, each set of the bus lines will remain at its last state. This type differs from the HC/HCT646 in one extra bus-management function. This is the possibility to transfer stored "A" data to the "B" bus and transfer stored "B" data to the "A" bus at the same time. The examples at the application information demonstrate all bus management functions. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f = 6 ns; V_{CC} = 4.5 V; C_L = 50 pF.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|------------------------------------|--|--|---------|-----|------|
| | | | HC | HCT | |
| t _{PLH} /t _{PZL} | propagation delay A _n /B _n to B _n /A _n | C _L = 15 pF; V _{CC} = 5 V | 13 | 13 | ns |
| | propagation delay CP _{AB} /CP _{BA} to B _n /A _n | | 18 | 20 | ns |
| | propagation delay S _{AB} /S _{BA} to B _n /A _n | | 20 | 23 | ns |
| t _{PHZ} /t _{PZL} | 3-state output enable time OE _{AB} /OE _{BA} to B _n /A _n | | 14 | 15 | ns |
| t _{PHZ} /t _{PLZ} | 3-state output disable time OE _{AB} /OE _{BA} to B _n /A _n | | 12 | 13 | ns |
| f _{max} | maximum clock frequency | | 92 | 92 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per channel | notes 1 and 2 | 26 | 28 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; C_L = output load capacitance in pF;

f_o = output frequency in MHz; V_{CC} = supply voltage in V;

∑ (C_L × V_{CC}² × f_o) = sum of the outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

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ORDERING AND PACKAGE INFORMATION

| TYPE NUMBER | PACKAGE | | | |
|--------------|---------|--------------|----------|---------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| 74HC/HCT652N | 24 | DIL | plastic | SOT101L |
| 74HC/HCT652D | 24 | SO | plastic | SOT137A |

PINNING

| SYMBOL | PIN | DESCRIPTION |
|---------------------------------|--------|----------------------------|
| CP _{AB} | 1 | A to B clock input |
| S _{AB} | 2 | select A to B source input |
| OE _{AB} | 3 | output enable A to B input |
| A ₀ ..A ₇ | 4..11 | A data inputs/outputs |
| GND | 12 | ground (0 V) |
| B ₇ ..B ₀ | 13..20 | B data inputs/outputs |
| OE _{BA} | 21 | output enable B to A input |
| S _{BA} | 22 | select B to A source input |
| CP _{BA} | 23 | B to A clock input |
| V _{CC} | 24 | positive supply voltage |

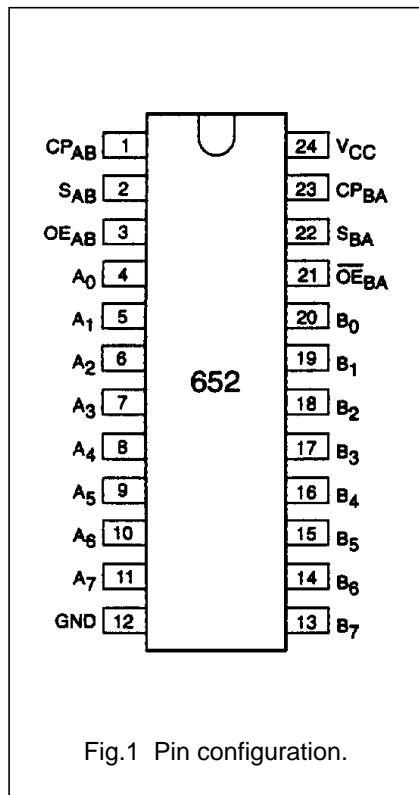


Fig.1 Pin configuration.

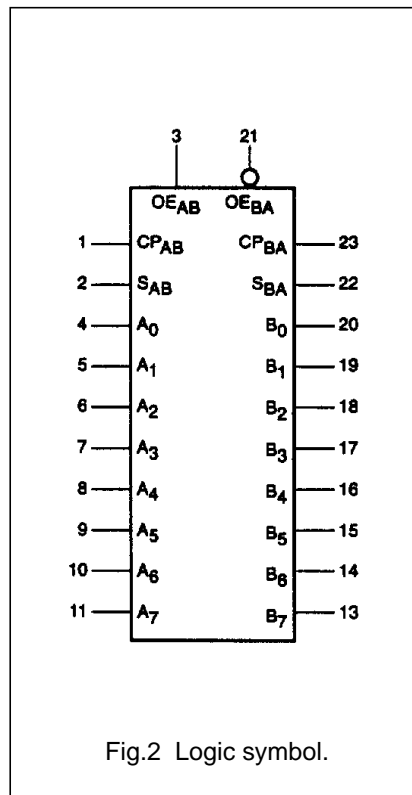


Fig.2 Logic symbol.

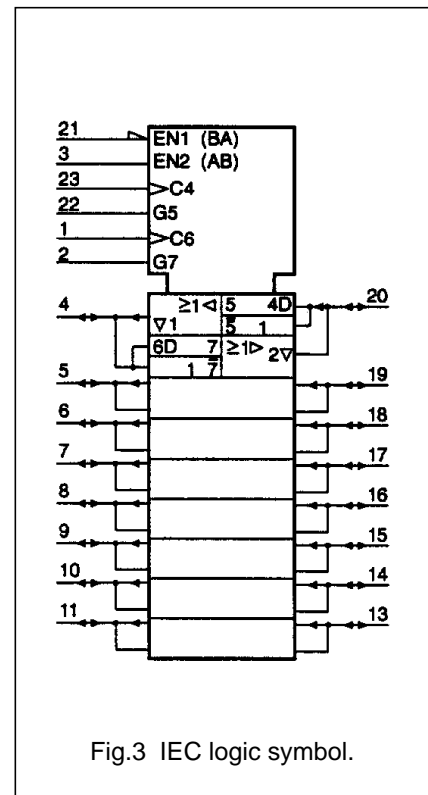


Fig.3 IEC logic symbol.

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FUNCTION TABLE

| INPUTS ⁽¹⁾ | | | | | | DATA I/O ⁽²⁾ | | OPERATION OR FUNCTION |
|-----------------------|------------------|------------------|------------------|-----------------|-----------------|------------------------------------|------------------------------------|--|
| OE _{AB} | OE _{BA} | CP _{AB} | CP _{BA} | S _{AB} | S _{BA} | A ₁ THRU A ₈ | B ₁ THRU B ₈ | HC/HCT652 |
| L | H | H or L | H or L | X | X | Input | Input | Isolation Store A and B data |
| L | H | ↑ | ↑ | X | X | Input | Input | |
| X | H | ↑ | H or L | X | X | Input | Not specified | Store A, Hold B |
| H | H | ↑ | ↑ | L | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Not specified | Input | Hold A, Store B |
| L | L | ↑ | ↑ | X | L | Ouput | Input | Store B in both registers |
| L | L | X | X | X | L | Ouput | Input | Real Time B Data to A Bus |
| L | L | X | H or L | X | H | Ouput | Input | Stored B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real Time A Data to B Bus |
| H | H | H or L | X | H | X | Input | Output | Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

Notes

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH transition
- The data output functions may be enabled or disabled by various signals at OE_{AB} and OE_{BA} inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

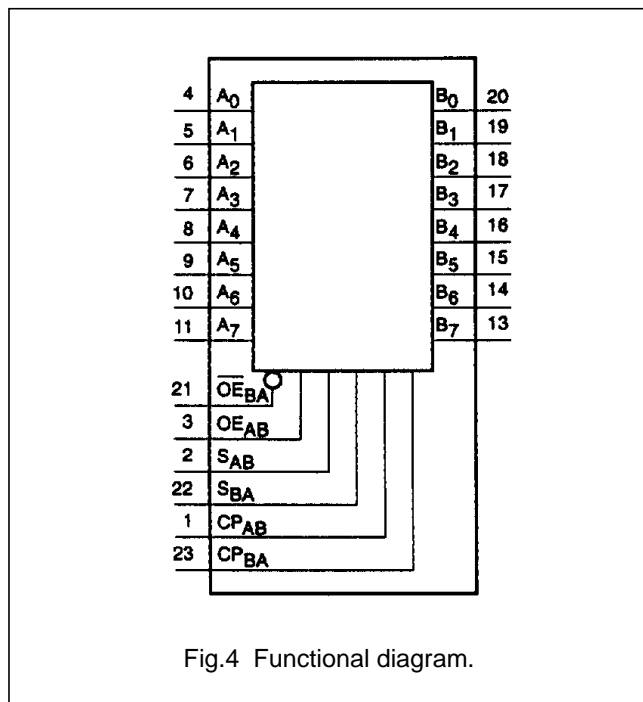
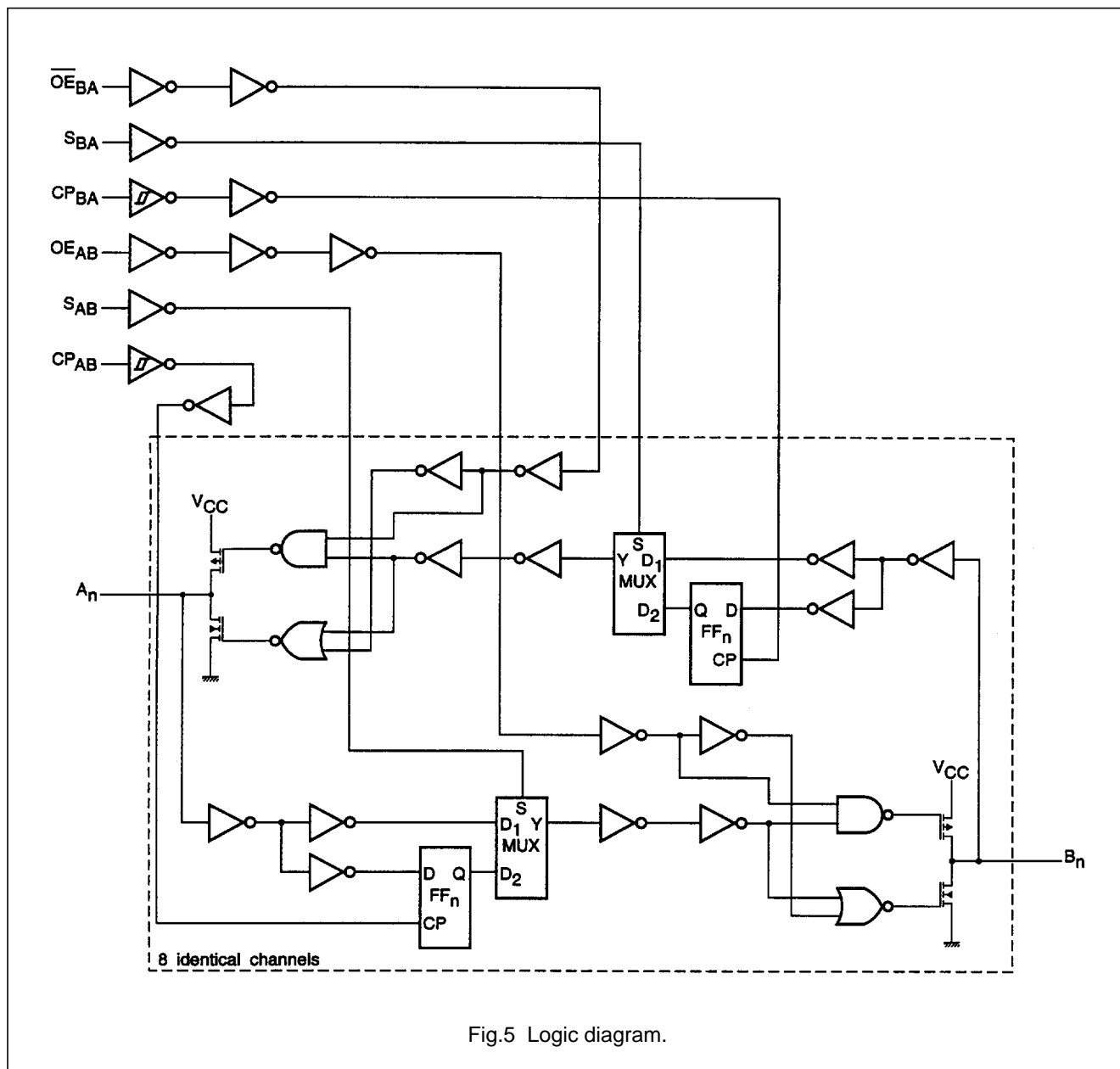


Fig.4 Functional diagram.

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Octal bus transceiver/register; 3-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|-----|------|------------------------|-----------|
| | | 74HC | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | MIN. | TYP. | MAX. | MIN. | MAX. | MIN. | MAX. | | | | |
| t _{PHL} /t _{PLH} | propagation delay A _n , B _n to B _n , A _n | - | 44 | 135 | - | 170 | - | 205 | ns | 2.0 | Fig.6 | |
| | | - | 16 | 27 | - | 34 | - | 41 | | | | |
| | | - | 13 | 23 | - | 29 | - | 35 | | | | |
| t _{PHL} /t _{PLH} | propagation delay CP _{AB} , CP _{BA} to B _n , A _n | - | 61 | 190 | - | 240 | - | 285 | ns | 2.0 | Fig.7 | |
| | | - | 22 | 38 | - | 48 | - | 57 | | | | |
| | | - | 18 | 32 | - | 41 | - | 48 | | | | |
| t _{PHL} /t _{PLH} | propagation delay S _{AB} , S _{BA} to B _n , A _n | - | 63 | 195 | - | 245 | - | 295 | ns | 2.0 | Fig.8 | |
| | | - | 23 | 39 | - | 49 | - | 59 | | | | |
| | | - | 18 | 33 | - | 42 | - | 50 | | | | |
| t _{PZH} /t _{PZL} | 3-state output enable time OE _{AB} , OE _{BA} to A _n , B _n | - | 47 | 150 | - | 190 | - | 225 | ns | 2.0 | Fig.9 | |
| | | - | 17 | 30 | - | 38 | - | 45 | | | | |
| | | - | 14 | 26 | - | 33 | - | 38 | | | | |
| t _{PHZ} /t _{PLZ} | 3-state output disable time OE _{AB} , OE _{BA} to A _n , B _n | - | 41 | 150 | - | 190 | - | 225 | ns | 2.0 | Fig.9 | |
| | | - | 15 | 30 | - | 38 | - | 45 | | | | |
| | | - | 12 | 26 | - | 33 | - | 38 | | | | |
| t _{THL} /t _{TLH} | output transition time | - | 14 | 60 | - | 75 | - | 90 | ns | 2.0 | Figs 6, 8 | |
| | | - | 5 | 12 | - | 15 | - | 18 | | | | |
| | | - | 4 | 10 | - | 13 | - | 15 | | | | |
| t _W | clock pulse width HIGH or LOW CP _{AB} or CP _{BA} | 80 | 17 | - | 100 | - | 120 | - | ns | 2.0 | Fig.7 | |
| | | 16 | 6 | - | 20 | - | 24 | - | | | | |
| | | 14 | 5 | - | 17 | - | 20 | - | | | | |
| t _{SU} | set-up time A _n , B _n to CP _{AB} , CP _{BA} | 100 | 17 | - | 125 | - | 150 | - | ns | 2.0 | Fig.7 | |
| | | 20 | 6 | - | 25 | - | 30 | - | | | | |
| | | 17 | 5 | - | 21 | - | 26 | - | | | | |
| t _H | hold time A _n , B _n to CP _{AB} , CP _{BA} | 25 | -8 | - | 30 | - | 35 | - | ns | 2.0 | Fig.7 | |
| | | 5 | -3 | - | 6 | - | 7 | - | | | | |
| | | 4 | -2 | - | 5 | - | 6 | - | | | | |
| f _{max} | maximum clock pulse frequency | 6.0 | 16 | - | 4.8 | - | 4.0 | - | MHz | 2.0 | Fig.7 | |
| | | 30 | 83 | - | 24 | - | 20 | - | | | | |
| | | 35 | 98 | - | 28 | - | 24 | - | | | | |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI.

Note to the HCT types

The value of additional quiescent supply current (ΔI_{CC}) for unit a load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below

| INPUT | UNIT LOAD COEFFICIENT |
|---|-----------------------|
| S _{AB} , S _{BA} | 0.75 |
| A ₀ to A ₇ and B ₀ to B ₇ | 0.75 |
| CP _{AB} , CP _{BA} | 1.50 |
| OE _{AB} | 1.50 |
| \overline{OE}_{BA} | 1.50 |

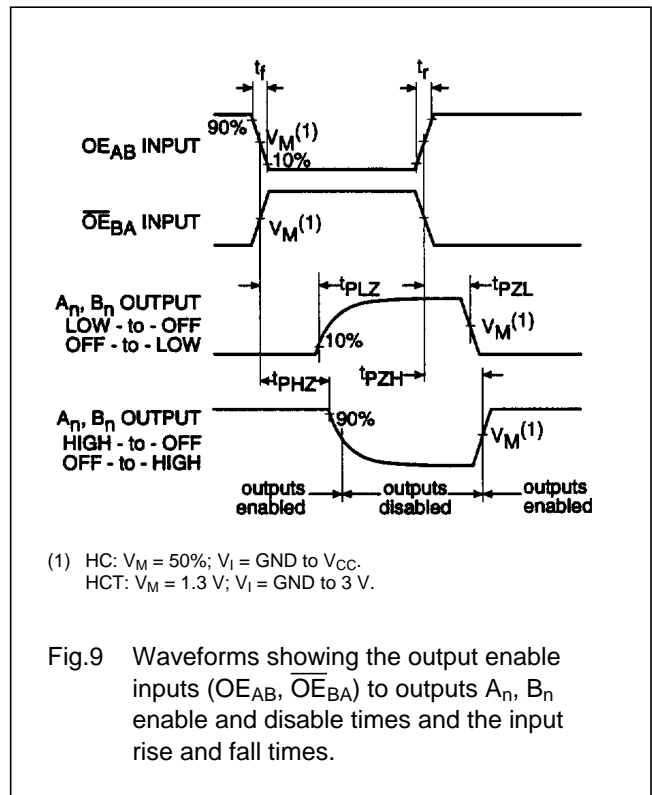
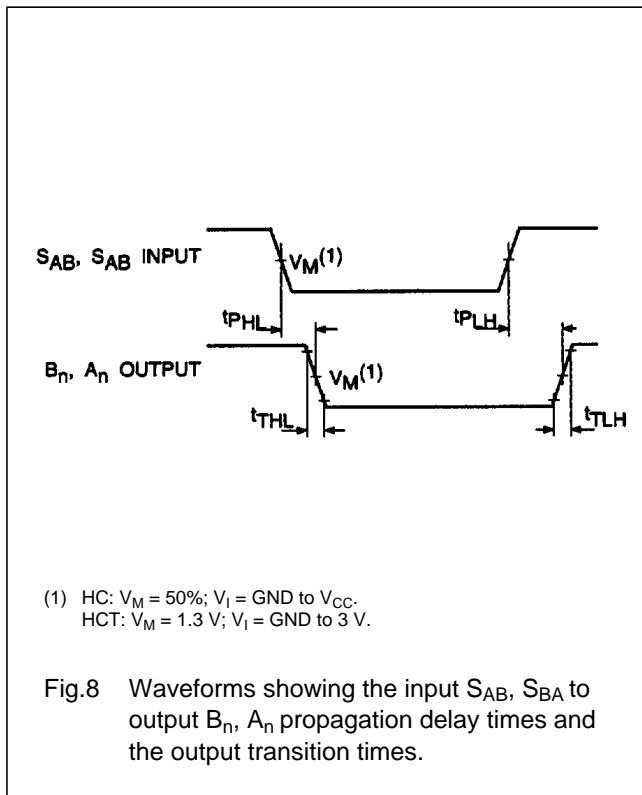
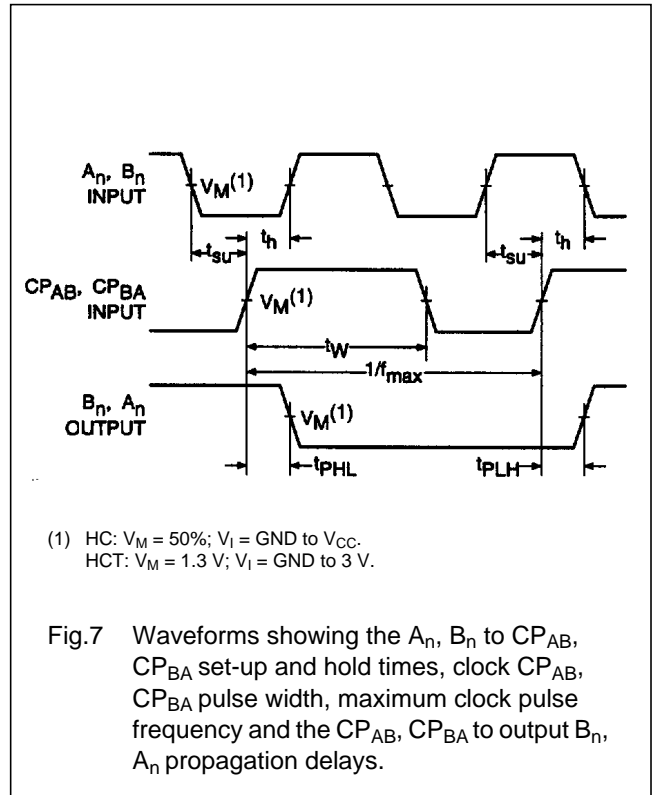
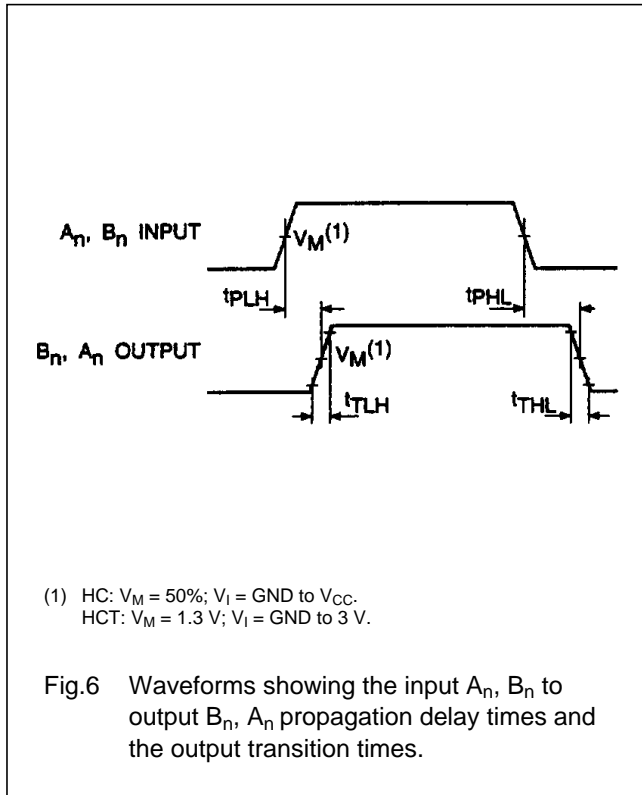
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.

| INPUT | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------------------------|-----------|----------|
| | | +25 | | | -40 to +85 | | -40 to +125 | | V _{CC} (V) | WAVEFORMS | |
| | | MIN. | TYP. | MAX. | MIN. | MAX. | MIN. | | | | MAX. |
| t _{PHL} /t _{PLH} | propagation delay A _n , B _n to B _n , A _n | – | 16 | 27 | – | 34 | – | 41 | ns | 4.5 | Fig.6 |
| t _{PHL} /t _{PLH} | propagation delay CP _{AB} , CP _{BA} to B _n , A _n | – | 23 | 39 | – | 49 | – | 59 | ns | 4.5 | Fig.7 |
| t _{PHL} /t _{PLH} | propagation delay S _{AB} , S _{BA} to B _n , A _n | – | 27 | 46 | – | 55 | – | 66 | ns | 4.5 | Fig.8 |
| t _{PZH} /t _{PZL} | 3-state output enable time OE _{AB} , \overline{OE}_{BA} to A _n , B _n | – | 18 | 33 | – | 41 | – | 50 | ns | 4.5 | Fig.9 |
| t _{PHZ} /t _{PLZ} | 3-state output disable time OE _{AB} , \overline{OE}_{BA} to A _n , B _n | – | 16 | 35 | – | 44 | – | 53 | ns | 4.5 | Fig.9 |
| t _{THL} /t _{TLH} | output transition time | – | 5 | 12 | – | 15 | – | 18 | ns | 4.5 | Fig.6, 8 |
| t _W | clock pulse width HIGH or LOW CP _{AB} or CP _{BA} | 16 | 6 | – | 20 | – | 24 | – | ns | 4.5 | Fig.7 |
| t _{su} | set-up time A _n , B _n to CP _{AB} , CP _{BA} | 10 | 5 | – | 13 | – | 15 | – | ns | 4.5 | Fig.7 |
| t _h | hold time A _n , B _n to CP _{AB} , CP _{BA} | 5 | –2 | – | 6 | – | 8 | – | ns | 4.5 | Fig.7 |
| f _{max} | maximum clock pulse frequency | 30 | 83 | – | 24 | – | 20 | – | MHz | 4.5 | Fig.7 |

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APPLICATION INFORMATION

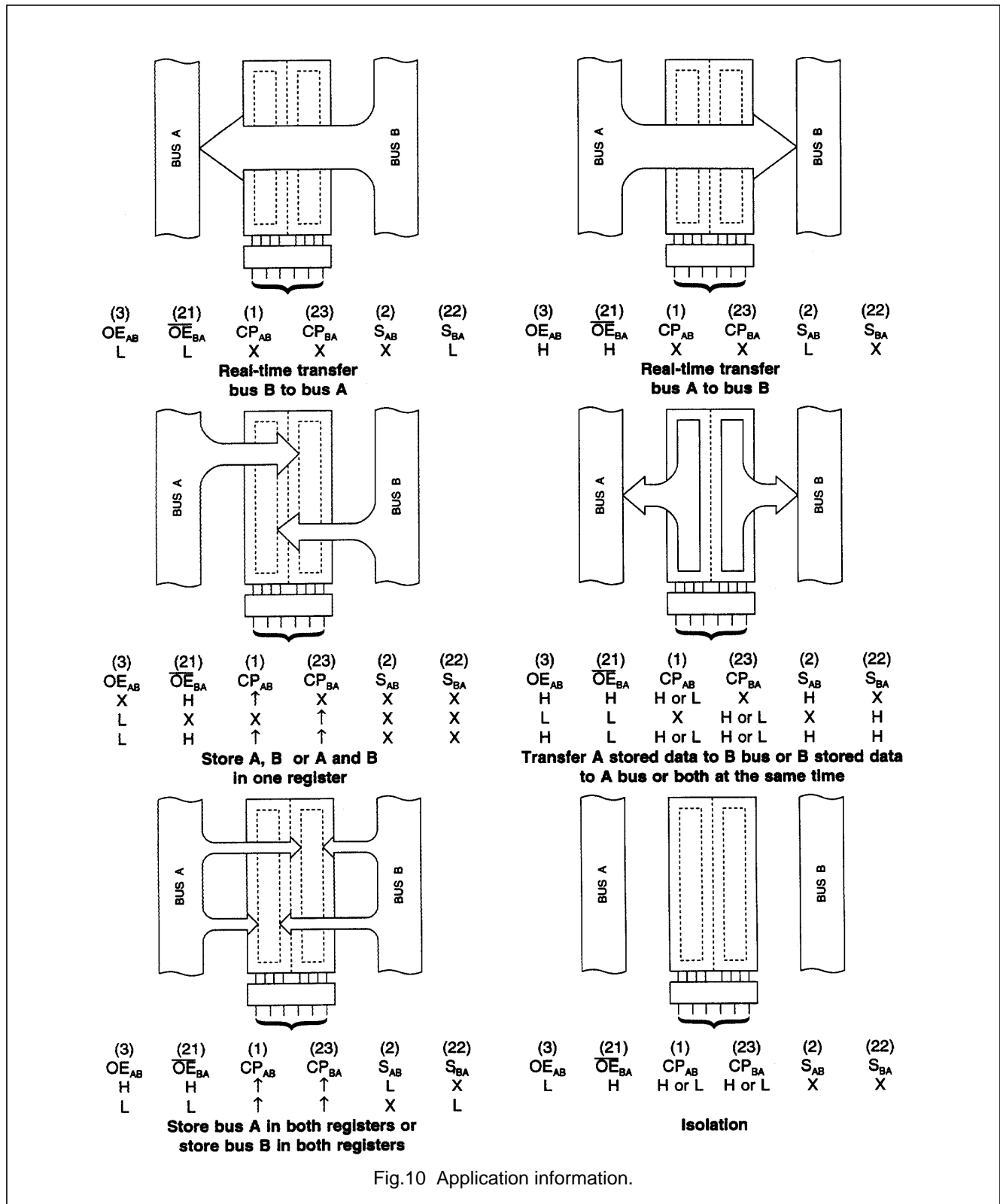


Fig.10 Application information.

Octal bus transceiver/register; 3-state

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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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