THE DATASHEET OF

74HC595PW

74HC595; 74HCT595

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Rev. 12 — 20 March 2024 Product data sheet

1. General description

The 74HC595; 74HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC595: CMOS level
  - For 74HCT595: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC595D 74HCT595D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC595PW 74HCT595PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC595BQ 74HCT595BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HC595BZ	-40 °C to +125 °C	DHXQFN16	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm × 2.4 mm × 0.48 mm	SOT8016-1

5. Functional diagram

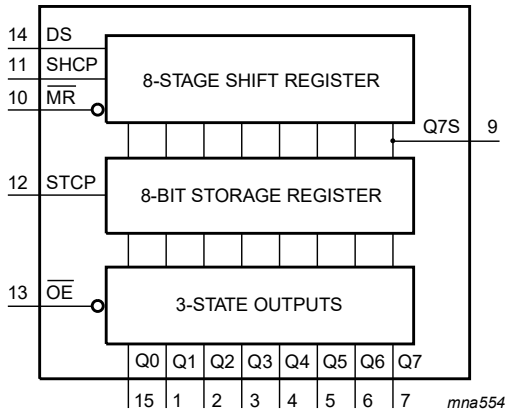


Fig. 1. Functional diagram

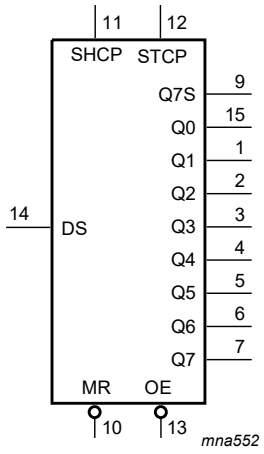


Fig. 2. Logic symbol

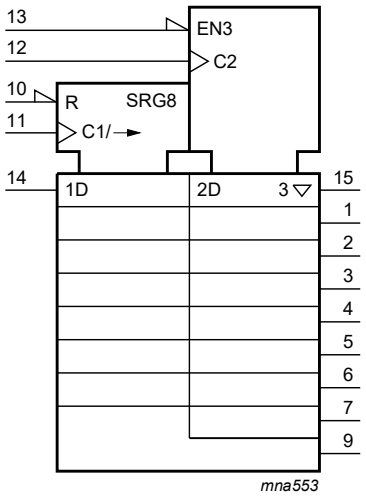


Fig. 3. IEC logic symbol

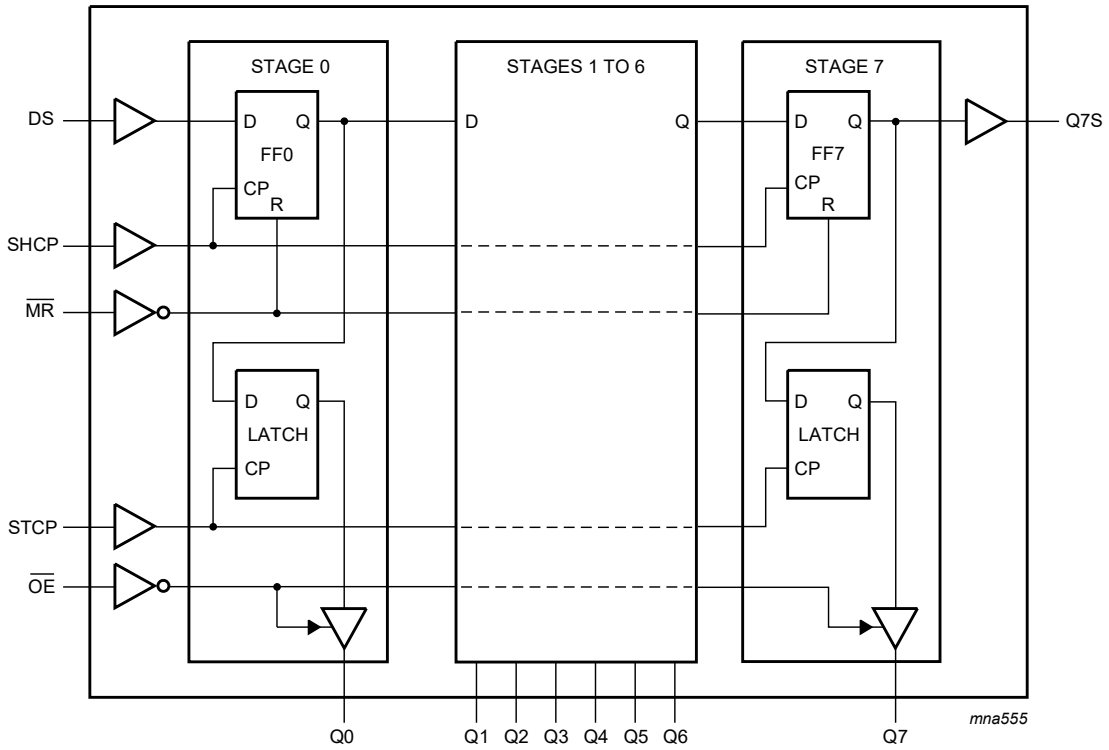
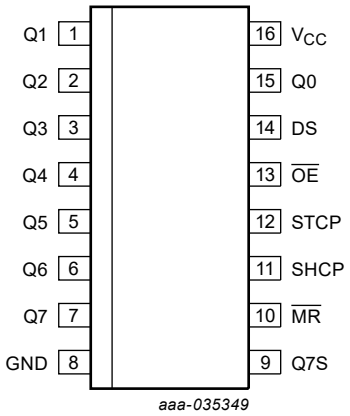


Fig. 4. Logic diagram

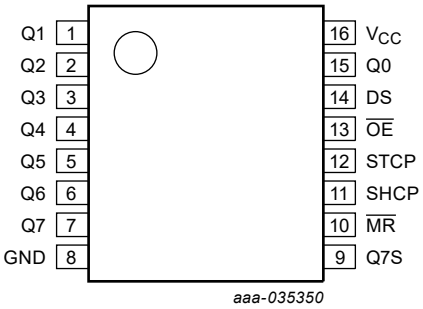
6. Pinning information

6.1. Pinning

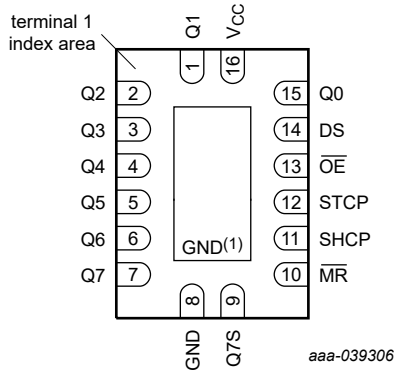
D package
SOT109-1 (SO16)



PW package
SOT403-1 (TSSOP16)

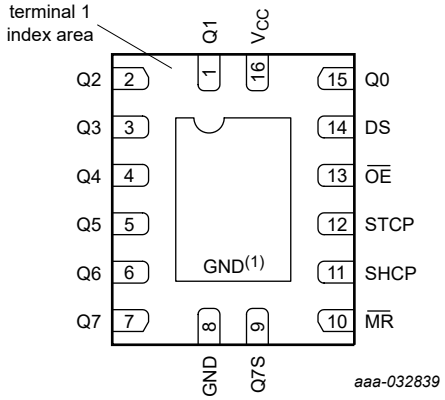


BQ package
SOT763-1 (DHVQFN16)



Transparent top view

BZ package
SOT8016-1 (DHXQFN16)



Transparent top view

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

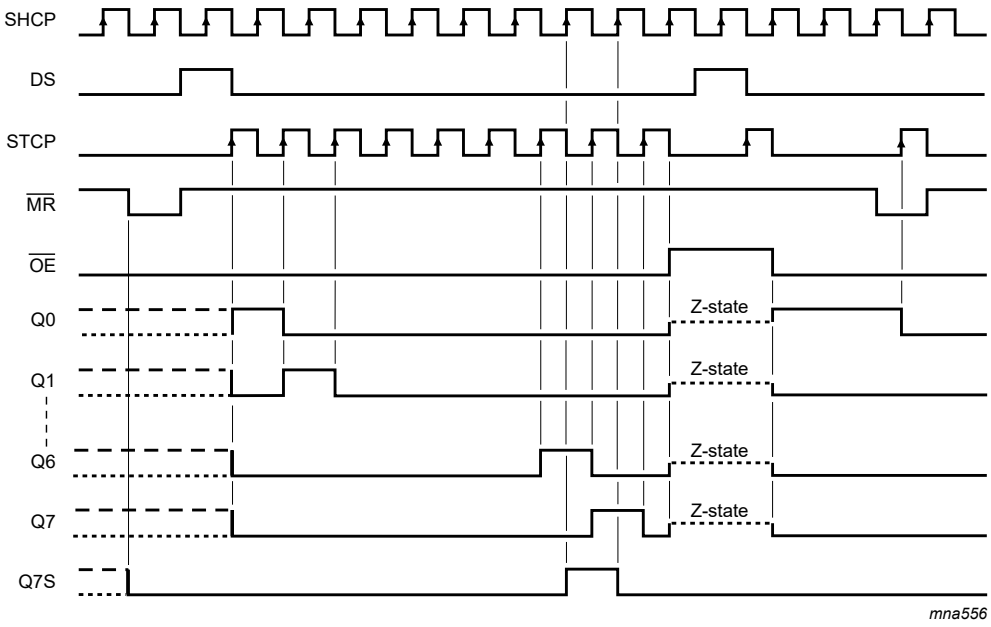


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)			
		pin Q7S	-	±25	mA
		pins Qn	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SOT109-1; SOT403-1; SOT763-1 [1]	-	500	mW
		SOT8016-1	-	250	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC595			74HCT595			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC595								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		all outputs						
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		Q7S output						
		I_O = -4 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
		Qn bus driver outputs						
		I_O = -6 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		all outputs						
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		Q7S output						
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
		Qn bus driver outputs						
		I_O = 6 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	pF
74HCT595								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		all outputs						
		I_O = -20 µA	4.4	4.5	-	4.4	-	V
		Q7S output						
		I_O = -4 mA	3.84	4.32	-	3.7	-	V
		Qn bus driver outputs						
		I_O = -6 mA	3.7	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		all outputs						
		I_O = 20 µA	-	0	0.1	-	0.1	V
		Q7S output						
		I_O = 4.0 mA	-	0.15	0.33	-	0.4	V
		Qn bus driver outputs						
		I_O = 6.0 mA	-	0.16	0.33	-	0.4	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; other inputs at V_{CC} or GND; I_O = 0 A; $V_I = V_{CC}$ - 2.1 V; V_{CC} = 4.5 V to 5.5 V						
		pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	150	675	-	735	µA
		pin DS	-	25	113	-	123	µA
C_I	input capacitance		-	3.5	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

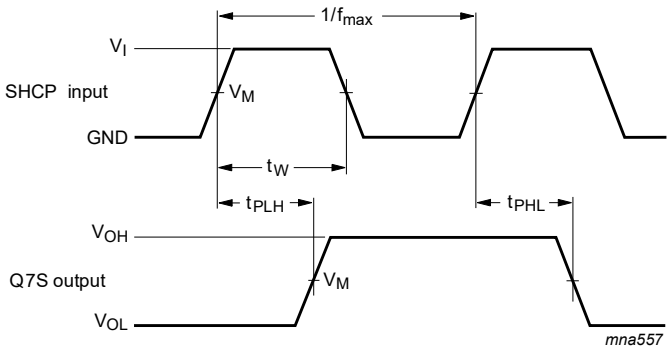
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HC595										
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]								
		V_{CC} = 2 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 6 V	-	15	27	-	34	-	41	ns
		STCP to Qn; see Fig. 7 [2]								
		V_{CC} = 2 V	-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 6 V	-	16	30	-	37	-	45	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 9								
		V_{CC} = 2 V	-	47	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	17	35	-	44	-	53	ns
		V_{CC} = 6 V	-	14	30	-	37	-	45	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 10 [3]								
		V_{CC} = 2 V	-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	17	30	-	38	-	45	ns
		V_{CC} = 6 V	-	14	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 10 [4]								
		V_{CC} = 2 V	-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V_{CC} = 6 V	-	12	27	-	33	-	38	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_W	pulse width	SHCP HIGH or LOW; see Fig. 6								
		V_{CC} = 2 V	75	17	-	95	-	110	-	ns
		V_{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V_{CC} = 6 V	13	5	-	16	-	19	-	ns
		STCP HIGH or LOW; see Fig. 7								
		V_{CC} = 2 V	75	11	-	95	-	110	-	ns
		V_{CC} = 4.5 V	15	4	-	19	-	22	-	ns
		V_{CC} = 6 V	13	3	-	16	-	19	-	ns
		$\overline{MR}$ LOW; see Fig. 9								
		V_{CC} = 2 V	75	17	-	95	-	110	-	ns
		V_{CC} = 4.5 V	15	6	-	19	-	22	-	ns
		V_{CC} = 6 V	13	5	-	16	-	19	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 8								
		V_{CC} = 2 V	50	11	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	4	-	13	-	15	-	ns
		V_{CC} = 6 V	9	3	-	11	-	13	-	ns
		SHCP to STCP; see Fig. 8								
		V_{CC} = 2 V	75	22	-	95	-	110	-	ns
		V_{CC} = 4.5 V	15	8	-	19	-	22	-	ns
		V_{CC} = 6 V	13	7	-	16	-	19	-	ns
t_h	hold time	DS to SHCP; see Fig. 8								
		V_{CC} = 2 V	3	-6	-	3	-	3	-	ns
		V_{CC} = 4.5 V	3	-2	-	3	-	3	-	ns
		V_{CC} = 6 V	3	-2	-	3	-	3	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 9								
		V_{CC} = 2 V	50	-19	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	-7	-	13	-	15	-	ns
		V_{CC} = 6 V	9	-6	-	11	-	13	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Fig. 6 and Fig. 7								
		V_{CC} = 2 V	9	30	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	91	-	24	-	20	-	MHz
		V_{CC} = 6 V	35	108	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [5] [6]	-	115	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HCT595; V_{CC} = 4.5 V to 5.5 V										
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]	-	25	42	-	53	-	63	ns
		STCP to Qn; see Fig. 7 [2]	-	24	40	-	50	-	60	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 9	-	23	40	-	50	-	60	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 10 [3]	-	21	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 10 [4]	-	18	30	-	38	-	45	ns
t_W	pulse width	SHCP HIGH or LOW; see Fig. 6	16	6	-	20	-	24	-	ns
		STCP HIGH or LOW; see Fig. 7	16	5	-	20	-	24	-	ns
		$\overline{MR}$ LOW; see Fig. 9	20	8	-	25	-	30	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 8	16	5	-	20	-	24	-	ns
		SHCP to STCP; see Fig. 8	16	8	-	20	-	24	-	ns
t_h	hold time	DS to SHCP; see Fig. 8	3	-2	-	3	-	3	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 9	10	-7	-	13	-	15	-	ns
f_{max}	maximum frequency	SHCP and STCP; see Fig. 6 and Fig. 7	30	52	-	24	-	20	-	MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; [5] V_I = GND to V_{CC} - 1.5 V [6]	-	130	-	-	-	-	-	pF

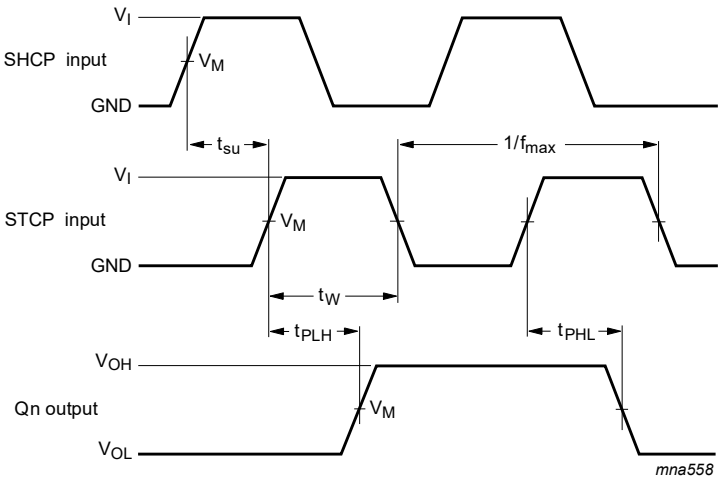
[1] Typical values are measured at nominal supply voltage.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.
[6] All 9 outputs switching.

11.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

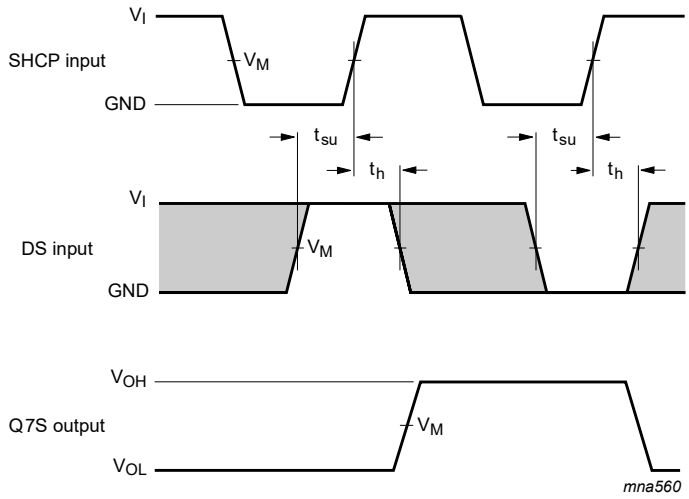
Fig. 6. Shift clock pulse, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Storage clock to output propagation delays

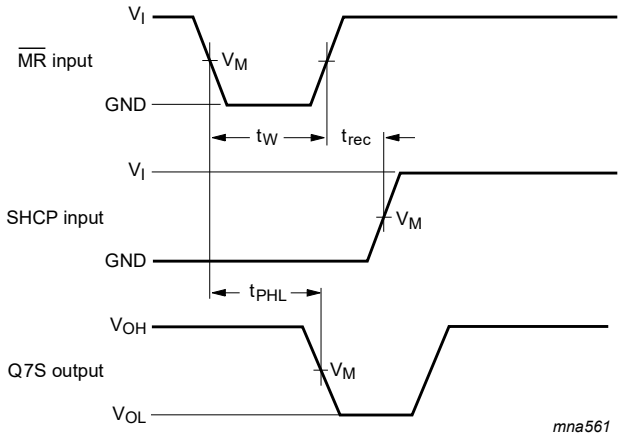


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

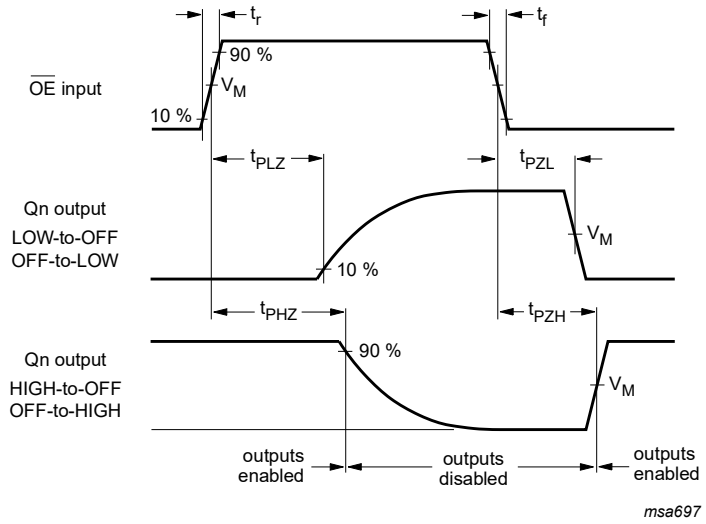
Fig. 8. Data set-up and hold times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Master reset to output propagation delays



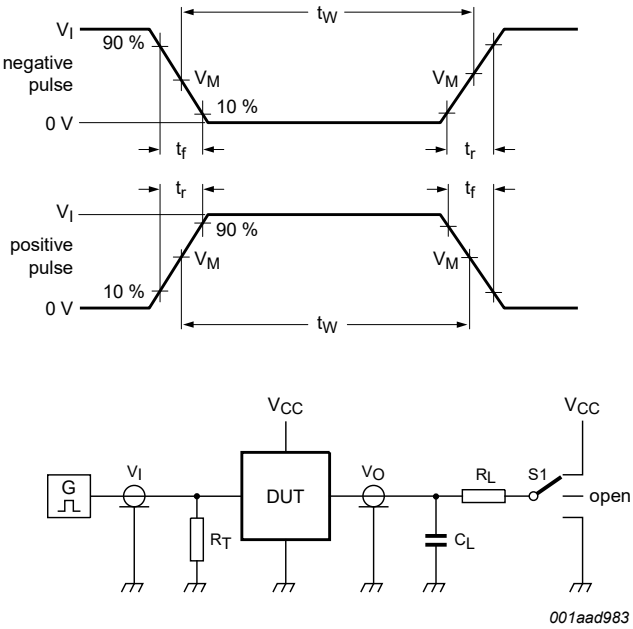
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC595	$0.5V_{CC}$	$0.5V_{CC}$
74HCT595	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

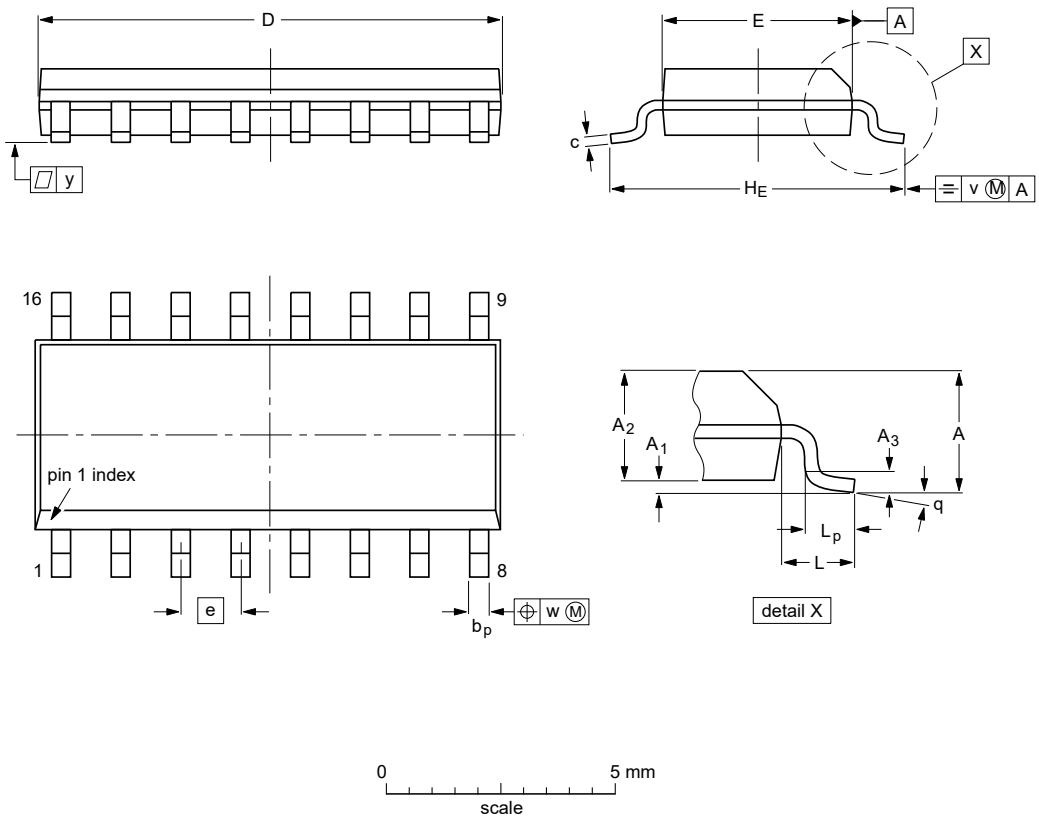
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595	V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT595	3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

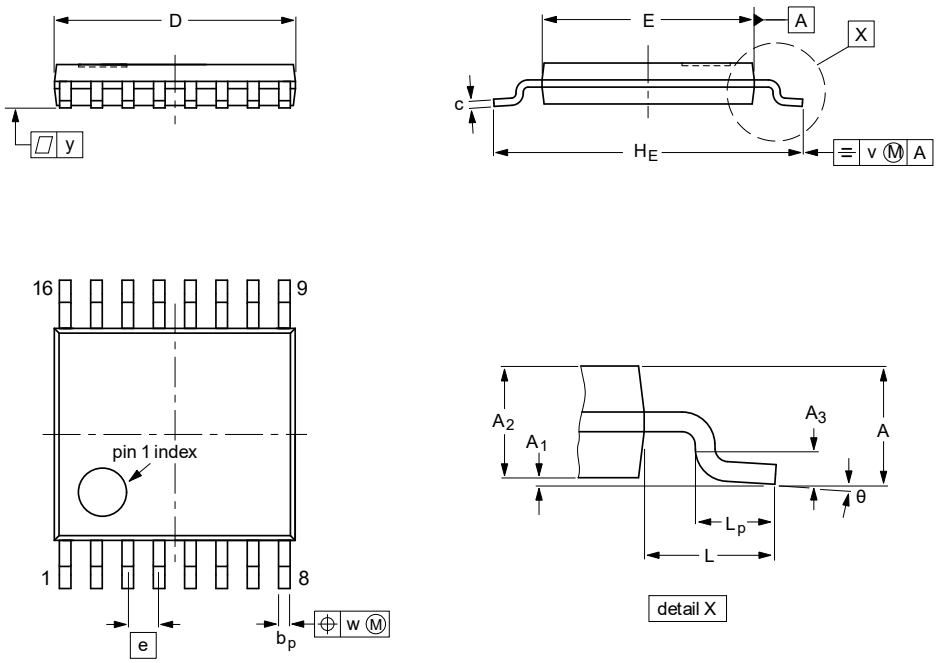
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

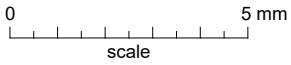
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

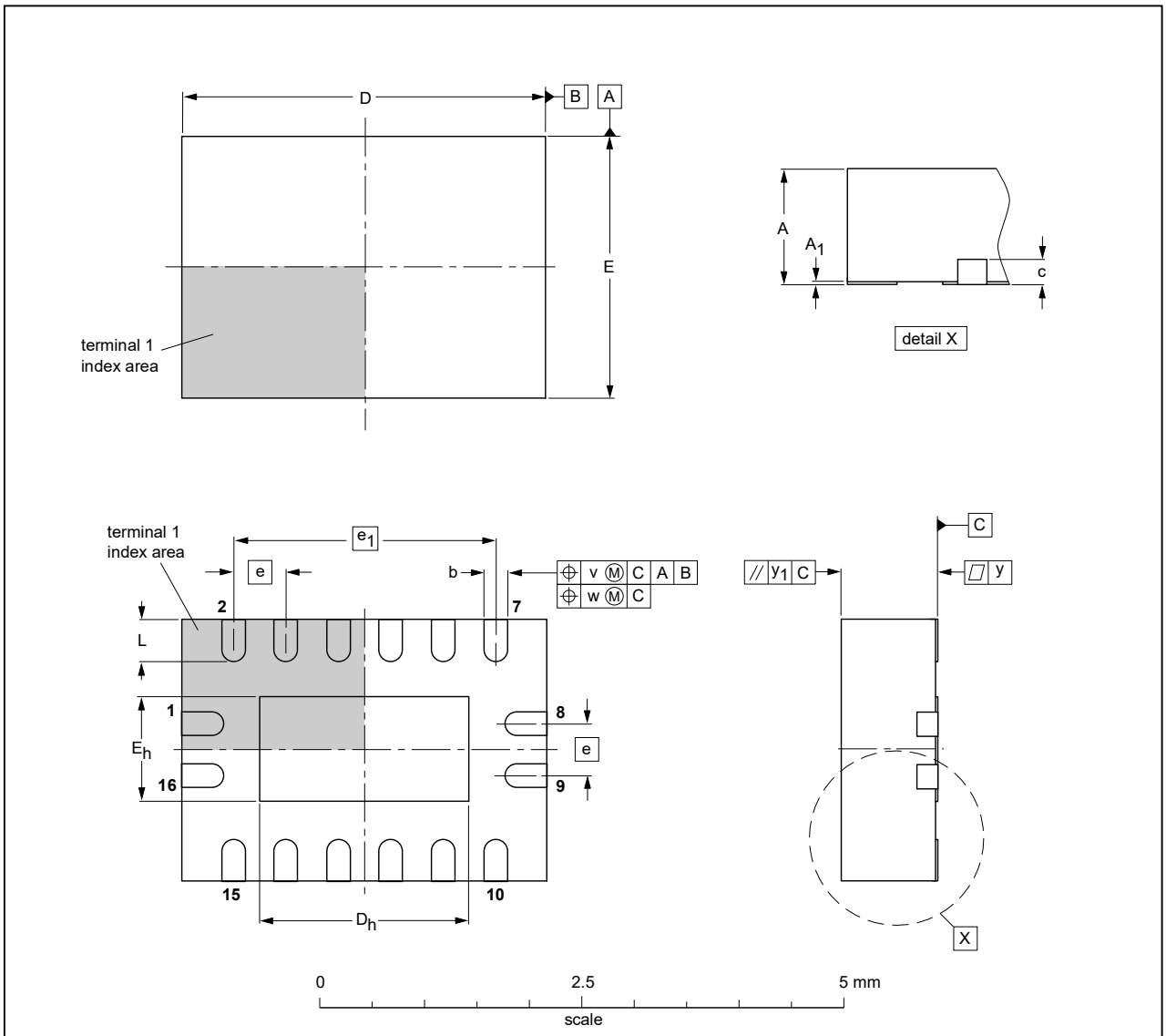
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

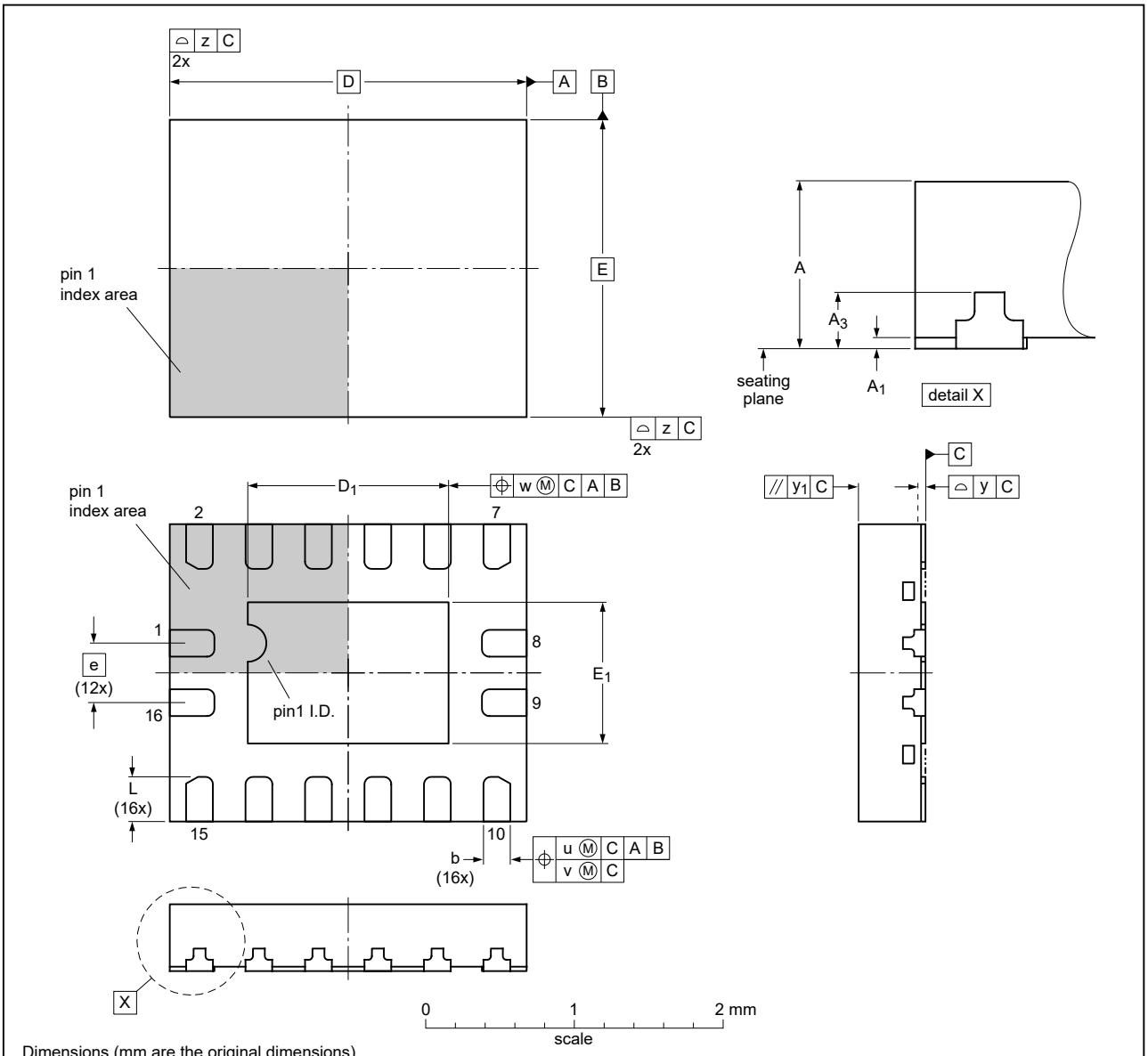
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 14. Package outline SOT763-1 (DHVQFN16)

DHXQFN16: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm x 2.4 mm x 0.48 mm **SOT8016-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_3	b	D	D_1	E	E_1	e	k	L	u	v	w	y	y_1	z
mm	max	0.48	0.05	0.15 (typ)	0.23	2.4	1.40	2.0	1.00	0.4		0.35	0.1	0.05	0.1	0.05	0.05	0.05
	nom	0.45	0.02		0.18		1.35		0.95			0.30						
	min	0.42	0.00		0.13		1.30		0.90		0.2	0.25						

sot8016-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8016-1						~~20-09-18~~ 20-09-22

Fig. 15. Package outline SOT8016-1 (DHXQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT595 v.12	20240320	Product data sheet	-	74HC_HCT595 v.11
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 12 and Fig. 13: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74HC_HCT595 v.11	20210910	Product data sheet	-	74HC_HCT595 v.10
Modifications:	• Type numbers 74HC595DB and 74HCT595DB (SOT338-1/SSOP16) removed. • Section 2updated.			
74HC_HCT595 v.10	20210429	Product data sheet	-	74HC_HCT595 v.9
Modifications:	• Type number 74HC595BZ (SOT8016-1 / DHXQFN16) added. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT595 v.9	20170228	Product data sheet	-	74HC_HCT595 v.8
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT595 v.8	20160225	Product data sheet	-	74HC_HCT595 v.7
Modifications:	• Type numbers 74HC595N and 74HCT595N (SOT38-4) removed.			
74HC_HCT595 v.7	20150126	Product data sheet	-	74HC_HCT595 v.6
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT595 is corrected.			
74HC_HCT595 v.6	20111212	Product data sheet	-	74HC_HCT595 v.5
Modifications:	• Legal pages updated.			
74HC_HCT595 v.5	20110628	Product data sheet	-	74HC_HCT595 v.4
74HC_HCT595 v.4	20030604	Product specification	-	74HC_HCT595_CNV v.3
74HC_HCT595_CNV v.3	19980604	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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