



**THE DATASHEET OF
SN74LVC32ANSR**



SNx4LVC32A Quadruple 2-Input Positive-OR Gates

1 Features

- Operate From 1.65 V to 3.6 V
- Specified From -40°C to $+85^{\circ}\text{C}$, -40°C to $+125^{\circ}\text{C}$, and -55°C to $+125^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theater
- MP3 Players or Recorders
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------|------------|--------------------|
| SN74LVC32AD | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74LVC32ADB | SSOP (14) | 6.20 mm × 5.30 mm |
| SN74LVC32ANS | SO (14) | 10.30 mm × 5.30 mm |
| SN74LVC32APW | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN74LVC32ARGY | VQFN (14) | 3.50 mm × 3.50 mm |
| SN54LVC32AJ | CDIP (14) | 19.56 mm × 6.67 mm |
| SN54LVC32AW | CFP (14) | 9.21 mm × 5.97 mm |
| SN54LVC32AFK | LCCC (20) | 8.89 mm × 8.89 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

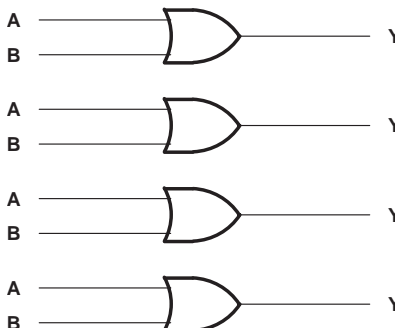


Table of Contents

| | | | | | |
|----------|--|----------|-----------|---|-----------|
| 1 | Features | 1 | 8.1 | Overview | 9 |
| 2 | Applications | 1 | 8.2 | Functional Block Diagram | 9 |
| 3 | Description | 1 | 8.3 | Feature Description | 9 |
| 4 | Revision History | 2 | 8.4 | Device Functional Modes | 9 |
| 5 | Pin Configuration and Functions | 3 | 9 | Application and Implementation | 10 |
| 6 | Specifications | 4 | 9.1 | Application Information | 10 |
| 6.1 | Absolute Maximum Ratings | 4 | 9.2 | Typical Application | 10 |
| 6.2 | ESD Ratings | 4 | 10 | Power Supply Recommendations | 11 |
| 6.3 | Recommended Operating Conditions, SN54LVC32A | 5 | 11 | Layout | 11 |
| 6.4 | Recommended Operating Conditions, SN74LVC32A | 5 | 11.1 | Layout Guidelines | 11 |
| 6.5 | Thermal Information | 6 | 11.2 | Layout Example | 11 |
| 6.6 | Electrical Characteristics, SN54LVC32A | 6 | 12 | Device and Documentation Support | 12 |
| 6.7 | Electrical Characteristics, SN74LVC32A | 6 | 12.1 | Related Links | 12 |
| 6.8 | Switching Characteristics, SN54LVC32A | 7 | 12.2 | Receiving Notification of Documentation Updates | 12 |
| 6.9 | Switching Characteristics, SN74LVC32A | 7 | 12.3 | Community Resources | 12 |
| 6.10 | Operating Characteristics | 7 | 12.4 | Trademarks | 12 |
| 6.11 | Typical Characteristics | 7 | 12.5 | Electrostatic Discharge Caution | 12 |
| 7 | Parameter Measurement Information | 8 | 12.6 | Glossary | 12 |
| 8 | Detailed Description | 9 | 13 | Mechanical, Packaging, and Orderable Information | 12 |

4 Revision History

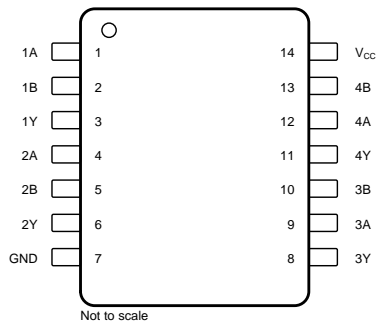
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision Q (December 2014) to Revision R | Page |
|---|-------------|
| • Added CDIP (14), CFP (14), and LCCC (20) packages to <i>Device Information</i> table | 1 |
| • Added Junction temperature, T_J in <i>Absolute Maximum Ratings</i> | 4 |
| • Deleted open-drain from <i>Application Information</i> | 10 |
| • Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section | 12 |

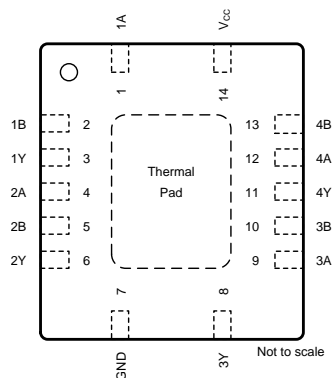
| Changes from Revision P (April 2005) to Revision Q | Page |
|--|-------------|
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table. | 1 |
| • Added Military Disclaimer to <i>Features</i> | 1 |

5 Pin Configuration and Functions

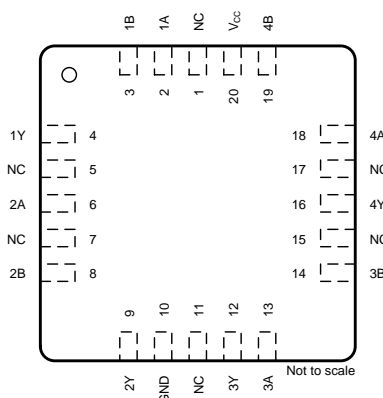
**SN54LVC32A J or W Package
SN74LVC32A D, DB, NS, or PW Package
14-Pin CDIP, CFP, SOIC, SSOP, SO, TSSOP
Top View**



**SN74LVC32A RGY Package
14-Pin VQFN With Thermal Pad
Top View**



**SN54LVC32A FK Package
20-Pin LCCC
Top View**



NC – No internal connection

Pin Functions

| NAME | PIN | | | | TYPE | DESCRIPTION |
|-----------------|---------------|-----|------------|---------------------|------|---------------|
| | SN74LVC32A | | SN54LVC32A | | | |
| | D, DB, NS, PW | RGY | J, W | FK | | |
| 1A | 1 | 1 | 1 | 2 | I | Gate 1 input |
| 1B | 2 | 2 | 2 | 3 | I | Gate 1 input |
| 1Y | 3 | 3 | 3 | 4 | O | Gate 1 output |
| 2A | 4 | 4 | 4 | 6 | I | Gate 2 input |
| 2B | 5 | 5 | 5 | 8 | I | Gate 2 input |
| 2Y | 6 | 6 | 6 | 9 | O | Gate 2 output |
| GND | 7 | 7 | 7 | 10 | — | Ground Pin |
| 3Y | 8 | 8 | 8 | 12 | O | Gate 3 output |
| 3A | 9 | 9 | 9 | 13 | I | Gate 3 input |
| 3B | 10 | 10 | 10 | 14 | I | Gate 3 input |
| 4Y | 11 | 11 | 11 | 16 | O | Gate 4 output |
| 4A | 12 | 12 | 12 | 18 | I | Gate 4 input |
| 4B | 13 | 13 | 13 | 19 | I | Gate 4 input |
| V _{CC} | 14 | 14 | 14 | 20 | — | Power Pin |
| NC | — | — | — | 1, 5, 7, 11, 15, 17 | — | No Connection |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|--|-----------------------|------|----|
| V _{CC} | Supply voltage | -0.5 | 6.5 | V | |
| V _I | Input voltage ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Output voltage ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA | |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA | |
| I _O | Continuous output current | | ±50 | mA | |
| | Continuous current through V _{CC} or GND | | ±100 | mA | |
| P _{tot} | Power dissipation | T _A = -40°C to +125°C ⁽⁴⁾⁽⁵⁾ | 500 | mW | |
| T _J | Junction temperature | | 150 | °C | |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* tables.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | | V |
| | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 | |
| | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions, SN54LVC32A

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54LVC32A | | UNIT | |
|-----------------|-------------------------------------|----------------------------------|-----------------|------|------|
| | | –55 to +125°C | | | |
| | | MIN | MAX | | |
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 2 | V |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 0.8 | V |
| V _I | Input voltage | 0 | 5.5 | | V |
| V _O | Output voltage | 0 | V _{CC} | | V |
| I _{OH} | High-level output current | V _{CC} = 2.7 V | | –12 | mA |
| | | V _{CC} = 3 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 2.7 V | | 12 | mA |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δv | Input transition rise and fall rate | | | 7 | ns/V |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.4 Recommended Operating Conditions, SN74LVC32A

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN74LVC32A | | | | | | UNIT | |
|-----------------|-------------------------------------|------------------------------------|------------------------|--------------|------------------------|---------------|------------------------|------|----|
| | | T _A = 25°C | | –40 to +85°C | | –40 to +125°C | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | 1.7 | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | 0.7 | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | | 0.8 | | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | | –4 | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | | –8 | | –8 | |
| | | V _{CC} = 2.7 V | | –12 | | –12 | | –12 | |
| | | V _{CC} = 3 V | | –24 | | –24 | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | | 4 | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | | 8 | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | | 12 | | 12 | |
| | | V _{CC} = 3 V | | 24 | | 24 | | 24 | |
| Δt/Δv | Input transition rise and fall rate | | 7 | | 7 | | 7 | ns/V | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SNx4LVC32A | | | | | UNIT |
|---|------------|---------|---------|---------|---------|------|
| | D | DB | NS | PW | RGY | |
| | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 86 | 96 | 76 | 113 | 47 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LVC32A | | UNIT |
|------------------|--|-----------------|-----------------------|-----|------|
| | | | –55 to +125°C | | |
| | | | MIN | MAX | |
| V _{OH} | I _{OH} = –100 μA | 2.7 V to 3.6 V | V _{CC} – 0.2 | | V |
| | I _{OH} = –12 mA | 2.7 V | 2.2 | | |
| | I _{OH} = –24 mA | 3 V | 2.4 | | |
| V _{OL} | I _{OL} = 100 μA | 2.7 V to 3.6 V | 0.2 | | V |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±5 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 10 | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | μA |

6.7 Electrical Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN74LVC32A | | | | | | UNIT | |
|--------------------------|--|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|------|-----|
| | | | T _A = 25°C | | | –40 to +85°C | | –40 to +125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 3.6 V | V _{CC} – 0.2 | | | V _{CC} – 0.2 | | V _{CC} – 0.3 | | V |
| | I _{OH} = –4 mA | 1.65 V | 1.29 | | | 1.2 | | 1.05 | | |
| | I _{OH} = –8 mA | 2.3 V | 1.9 | | | 1.7 | | 1.55 | | |
| | I _{OH} = –12 mA | 2.7 V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3 V | 2.4 | | | 2.4 | | 2.25 | | |
| I _{OH} = –24 mA | 3 V | 2.3 | | | 2.2 | | 2 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.1 | | | 0.2 | | 0.3 | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.24 | | | 0.45 | | 0.6 | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.7 | | 0.85 | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | 0.4 | | 0.6 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | 0.55 | | 0.8 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±1 | | | ±5 | | ±20 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 1 | | | 10 | | 40 | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | 500 | | 5000 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | | | | | | pF |

6.8 Switching Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN54LVC32A | | UNIT |
|-----------------|--------------|-------------|-----------------|---------------|-----|------|
| | | | | –55 to +125°C | | |
| | | | | MIN | MAX | |
| t _{pd} | A or B | Y | 2.7 V | 4.4 | | ns |
| | | | 3.3 V ± 0.3 V | 1 | 3.8 | |

6.9 Switching Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN74LVC32A | | | | | | UNIT | |
|--------------------|--------------|-------------|-----------------|-----------------------|-----|-----|--------------|-----|---------------|------|-----|
| | | | | T _A = 25°C | | | –40 to +85°C | | –40 to +125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| t _{pd} | A or B | Y | 1.8 V ± 0.15 V | 1 | 4.2 | 8.2 | 1 | 8.7 | 1 | 10.2 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 2.6 | 4.9 | 1 | 5.4 | 1 | 6.9 | |
| | | | 2.7 V | 1 | 3 | 4.2 | 1 | 4.4 | 1 | 5.5 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.5 | 3.6 | 1 | 3.8 | 1 | 5 | |
| t _{sk(o)} | | | 3.3 V ± 0.3 V | | | | 1 | | 1.5 | ns | |

6.10 Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|-----------------|--|-----------------|-----------------|------|------|
| C _{pd} | Power dissipation capacitance per gate | f = 10 MHz | 1.8 V | 7.5 | pF |
| | | | 2.5 V | 10.6 | |
| | | | 3.3 V | 12.5 | |

6.11 Typical Characteristics

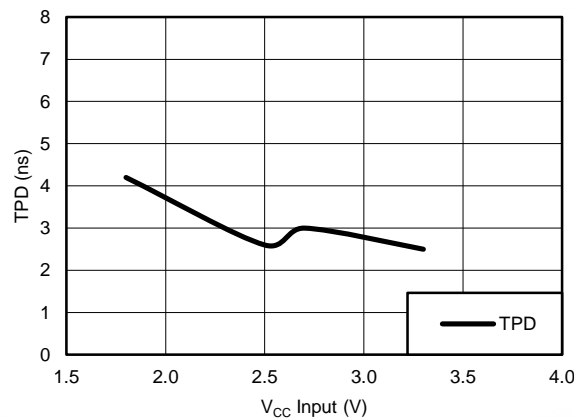
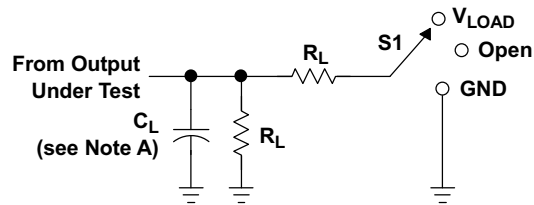


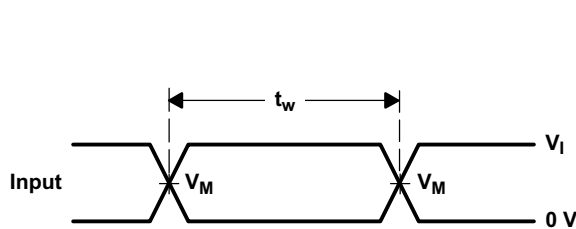
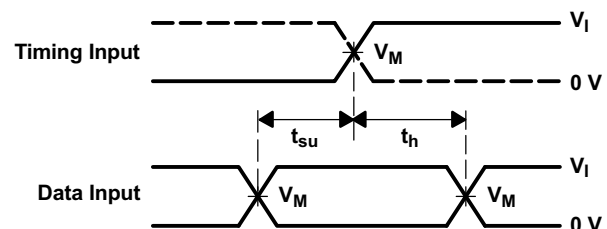
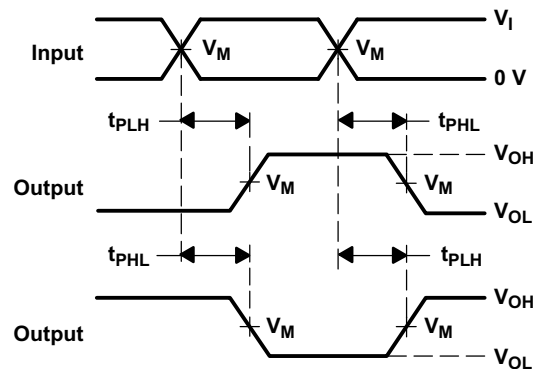
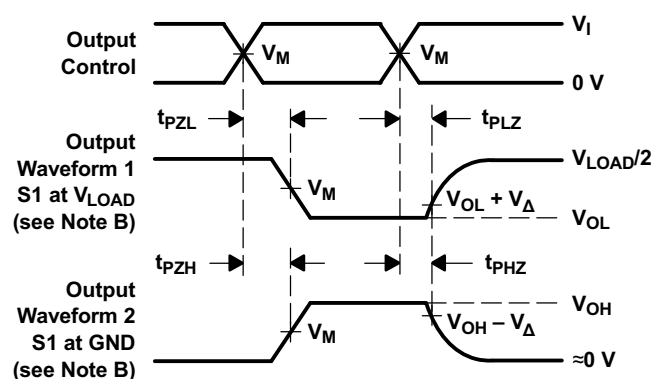
Figure 1. TPD vs V_{CC} (T_A = 25°C)

7 Parameter Measurement Information


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2-V to 3.6-V V_{CC} operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V/5-V system environment.

8.2 Functional Block Diagram

Logic Diagram, Each Gate (Positive Logic)



8.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows up or down voltage translation
 - Inputs accept voltages to 5.5 V

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of SNx4LVC32A.

**Table 1. Function Table
(Each Gate)**

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | X | H |
| X | H | H |
| L | L | L |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74LVC32A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate down to V_{CC} .

9.2 Typical Application

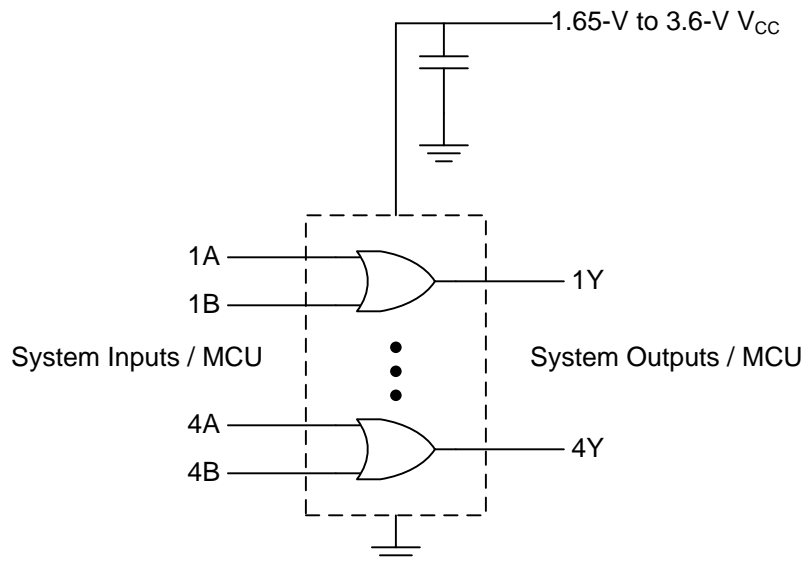


Figure 3. Typical OR Gate Application and Supply Voltage

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions, SN74LVC32A](#) table.
 - Specified high and low levels: See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions, SN74LVC32A](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above 5.5 V.

Typical Application (continued)

9.2.3 Application Curve

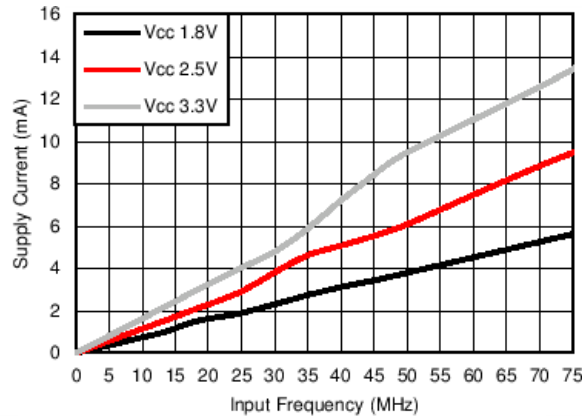


Figure 4. Supply Current vs Input Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions, SN74LVC32A](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Layout Example](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

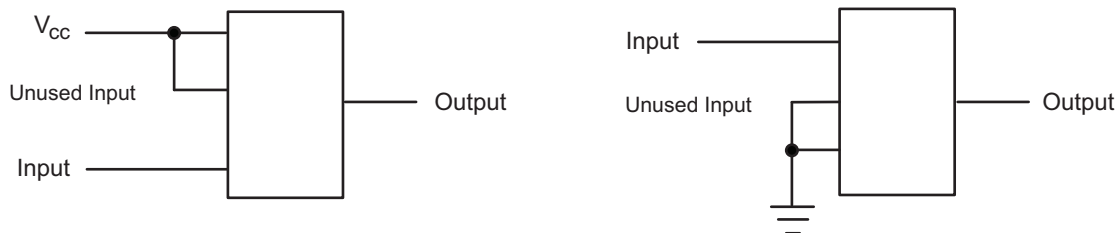


Figure 5. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC32A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC32A | Click here | Click here | Click here | Click here | Click here |

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-9761801Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9761801Q2A SNJ54LVC32AFK | Samples |
| 5962-9761801QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9761801QC A SNJ54LVC32AJ | Samples |
| 5962-9761801QDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9761801QD A SNJ54LVC32AW | Samples |
| SN74LVC32AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32ADT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32ADTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32A | Samples |
| SN74LVC32APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74LVC32APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWRG3 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC32A | Samples |
| SN74LVC32ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC32A | Samples |
| SNJ54LVC32AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9761801Q2A SNJ54LVC32AFK | Samples |
| SNJ54LVC32AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9761801QC A SNJ54LVC32AJ | Samples |
| SNJ54LVC32AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9761801QD A SNJ54LVC32AW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVC32A, SN74LVC32A :

- Catalog: [SN74LVC32A](#)
- Automotive: [SN74LVC32A-Q1](#), [SN74LVC32A-Q1](#)
- Enhanced Product: [SN74LVC32A-EP](#), [SN74LVC32A-EP](#)
- Military: [SN54LVC32A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC32ADR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC32ADR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LVC32ADT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC32ANSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC32APWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC32APWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC32APWRG3 | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC32APWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC32APWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |
| SN74LVC32ARGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - $\triangle F$ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



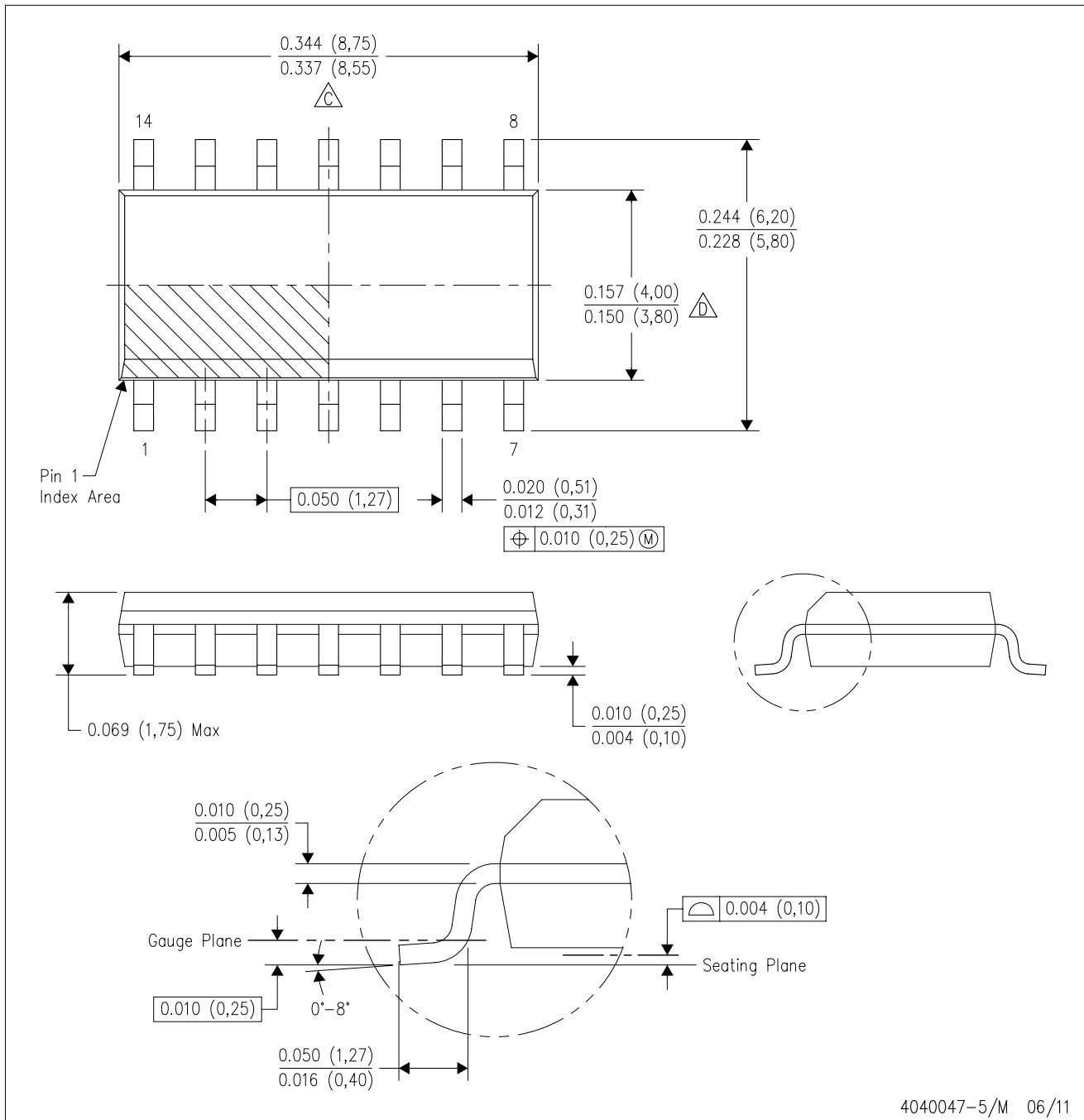
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management