



**THE DATASHEET OF  
SN74LVC08ANSR**



## SN74LVC08A Quadruple 2-Input Positive-AND Gates

### 1 Features

- Operate From 1.65 V to 3.6 V
- Specified From  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.1 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- $I_{off}$  Support Live Insertion, Partial-Power-Down Mode and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
  - On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Servers
- LED Displays
- Network Switches
- I/O expanders
- Base station processor board

### 3 Description

The SN54LVC08A quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC08A quadruple 2-input positive-AND gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The LVC08A devices perform the Boolean function  $Y = A \cdot B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| SNJ54LVC08A | CFP (14)   | 9.21 mm × 5.97 mm  |
|             | CDIP (14)  | 19.56 mm × 6.92 mm |
|             | LCCC (20)  | 8.89 mm × 8.89 mm  |
| SN74LVC08A  | VQFN (14)  | 3.50 mm × 3.50 mm  |
|             | TSSOP (14) | 5.00 mm × 4.40 mm  |
|             | SOP (14)   | 10.30 mm × 5.30 mm |
|             | SOIC (14)  | 8.65 mm × 3.91 mm  |
|             | SSOP (14)  | 6.20 mm × 5.30 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram, Each Gate (Positive Logic)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision R (June 2015) to Revision S</b>         | <b>Page</b> |
|--|-------------|
| • Added $T_J$ junction temperature spec to Abs Max Ratings ..... | <b>5</b>    |

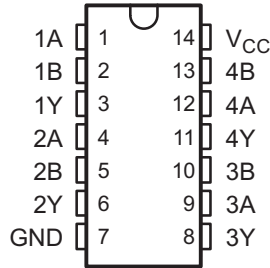
| <b>Changes from Revision Q (November 2010) to Revision R</b>  | <b>Page</b> |
|---|-------------|
| • Updated document to new TI data sheet format - no specification changes. ....   | <b>1</b>    |
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b>    |
| • Added Military Disclaimer to <i>Features</i> .....  | <b>1</b>    |
| • Added <i>Thermal Information</i> table .....  | <b>6</b>    |

## 5 Device Options

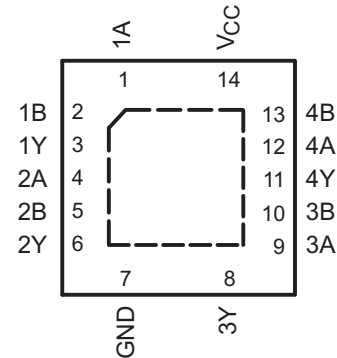
| PART NUMBER    | PACKAGE    | BODY SIZE          |
|----------------|------------|--------------------|
| SNJ54LVC08AW   | CFP (14)   | 9.21 mm × 5.97 mm  |
| SNJ54LVC08AJ   | CDIP (14)  | 19.56 mm × 6.92 mm |
| SNJ54LVC08AFK  | LCCC (20)  | 8.89 mm × 8.89 mm  |
| SN74LVC08ARGYR | VQFN (14)  | 3.50 mm × 3.50 mm  |
| SN74LVC08APW   | TSSOP (14) | 5.00 mm × 4.40 mm  |
| SN74LVC08APWT  |            |                    |
| SN74LVC08APWG3 |            |                    |
| SN74LVC08ANSR  | SOP (14)   | 10.30 mm × 5.30 mm |
| SN74LVC08AD    | SOIC (14)  | 8.65 mm × 3.91 mm  |
| SN74LVC08ADT   |            |                    |
| SN74LVC08ADRG3 |            |                    |
| SN74LVC08ADBR  | SSOP (14)  | 6.20 mm × 5.30 mm  |

## 6 Pin Configuration and Functions

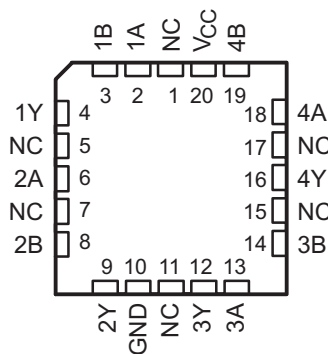
**D, DB, NS, J, W, or PW Package**  
**14-Pin SOIC, SSOP, SOP, CDIP, or TSSOP**  
**Top View**



**RGY Package**  
**14-Pin VQFN**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



### Pin Functions

| PIN             |                                 |      |        |                           |
|-----------------|---------------------------------|------|--------|---------------------------|
| NAME            | SOIC, SSOP, SOP, CDIP, or TSSOP | LCCC | TYPE   | DESCRIPTION               |
| 1A              | 1                               | 2    | I      | AND Gate Input            |
| 1B              | 2                               | 3    | I      | AND Gate Input            |
| 1Y              | 3                               | 4    | O      | AND Gate Output           |
| 2A              | 4                               | 6    | I      | AND Gate Input            |
| 2B              | 5                               | 8    | I      | AND Gate Input            |
| 2Y              | 6                               | 9    | O      | AND Gate Output           |
| GND             | 7                               | 10   | Ground | Ground pin for the device |
| 3Y              | 8                               | 12   | O      | AND Gate Output           |
| 3A              | 9                               | 13   | I      | AND Gate Input            |
| 3B              | 10                              | 14   | I      | AND Gate Input            |
| 4Y              | 11                              | 16   | O      | AND Gate Output           |
| 4A              | 12                              | 18   | I      | AND Gate Input            |
| 4B              | 13                              | 19   | I      | AND Gate Input            |
| V <sub>CC</sub> | 14                              | 20   | Power  | Power pin for the device  |

**Pin Functions (continued)**

| PIN               |                                 | LCCC | TYPE | DESCRIPTION |
|-------------------|---------------------------------|------|------|-------------|
| NAME              | SOIC, SSOP, SOP, CDIP, or TSSOP |      |      |             |
| NC <sup>(1)</sup> | —                               | 1    | —    | No connect  |
|                   |                                 | 5    |      |             |
|                   |                                 | 7    |      |             |
|                   |                                 | 11   |      |             |
|                   |                                 | 15   |      |             |
|                   |                                 | 17   |      |             |

(1) NC – No internal connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|   |                                     | MIN                             | MAX                   | UNIT |    |
|---|-------------------------------------|---------------------------------|-----------------------|------|----|
| V <sub>CC</sub>                                   | Supply voltage                      | -0.5                            | 6.5                   | V    |    |
| V <sub>I</sub>                                    | Input voltage <sup>(2)</sup>        | -0.5                            | 6.5                   | V    |    |
| V <sub>O</sub>                                    | Output voltage <sup>(2)(3)</sup>    | -0.5                            | V <sub>CC</sub> + 0.5 | V    |    |
| I <sub>IK</sub>                                   | Input clamp current                 | V <sub>I</sub> < 0              |                       | -50  | mA |
| I <sub>OK</sub>                                   | Output clamp current                | V <sub>O</sub> < 0              |                       | -50  | mA |
| I <sub>O</sub>                                    | Continuous output current           |                                 |                       | ±50  | mA |
| Continuous current through V <sub>CC</sub> or GND |                                     |                                 |                       | ±100 | mA |
| P <sub>tot</sub>                                  | Power dissipation <sup>(4)(5)</sup> | T <sub>A</sub> = -40°C to 125°C |                       | 500  | mW |
| T <sub>J</sub>                                    | Junction temperature                | -65                             | 150                   | °C   |    |
| T <sub>stg</sub>                                  | Storage temperature                 | -65                             | 150                   | °C   |    |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P<sub>tot</sub> derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

### 7.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions for SN54LVC08A<sup>(1)</sup>

|                 |                          | SN54LVC08A                       |     | UNIT |
|-----------------|--------------------------|----------------------------------|-----|------|
|                 |                          | -55°C to 125°C                   |     |      |
|                 |                          | MIN                              | MAX |      |
| V <sub>CC</sub> | Supply voltage           | Operating                        | 2   | 3.6  |
|                 |                          | Data retention only              | 1.5 |      |
| V <sub>IH</sub> | High-level input voltage | V <sub>CC</sub> = 2.7 V to 3.6 V |     | 2    |
| V <sub>IL</sub> | Low-level input voltage  | V <sub>CC</sub> = 2.7 V to 3.6 V |     | 0.8  |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

**Recommended Operating Conditions for SN54LVC08A<sup>(1)</sup> (continued)**

|                 |                                    | SN54LVC08A              |                 | UNIT   |
|-----------------|------------------------------------|-------------------------|-----------------|--------|
|                 |                                    | –55°C to 125°C          |                 |        |
|                 |                                    | MIN                     | MAX             |        |
| V <sub>I</sub>  | Input voltage                      | 0                       | 5.5             | V      |
| V <sub>O</sub>  | Output voltage                     | 0                       | V <sub>CC</sub> | V      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2.7 V |                 | –12    |
|                 |                                    | V <sub>CC</sub> = 3 V   |                 | –24    |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2.7 V |                 | 12     |
|                 |                                    | V <sub>CC</sub> = 3 V   |                 | 24     |
| Δt/Δv           | Input transition rise or fall rate |                         |                 | 8 ns/V |

**7.4 Recommended Operating Conditions for SN74LVC08A<sup>(1)</sup>**

|                 |                                    | SN74LVC08A                         |                 |                        |                 |                        |                 | UNIT                   |                 |      |
|-----------------|------------------------------------|------------------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------|
|                 |                                    | T <sub>A</sub> = 25°C              |                 | –40°C to 85°C          |                 | –40°C to 125°C         |                 |                        |                 |      |
|                 |                                    | MIN                                | MAX             | MIN                    | MAX             | MIN                    | MAX             |                        |                 |      |
| V <sub>CC</sub> | Supply voltage                     | Operating                          |                 | 1.65                   | 3.6             | 1.65                   | 3.6             | 1.65                   | 3.6             | V    |
|                 | Data retention only                |                                    | 1.5             |                        | 1.5             |                        | 1.5             |                        |                 |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V |                 | 0.65 × V <sub>CC</sub> |                 | 0.65 × V <sub>CC</sub> |                 | 0.65 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   |                 | 1.7                    |                 | 1.7                    |                 | 1.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   |                 | 2                      |                 | 2                      |                 | 2                      |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V |                 | 0.35 × V <sub>CC</sub> |                 | 0.35 × V <sub>CC</sub> |                 | 0.35 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   |                 | 0.7                    |                 | 0.7                    |                 | 0.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   |                 | 0.8                    |                 | 0.8                    |                 | 0.8                    |                 |      |
| V <sub>I</sub>  | Input voltage                      | 0                                  | 5.5             | 0                      | 5.5             | 0                      | 5.5             | 0                      | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           |                 | –4                     |                 | –4                     |                 | –4                     |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            |                 | –8                     |                 | –8                     |                 | –8                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            |                 | –12                    |                 | –12                    |                 | –12                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V              |                 | –24                    |                 | –24                    |                 | –24                    |                 |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           |                 | 4                      |                 | 4                      |                 | 4                      |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            |                 | 8                      |                 | 8                      |                 | 8                      |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            |                 | 12                     |                 | 12                     |                 | 12                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V              |                 | 24                     |                 | 24                     |                 | 24                     |                 |      |
| Δt/Δv           | Input transition rise or fall rate | 8                                  |                 | 8                      |                 | 8                      |                 | 8                      |                 | ns/V |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

**7.5 Thermal Information**

| THERMAL METRIC <sup>(1)</sup> |  | SN74LVC08A |           |          |            |            | UNIT |
|-------------------------------|--|------------|-----------|----------|------------|------------|------|
|                               |  | D (SOIC)   | DB (SSOP) | NS (SOP) | PW (TSSOP) | RGY (LCCC) |      |
|                               |  | 14 PINS    | 14 PINS   | 14 PINS  | 14 PINS    | 14 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 86         | 96        | 76       | 113        | 47         | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.6 Electrical Characteristics for SN54LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS  | V <sub>CC</sub> | SN54LVC08A            |                    |     | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|-----|------|
|                  |  |                 | –55°C to 125°C        |                    |     |      |
|                  |  |                 | MIN                   | TYP <sup>(1)</sup> | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA  | 2.7 V to 3.6 V  | V <sub>CC</sub> – 0.2 |                    |     | V    |
|                  | I <sub>OH</sub> = –12 mA   | 2.7 V           | 2.2                   |                    |     |      |
|                  |  | 3 V             | 2.4                   |                    |     |      |
|                  | I <sub>OH</sub> = –24 mA   | 3 V             | 2.2                   |                    |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA   | 2.7 V to 3.6 V  | 0.2                   |                    |     | V    |
|                  | I <sub>OL</sub> = 12 mA  | 2.7 V           | 0.4                   |                    |     |      |
|                  |  | 3 V             | 0.55                  |                    |     |      |
|                  | I <sub>OL</sub> = 24 mA  | 3 V             | 0.55                  |                    |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND  | 3.6 V           | ±5                    |                    |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 10                    |                    |     | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |                    |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 5                     |                    |     | pF   |

(1) T<sub>A</sub> = 25°C

## 7.7 Electrical Characteristics for SN74LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS  | V <sub>CC</sub> | SN74LVC08A            |     |     |                       |     |                       | UNIT |     |
|------------------|--|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|------|-----|
|                  |  |                 | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C         |     | –40°C to 125°C        |      |     |
|                  |  |                 | MIN                   | TYP | MAX | MIN                   | MAX | MIN                   |      | MAX |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |     |     | V <sub>CC</sub> – 0.2 |     | V <sub>CC</sub> – 0.3 |      | V   |
|                  | I <sub>OH</sub> = –4 mA  | 1.65 V          | 1.29                  |     |     | 1.2                   |     | 1.05                  |      |     |
|                  |  | 2.3 V           | 1.9                   |     |     | 1.7                   |     | 1.55                  |      |     |
|                  | I <sub>OH</sub> = –12 mA   | 2.7 V           | 2.2                   |     |     | 2.2                   |     | 2.05                  |      |     |
|                  |  | 3 V             | 2.4                   |     |     | 2.4                   |     | 2.25                  |      |     |
|                  | I <sub>OH</sub> = –24 mA   | 3 V             | 2.3                   |     |     | 2.2                   |     | 2                     |      |     |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V | 0.1                   |     |     | 0.2                   |     | 0.3                   |      | V   |
|                  | I <sub>OL</sub> = 4 mA   | 1.65 V          | 0.24                  |     |     | 0.45                  |     | 0.6                   |      |     |
|                  |  | 2.3 V           | 0.3                   |     |     | 0.7                   |     | 0.75                  |      |     |
|                  | I <sub>OL</sub> = 12 mA  | 2.7 V           | 0.4                   |     |     | 0.4                   |     | 0.6                   |      |     |
|                  |  | 3 V             | 0.55                  |     |     | 0.55                  |     | 0.8                   |      |     |
|                  | I <sub>OL</sub> = 24 mA  | 3 V             | 0.55                  |     |     | 0.55                  |     | 0.8                   |      |     |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND  | 3.6 V           | ±1                    |     |     | ±5                    |     | ±20                   |      | μA  |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 1                     |     |     | 10                    |     | 40                    |      | μA  |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |     |     | 500                   |     | 5000                  |      | μA  |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 5                     |     |     |                       |     |                       |      | pF  |

## 7.8 Switching Characteristics for SN54LVC08A

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> | SN54LVC08A     |     | UNIT |
|-----------------|--------------|-------------|-----------------|----------------|-----|------|
|                 |              |             |                 | –55°C to 125°C |     |      |
|                 |              |             |                 | MIN            | MAX |      |
| t <sub>pd</sub> | A or B       | Y           | 2.7 V           | 4.8            |     | ns   |
|                 |              |             | 3.3 V ± 0.3 V   | 1              | 4.1 |      |

### 7.9 Switching Characteristics for SN74LVC08A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

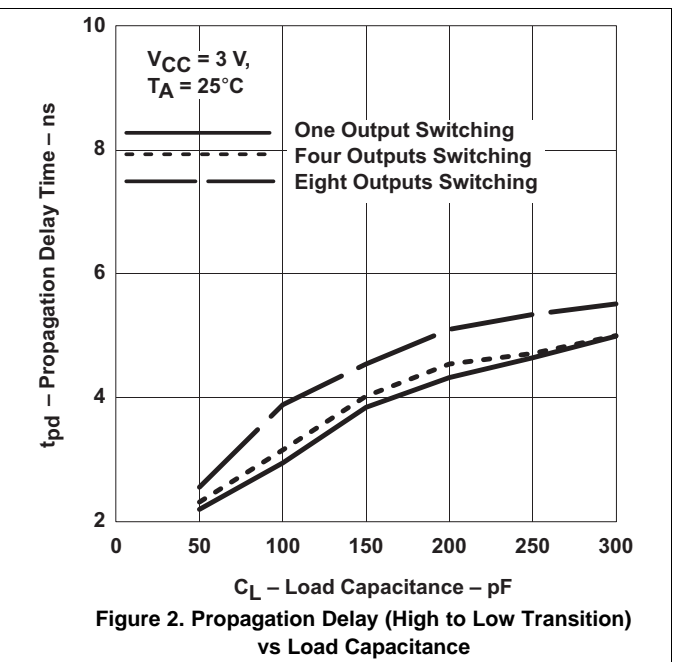
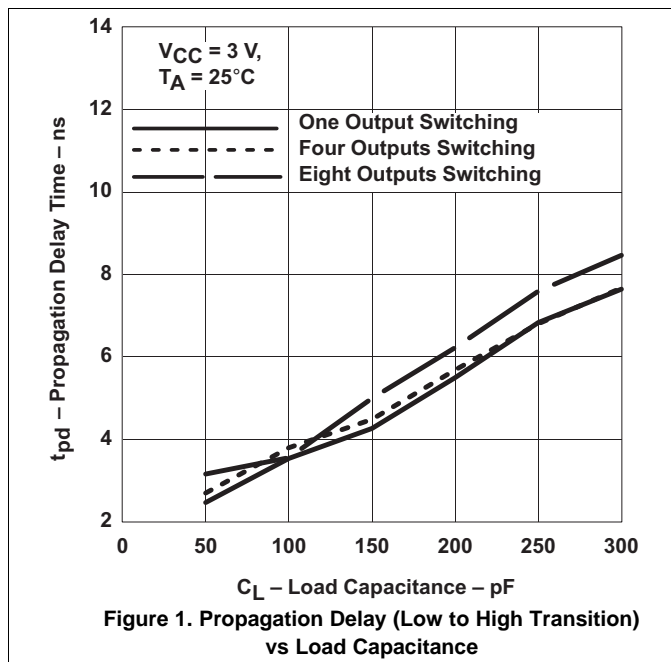
| PARAMETER          | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> | SN74LVC08A            |     |     |               |     |                | UNIT |     |
|--------------------|--------------|-------------|-----------------|-----------------------|-----|-----|---------------|-----|----------------|------|-----|
|                    |              |             |                 | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C |     | –40°C to 125°C |      |     |
|                    |              |             |                 | MIN                   | TYP | MAX | MIN           | MAX | MIN            |      | MAX |
| t <sub>pd</sub>    | A or B       | Y           | 1.8 V ± 0.15 V  | 1                     | 5   | 9.3 | 1             | 9.8 | 1              | 11.3 | ns  |
|                    |              |             | 2.5 V ± 0.2 V   | 1                     | 2.9 | 6.4 | 1             | 6.9 | 1              | 9    |     |
|                    |              |             | 2.7 V           | 1                     | 3   | 4.6 | 1             | 4.8 | 1              | 6    |     |
|                    |              |             | 3.3 V ± 0.3 V   | 1                     | 2.6 | 3.9 | 1             | 4.1 | 1              | 5.5  |     |
| t <sub>sk(o)</sub> |              |             | 3.3 V ± 0.3 V   |                       |     |     |               | 1   |                | 1.5  | ns  |

### 7.10 Operating Characteristics

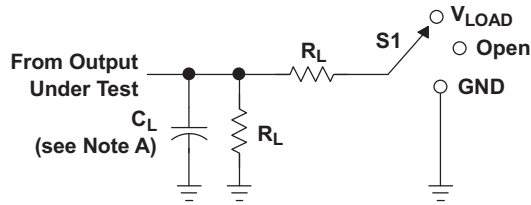
T<sub>A</sub> = 25°C

| PARAMETER       |  | TEST CONDITIONS | V <sub>CC</sub> | TYP | UNIT |
|-----------------|--|-----------------|-----------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance per gate | f = 10 MHz      | 1.8 V           | 7   | pF   |
|                 |  |                 | 2.5 V           | 9.8 |      |
|                 |  |                 | 3.3 V           | 10  |      |

### 7.11 Typical Characteristics



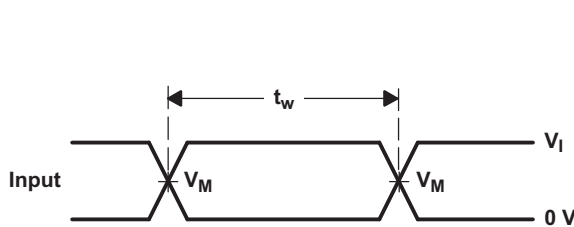
## 8 Parameter Measurement Information



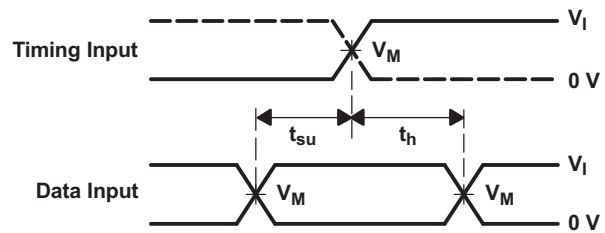
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

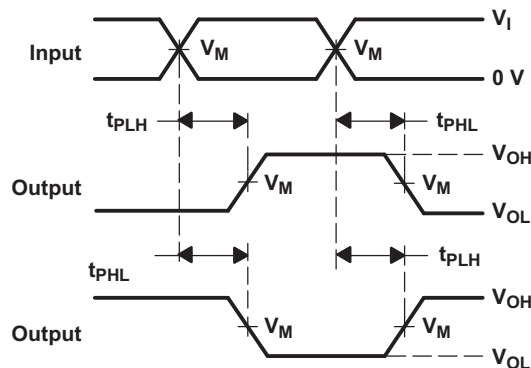
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_D$  |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |        |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V  |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V  |



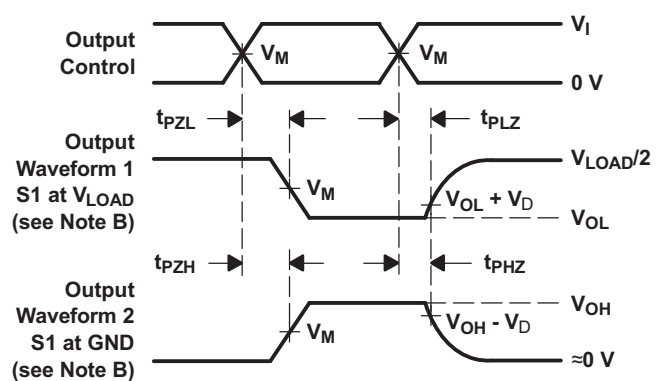
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

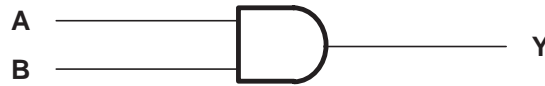
Figure 3. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SN74LVC08 device contains quadruple 2-input positive AND gate device and performs the Boolean function  $Y = A \cdot B$ . This device is useful when multiple AND function is used in the system.

### 9.2 Functional Block Diagram



**Figure 4. Logic Diagram, Each Gate (Positive Logic)**

### 9.3 Feature Description

The device can operate from 1.65 V to 3.6 V, allowing to be used in low voltage systems.

The device can accept voltages to 5.5 V make this device flexible to connect and work seamlessly with wide voltage range systems.

The maximum  $t_{pd}$  of 4.1 ns at 3.3 V is beneficial for use in high speed applications.

The device has a  $I_{off}$  support live insertion, a partial-power-down mode, and a back-drive protection.

### 9.4 Device Functional Modes

[Table 1](#) lists the functional modes for the SN54LVC08A and SN74LVC08A devices.

**Table 1. Truth Table**

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | H      |
| L      | X | L      |
| X      | L | L      |

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74LVC08A is used to drive CMOS device and used for implementing AND logic. LVC family can support current drive of about 24 mA at 3-V  $V_{CC}$ . The inputs for SN74LVC08 are 5.5-V tolerant allowing it to translate down to  $V_{CC}$ .

### 10.2 Typical Application

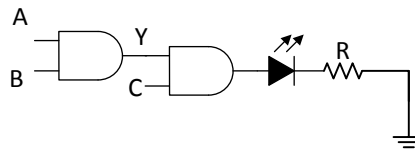


Figure 5. Three Input AND Gate Implementation and Driving LED

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

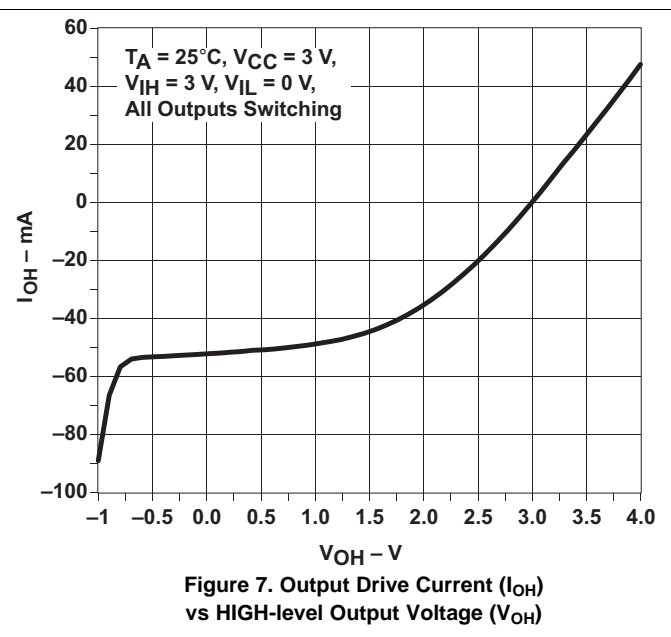
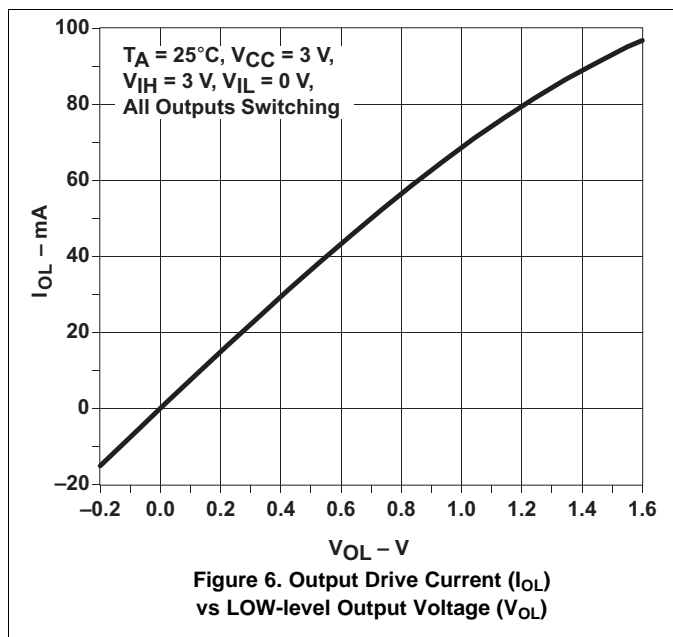
SN74LVC08A contains four AND gates in one package which can be used for individual AND function or to implement complex Boolean logic. Figure 5 shows an example of implementing 3input AND function. AB are inputs for AND gate which are connected to another AND gate.  $Z = A \cdot B \cdot C$ . SN74LVC08A support high drive current of 24 mA which can be used to drive LED's of even Drive low current signal FETs, an example is shown in Figure 5 TI recommends to use a series resistance to limit the current. If  $V_{CC}$  is 3 V, and LED current should be 10 mA, and the forward-voltage of LED is 2.5 V, then R as shown in Figure 5 is calculated using Equation 1 below:

$$R = (V_{CC} - V_{LED}) / I \quad (1)$$

$$R = (3 - 2.5) / 0.01 = 50 \Omega$$

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient.

### 12.2 Layout Examples

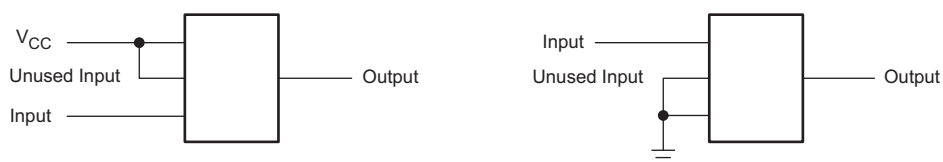


Figure 8. Layout Examples

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC08A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74LVC08A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)              | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-9753401Q2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-9753401Q2A<br>SNJ54LVC<br>08AFK | <a href="#">Samples</a> |
| 5962-9753401QCA  | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9753401QC<br>A<br>SNJ54LVC08AJ  | <a href="#">Samples</a> |
| 5962-9753401QDA  | ACTIVE        | CFP          | W               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9753401QD<br>A<br>SNJ54LVC08AW  | <a href="#">Samples</a> |
| SN74LVC08AD      | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADBR    | ACTIVE        | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                                | <a href="#">Samples</a> |
| SN74LVC08ADBRE4  | ACTIVE        | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                                | <a href="#">Samples</a> |
| SN74LVC08ADBRG4  | ACTIVE        | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                                | <a href="#">Samples</a> |
| SN74LVC08ADE4    | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADG4    | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADR     | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADRE4   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADRG3   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADRG4   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ADT     | ACTIVE        | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |
| SN74LVC08ANSR    | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                               | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)             | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74LVC08ANSRE4  | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC08A                              | <a href="#">Samples</a> |
| SN74LVC08APW     | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWG4   | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWR    | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWRE4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWRG3  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWRG4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWT    | ACTIVE        | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08APWTG4  | ACTIVE        | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08ARGYR   | ACTIVE        | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SN74LVC08ARGYRG4 | ACTIVE        | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | LC08A                               | <a href="#">Samples</a> |
| SNJ54LVC08AFK    | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-9753401Q2A<br>SNJ54LVC08AFK    | <a href="#">Samples</a> |
| SNJ54LVC08AJ     | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9753401QC<br>A<br>SNJ54LVC08AJ | <a href="#">Samples</a> |
| SNJ54LVC08AW     | ACTIVE        | CFP          | W               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9753401QD<br>A<br>SNJ54LVC08AW | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

---

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LVC08A, SN74LVC08A :**

- Catalog: [SN74LVC08A](#)
  
- Automotive: [SN74LVC08A-Q1](#), [SN74LVC08A-Q1](#)
  
- Enhanced Product: [SN74LVC08A-EP](#), [SN74LVC08A-EP](#)
  
- Military: [SN54LVC08A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADRG3  | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADRG4  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADRG4  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ADT    | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC08ANSR   | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC08APWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC08APWRG3 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC08APWRG4 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC08APWT   | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC08ARGYR  | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LVC08ADR    | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC08ADRG3  | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC08ADRG4  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74LVC08ADRG4  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74LVC08ADT    | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| SN74LVC08ANSR   | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC08APWR   | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC08APWRG3 | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC08APWRG4 | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC08APWT   | TSSOP        | PW              | 14   | 250  | 367.0       | 367.0      | 35.0        |
| SN74LVC08ARGYR  | VQFN         | RGY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |

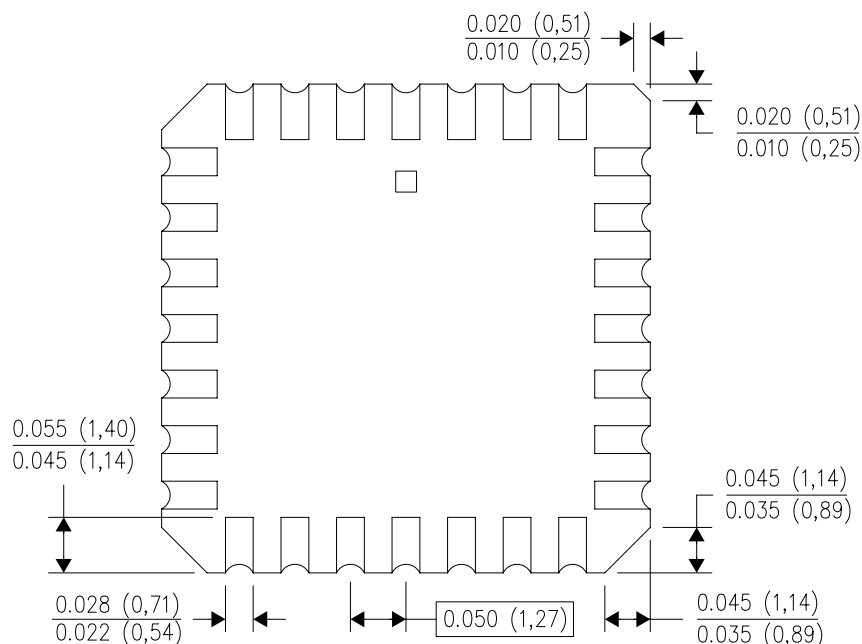
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - $\triangle F$  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

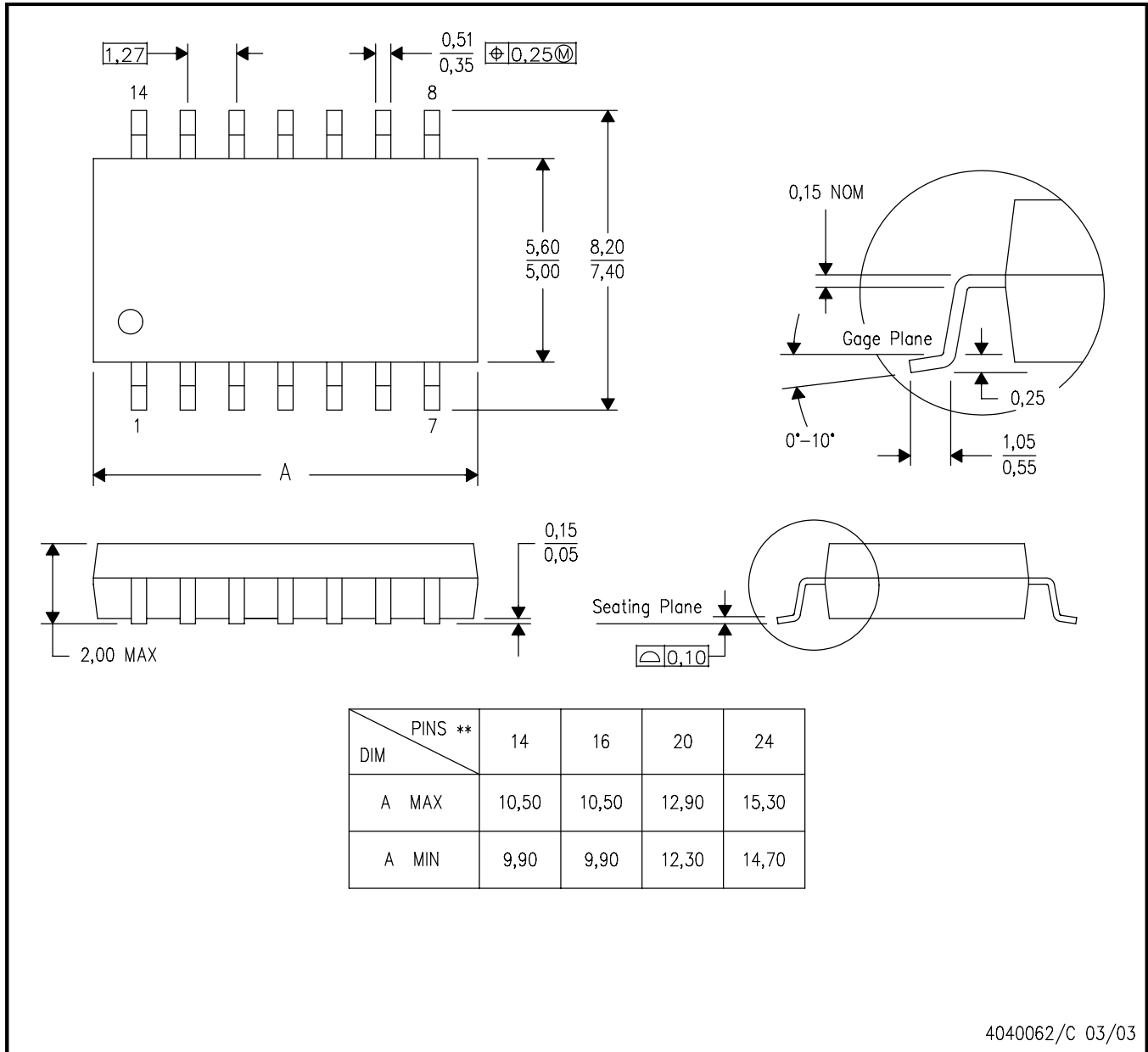
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

# J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

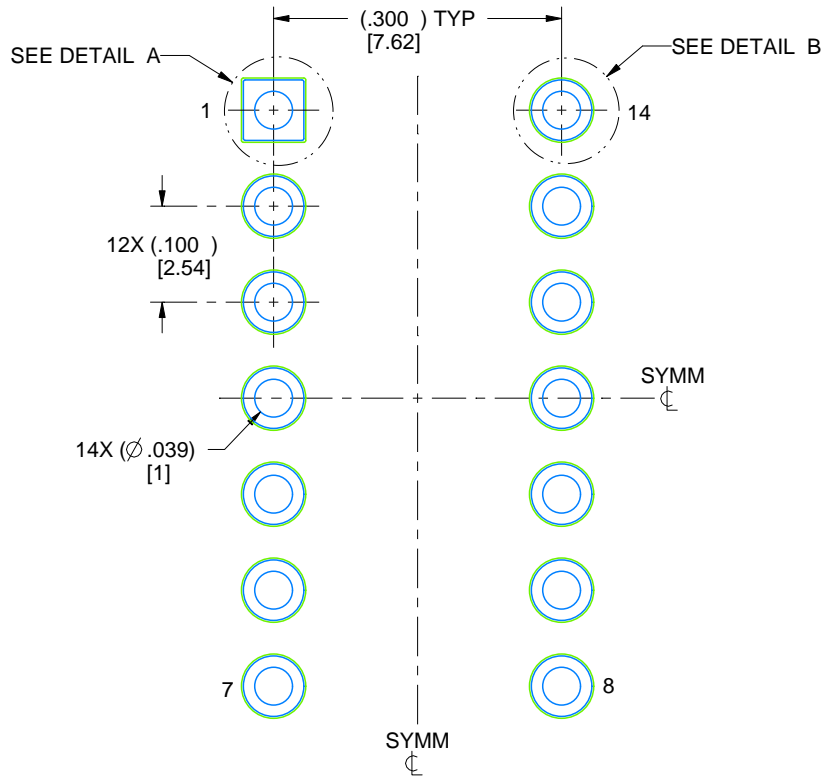
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

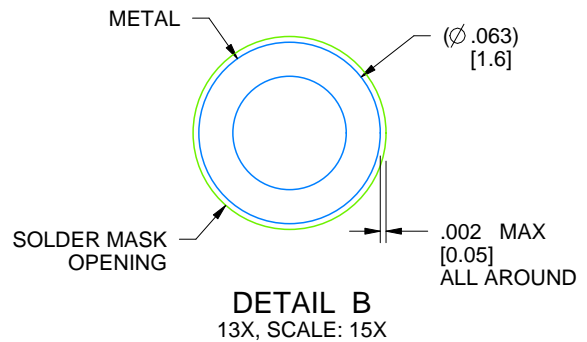
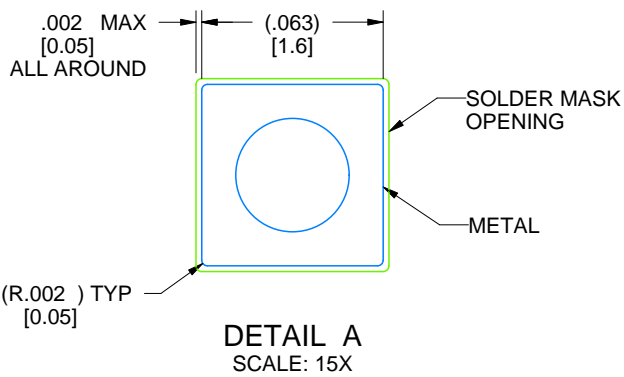
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



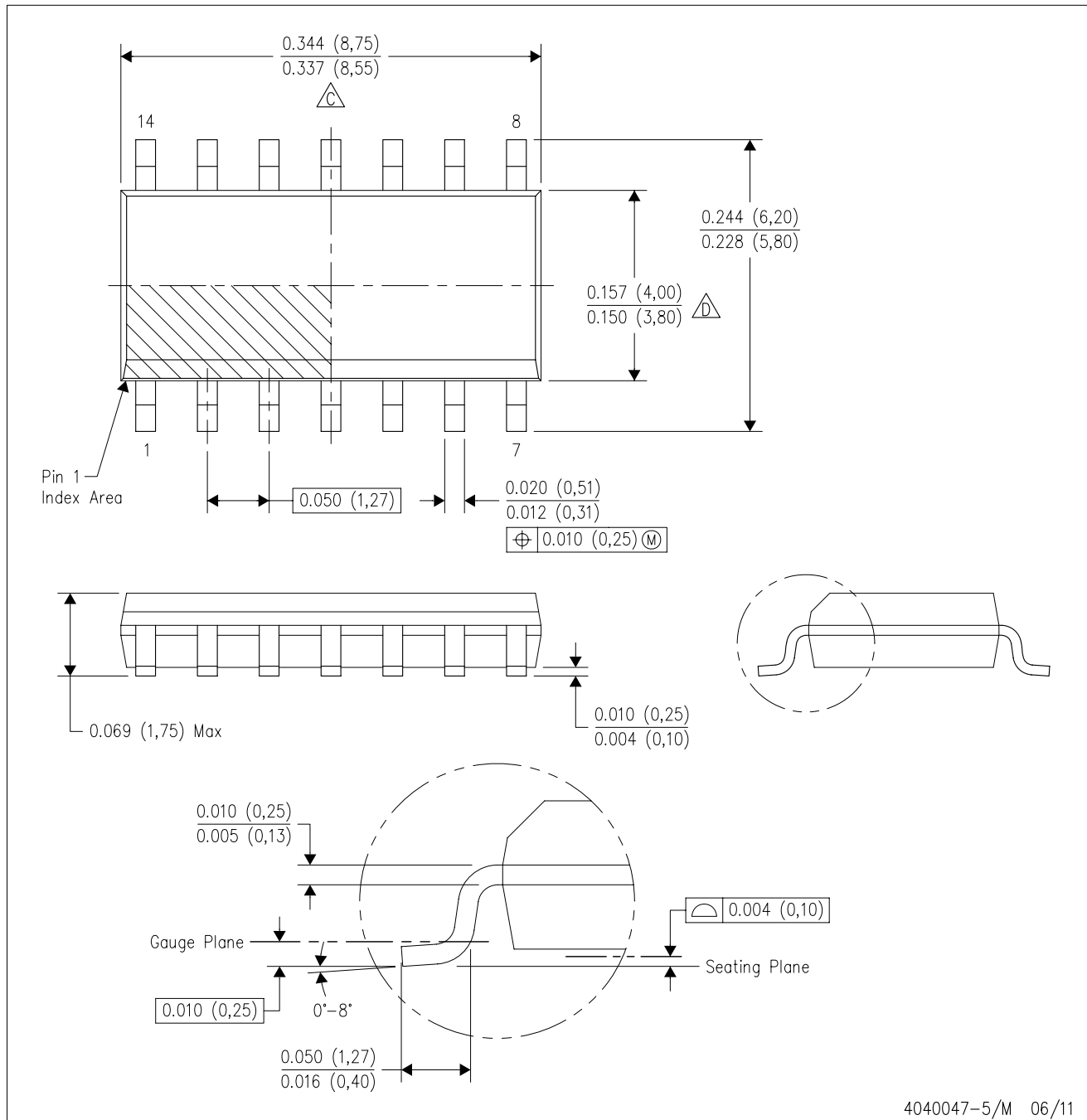
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

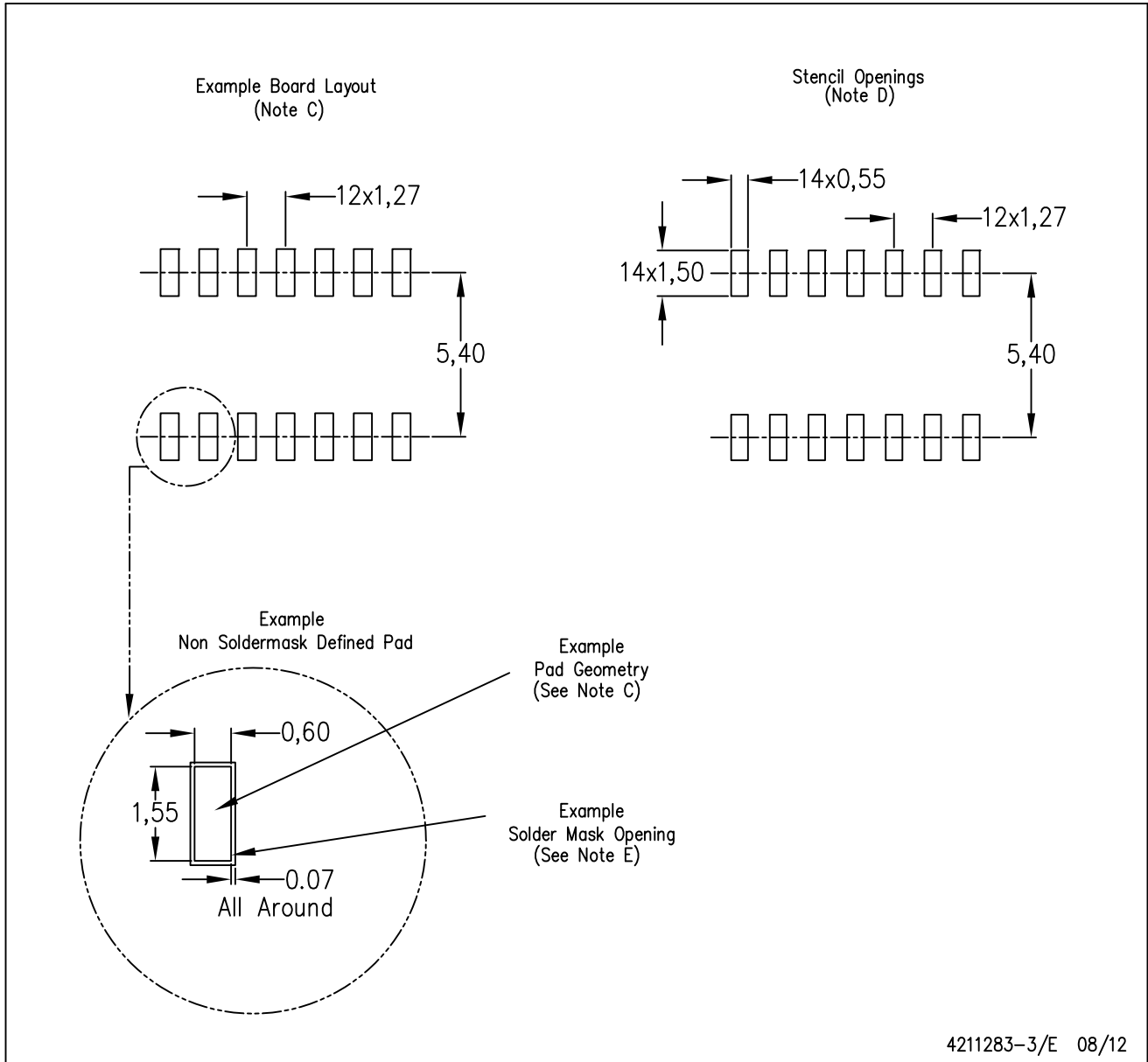
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

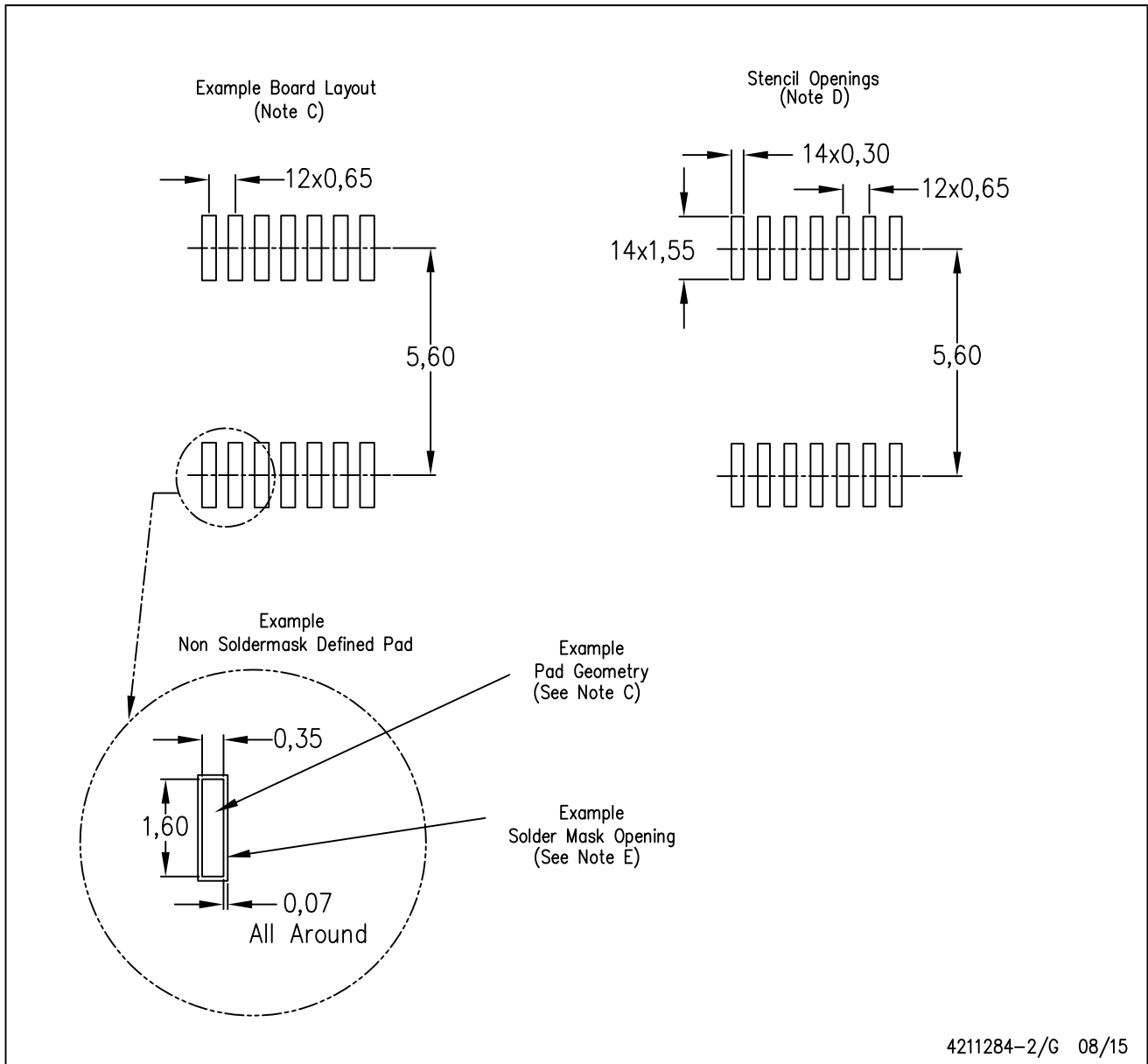


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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