



**THE DATASHEET OF
SN74LS173AN**

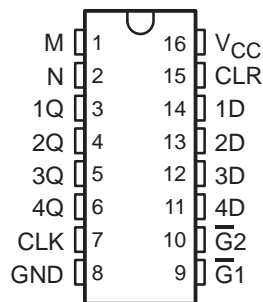


SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

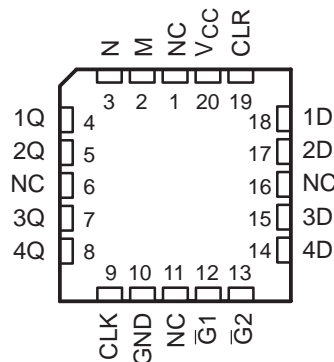
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- 3-State Outputs Interface Directly With System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:
 - Parallel Load
 - Do Nothing (Hold)
- For Application as Bus Buffer Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

SN54173, SN54LS173A . . . J OR W PACKAGE
SN74173 . . . N PACKAGE
SN74LS173A . . . D or N PACKAGE
(TOP VIEW)



SN54LS173A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

| TYPE | TYPICAL PROPAGATION DELAY TIME | MAXIMUM CLOCK FREQUENCY |
|---------|--------------------------------|-------------------------|
| '173 | 23 ns | 35 MHz |
| 'LS173A | 18 ns | 50 MHz |

description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable ($\overline{G1}$, $\overline{G2}$) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

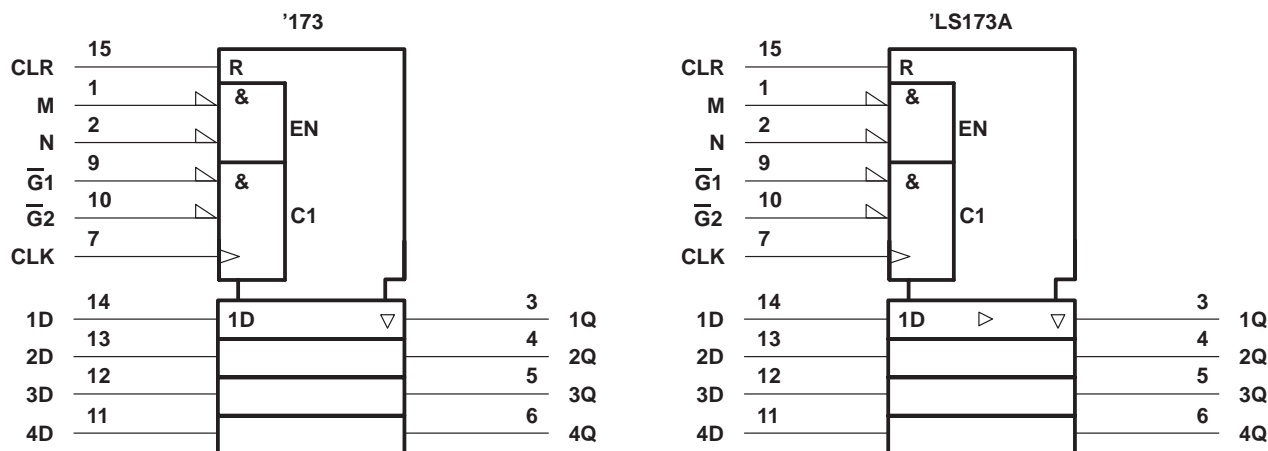
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FUNCTION TABLE

| CLR | CLK | INPUTS | | | OUTPUT Q |
|-----|------------|-----------------|-----------------|--------|----------|
| | | DATA ENABLE | | DATA D | |
| | | $\overline{G1}$ | $\overline{G2}$ | | |
| H | X | X | X | X | L |
| L | L | X | X | X | Q_0 |
| L | \uparrow | H | X | X | Q_0 |
| L | \uparrow | X | H | X | Q_0 |
| L | \uparrow | L | L | L | L |
| L | \uparrow | L | L | H | H |

When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†

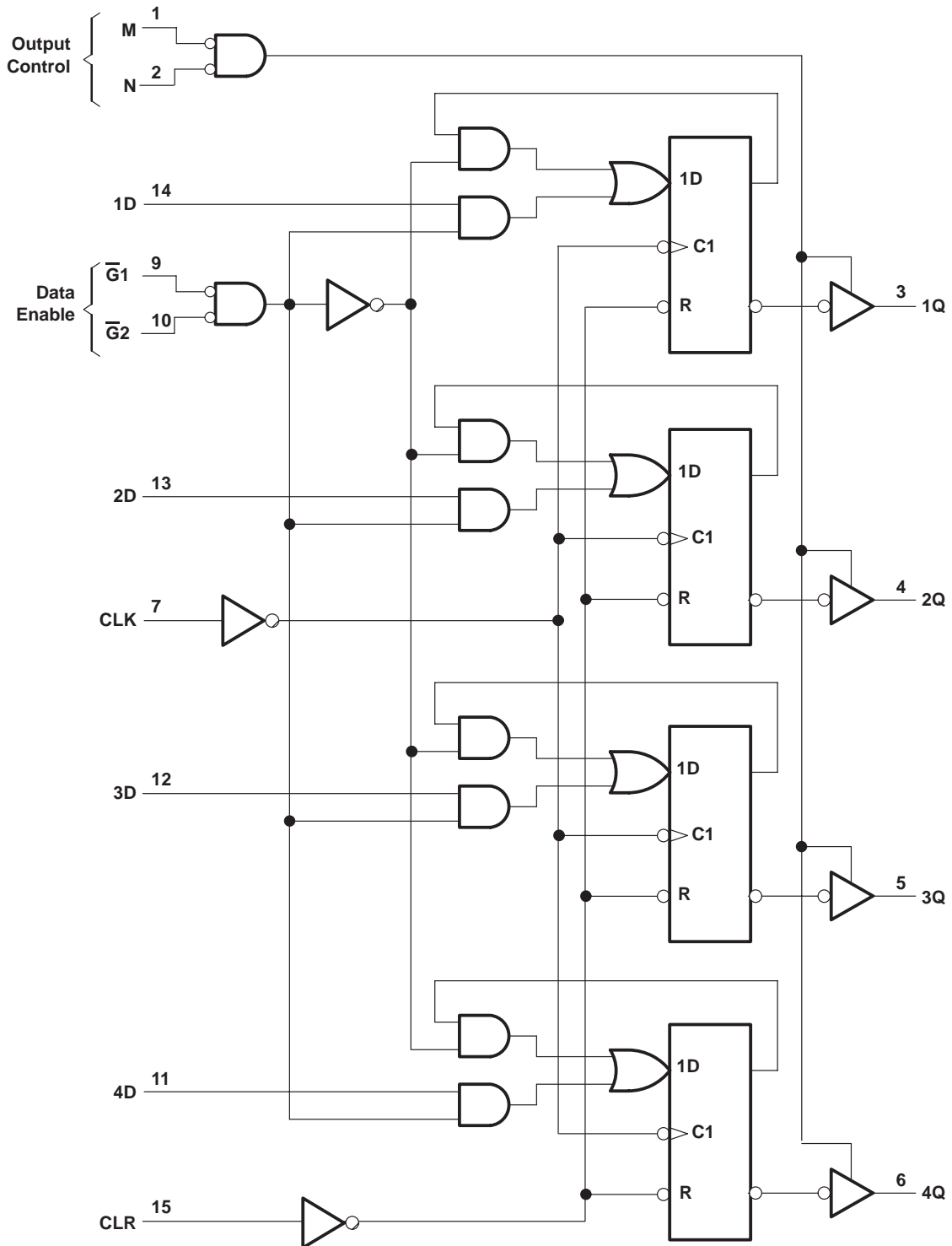


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN54173, SN54LS173A, SN74173, SN74LS173A
**4-BIT D-TYPE REGISTERS
 WITH 3-STATE OUTPUTS**

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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

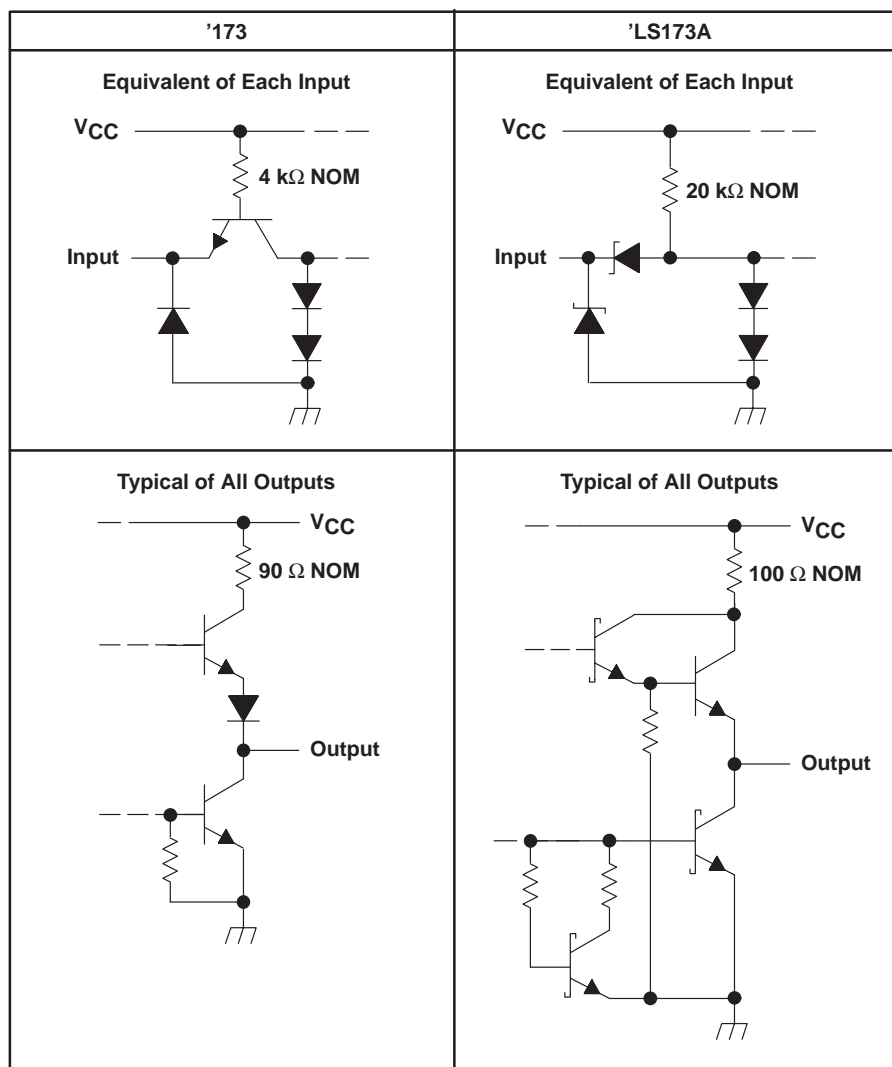
SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|-----------------|
| Supply voltage, V_{CC} (see Note 1) | –0.5 V to 7 V |
| Input voltage: '173 | –0.5 V to 5.5 V |
| 'LS173A | –0.5 V to 7 V |
| Off-state output voltage | –0.5 V to 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 113°C/W |
| N package | 78°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

| | | SN54173 | | | SN74173 | | | UNIT |
|-----------------|--------------------------------|---------|-----|-----|---------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I _{OH} | High-level output current | | | -2 | | | -5.2 | mA |
| I _{OL} | Low-level output current | | | 16 | | | 16 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54173 | | | SN74173 | | | UNIT |
|---------------------|---|--|------|------|---------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -12 mA | | -1.5 | | | -1.5 | V |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = 0.8 V, V _{IH} = 2 V, I _{OH} = MAX | | 2.4 | | | 2.4 | V |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = 0.8 V, V _{IH} = 2 V, I _{OL} = 16 mA | | | | | 0.4 | V |
| I _{O(off)} | Off-state (high-impedance state) output current | V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V | | 150 | | | 40 | μA |
| | | V _O = 0.4 V | | -150 | | | -40 | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 5.5 V | | | | | 1 | mA |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.4 V | | | | | 40 | μA |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | | | | -1.6 | mA |
| I _{OS} | Short-circuit output current§ | V _{CC} = MAX | | -30 | | | -70 | mA |
| I _{CC} | Supply current | V _{CC} = MAX, See Note 4 | | 50 | | | 72 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G1}$, $\overline{G2}$, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

| | | SN54173 | | SN74173 | | UNIT |
|--------------------|-----------------------|---|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{clock} | Input clock frequency | | 25 | | 25 | MHz |
| t _w | Pulse duration | CLK or CLR | | 20 | 20 | ns |
| t _{su} | Setup time | Data enable ($\overline{G1}$, $\overline{G2}$) | | 17 | 17 | ns |
| | | Data | | 10 | 10 | |
| | | CLR (inactive state) | | 10 | 10 | |
| t _h | Hold time | Data enable ($\overline{G1}$, $\overline{G2}$) | | 2 | 2 | ns |
| | | Data | | 10 | 10 | |



SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 400\ \Omega$ (see Figure 1)

| PARAMETER | TEST CONDITIONS | SN54173 | | | SN74173 | | | UNIT |
|-----------|---|---------|-----|-----|---------|-----|-----|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | Maximum clock frequency | 25 | 35 | | 25 | 35 | | MHz |
| t_{PHL} | Propagation delay time, high-to-low-level output from clear input | | 18 | 27 | | 18 | 27 | ns |
| t_{PLH} | Propagation delay time, low-to-high-level output from clock input | | 28 | 43 | | 28 | 43 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output from clock input | | 19 | 31 | | 19 | 31 | |
| t_{PZH} | Output enable time to high level | 7 | 16 | 30 | 7 | 16 | 30 | ns |
| t_{PZL} | Output enable time to low level | 7 | 21 | 30 | 7 | 21 | 30 | |
| t_{PHZ} | Output disable time from high level | 3 | 5 | 14 | 3 | 5 | 14 | ns |
| t_{PLZ} | Output disable time from low level | 3 | 11 | 20 | 3 | 11 | 20 | |



SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

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recommended operating conditions

| | | SN54LS173A | | | SN74LS173A | | | UNIT |
|-----------------|--------------------------------|------------|-----|-----|------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I _{OH} | High-level output current | | | -1 | | | -2.6 | mA |
| I _{OL} | Low-level output current | | | 12 | | | 24 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS173A | | | SN74LS173A | | | UNIT | |
|---------------------|---|--|------|----------|------------|----------|----------|------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | UNIT | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | |
| V _{IL} | Low-level input voltage | 0.7 | | | 0.8 | | | V | |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -18 mA | | | -1.5 | | | V | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = MAX | | | 2.4 3.4 | | | V | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 12 mA | | 0.25 0.4 | | 0.25 0.4 | | V | |
| | | I _{OL} = 24 mA | | | | 0.35 0.5 | | V | |
| I _{O(off)} | Off-state (high-impedance state) output current | V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V | | 20 | | 20 | | V | |
| | | V _O = 0.4 V | | -20 | | -20 | | | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7 V | | | 0.1 | | | mA | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7 V | | | 20 | | | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | | -0.4 | | | mA | |
| I _{OS} | Short-circuit output current§ | V _{CC} = MAX | | | -30 -130 | | -30 -130 | | mA |
| I _{CC} | Supply current | V _{CC} = MAX, See Note 4 | | | 19 30 | | 19 24 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G1}$, $\overline{G2}$, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

| | | SN54LS173A | | SN74LS173A | | UNIT |
|--------------------|-----------------------|---|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{clock} | Input clock frequency | 30 | | 25 | | MHz |
| t _w | Pulse duration | CLK or CLR | | 25 | | ns |
| t _{su} | Setup time | Data enable ($\overline{G1}$, $\overline{G2}$) | | 35 | | ns |
| | | Data | | 17 | | |
| | | CLR (inactive state) | | 10 | | |
| t _h | Hold time | Data enable ($\overline{G1}$, $\overline{G2}$) | | 0 | | ns |
| | | Data | | 3 | | |



SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

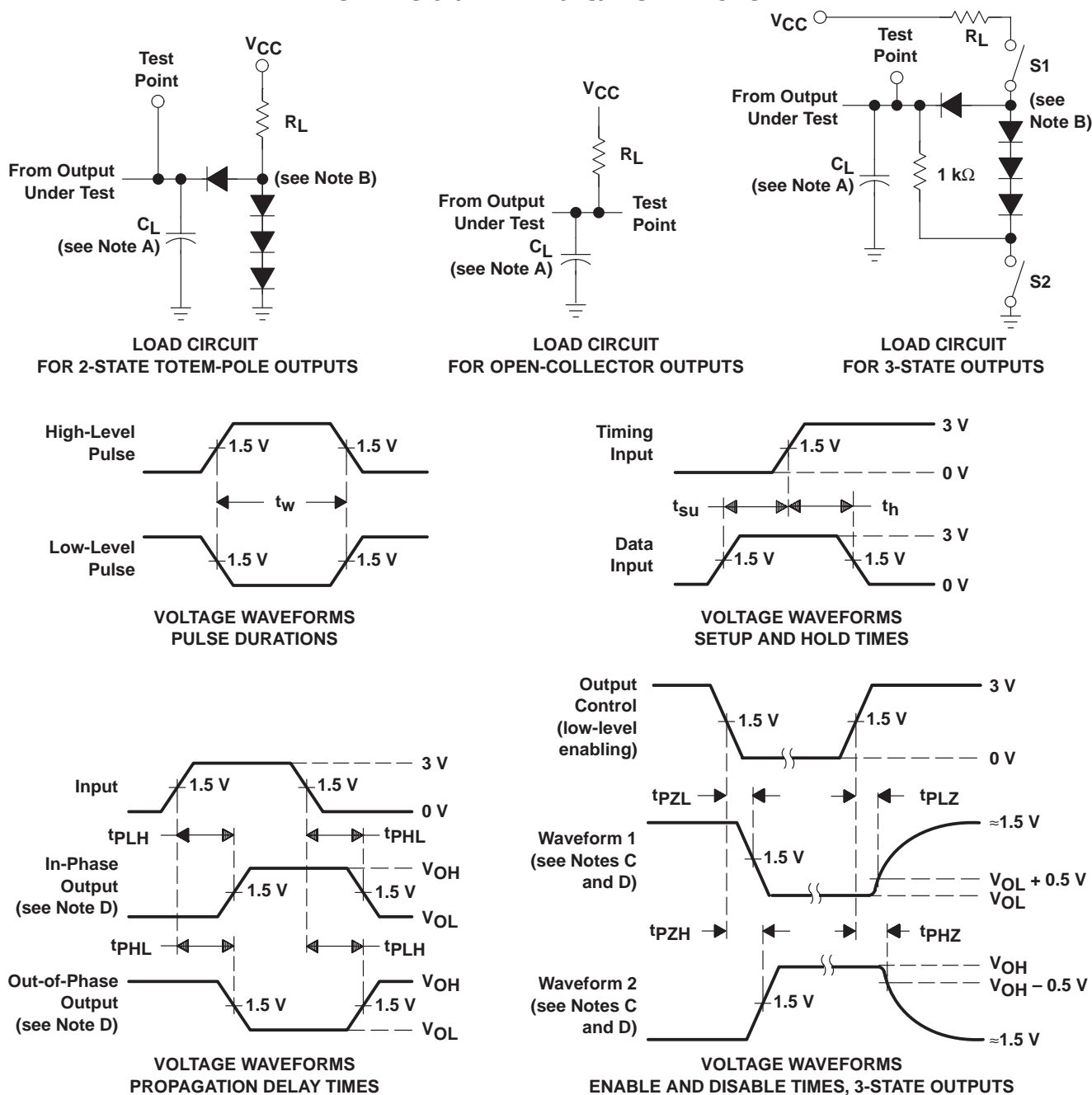
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 667\ \Omega$ (see Figure 2)

| PARAMETER | TEST CONDITIONS | SN54LS173A | | | SN74LS173A | | | UNIT |
|-----------|---|------------|-----|-----|------------|-----|-----|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | Maximum clock frequency | 30 | 50 | | 30 | 50 | | MHz |
| t_{PHL} | Propagation delay time, high-to-low-level output from clear input | | 26 | 35 | | 26 | 35 | ns |
| t_{PLH} | Propagation delay time, low-to-high-level output from clock input | | 17 | 25 | | 17 | 25 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output from clock input | | 22 | 30 | | 22 | 30 | |
| t_{PZH} | Output enable time to high level | | 15 | 23 | | 15 | 23 | ns |
| t_{PZL} | Output enable time to low level | | 18 | 27 | | 18 | 27 | |
| t_{PHZ} | Output disable time from high level | | 11 | 20 | | 11 | 20 | ns |
| t_{PLZ} | Output disable time from low level | | 11 | 17 | | 11 | 17 | |



PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



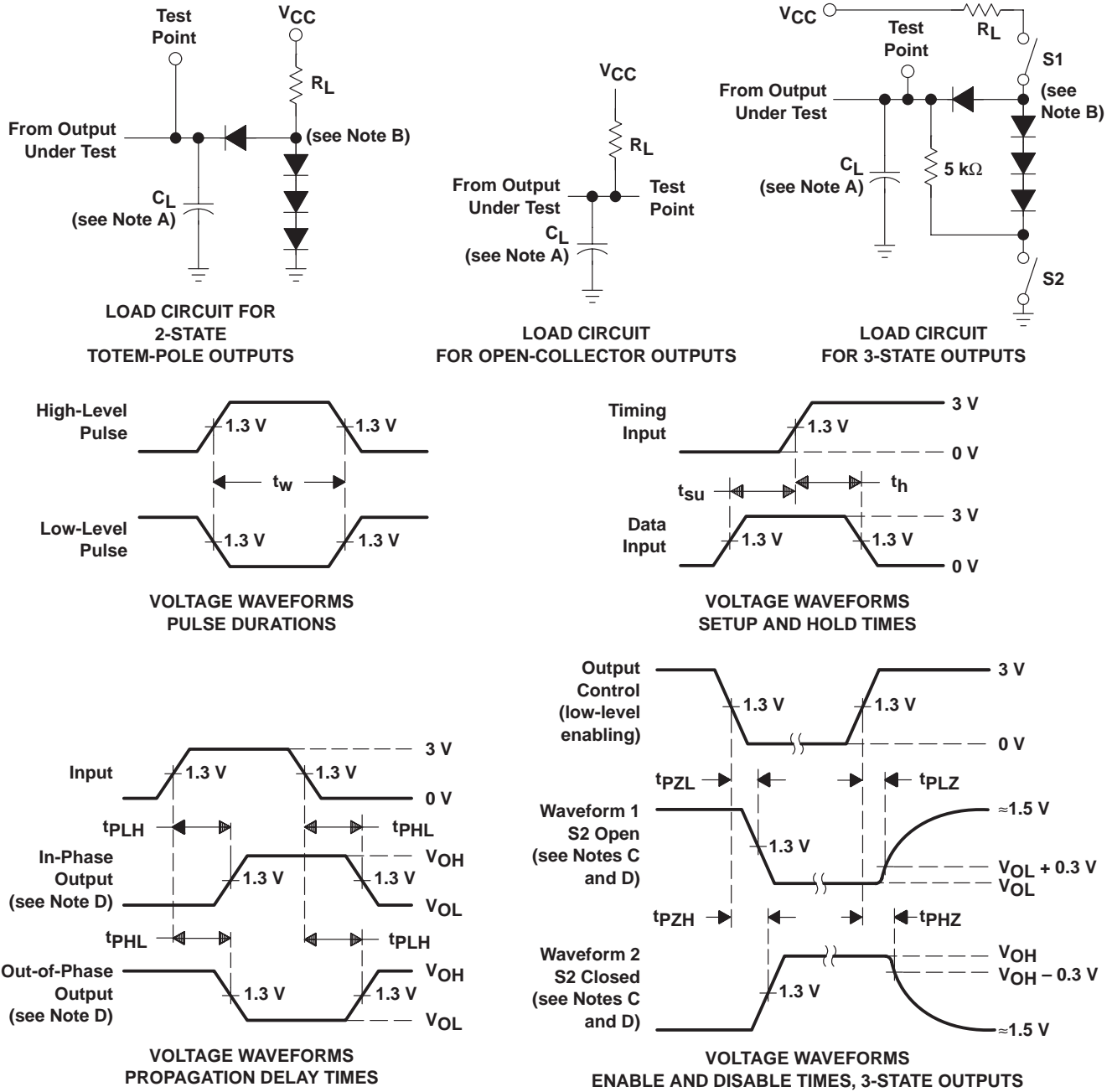
- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/36101BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 36101BEA | Samples |
| JM38510/36101BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 36101BFA | Samples |
| M38510/36101BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 36101BEA | Samples |
| M38510/36101BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 36101BFA | Samples |
| SN54173J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54173J | Samples |
| SN54LS173AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS173AJ | Samples |
| SN74LS173AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS173A | Samples |
| SN74LS173AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS173AN | Samples |
| SNJ54173J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54173J | Samples |
| SNJ54LS173AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 173AFK | Samples |
| SNJ54LS173AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS173AJ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS173A, SN74LS173A :

- Catalog: [SN74LS173A](#)
- Military: [SN54LS173A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

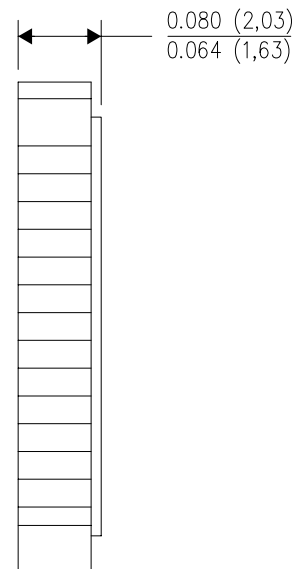
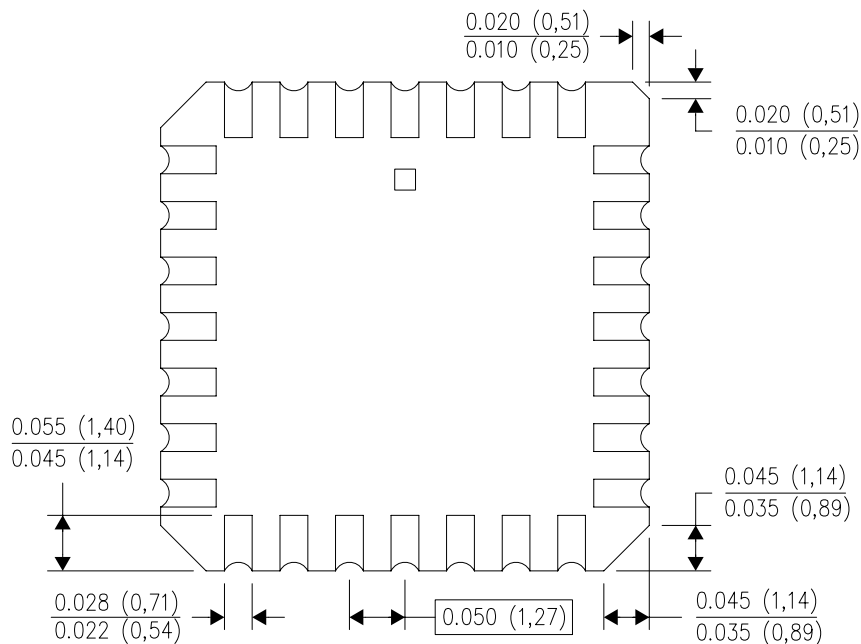
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

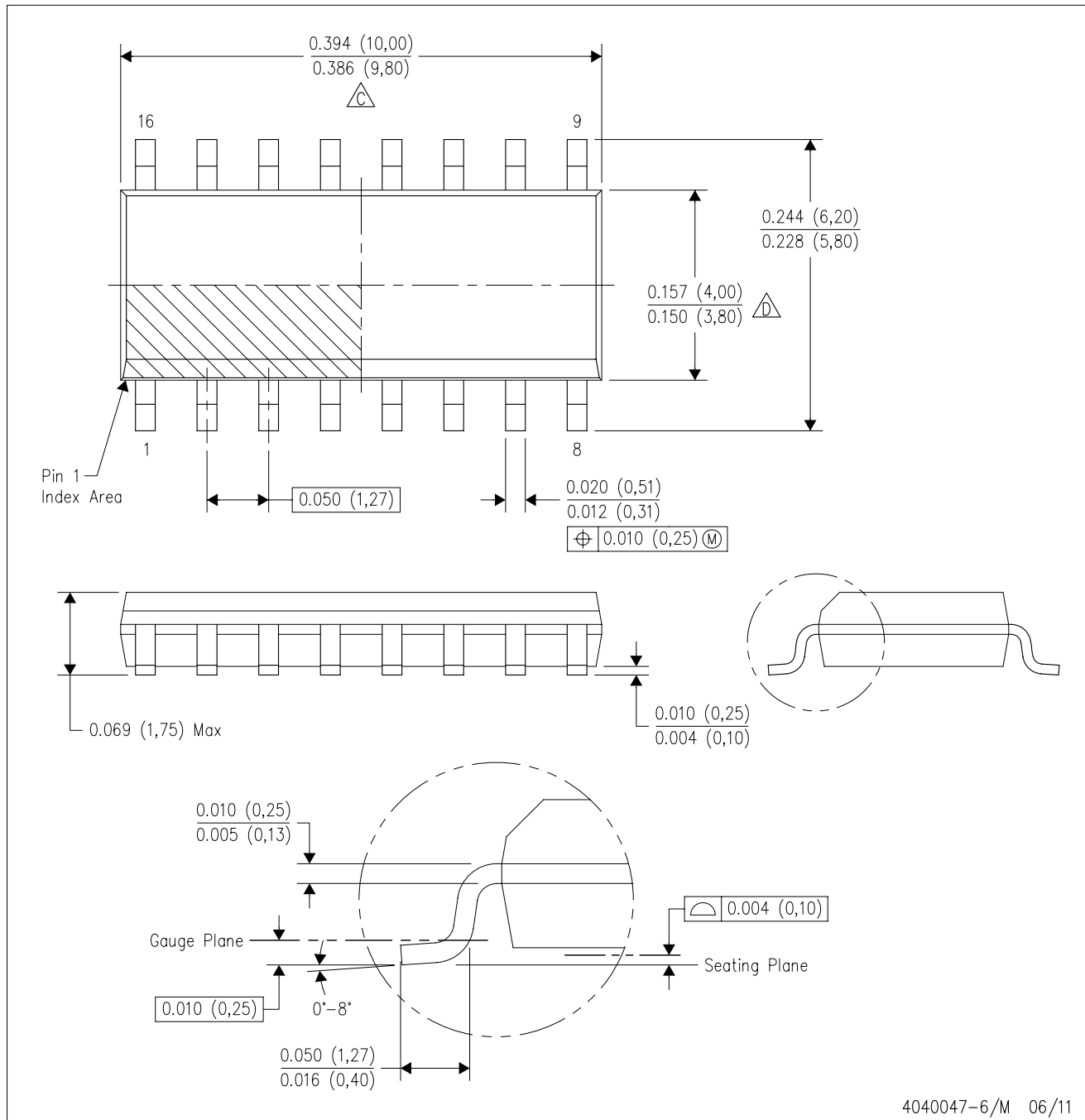


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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