



**THE DATASHEET OF
74HC4020PW,118**



74HC4020; 74HCT4020

14-stage binary ripple counter

Rev. 6 — 3 February 2016

Product data sheet

1. General description

The 74HT4020; 74HCT4020 is a 14-stage binary ripple counter with a clock input (CP), an overriding asynchronous master reset input (MR) and 12 buffered parallel outputs (Q0, and Q3 to Q13). The counter advances on the HIGH-to-LOW transition of CP. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP. Each counter stage is a static toggle flip-flop. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - ◆ For 74HC4020: CMOS level
 - ◆ For 74HCT4020: TTL level
- Multiple package options
- Complies with JEDEC standard no. 7A
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|--------|---|----------|
| | Temperature range | Name | Description | Version |
| 74HC4020D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT4020D | | | | |
| 74HC4020DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT4020DB | | | | |

Table 1. Ordering information ...continued

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC4020PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT4020PW | | | | |
| 74HC4020BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT4020BQ | | | | |

5. Functional diagram

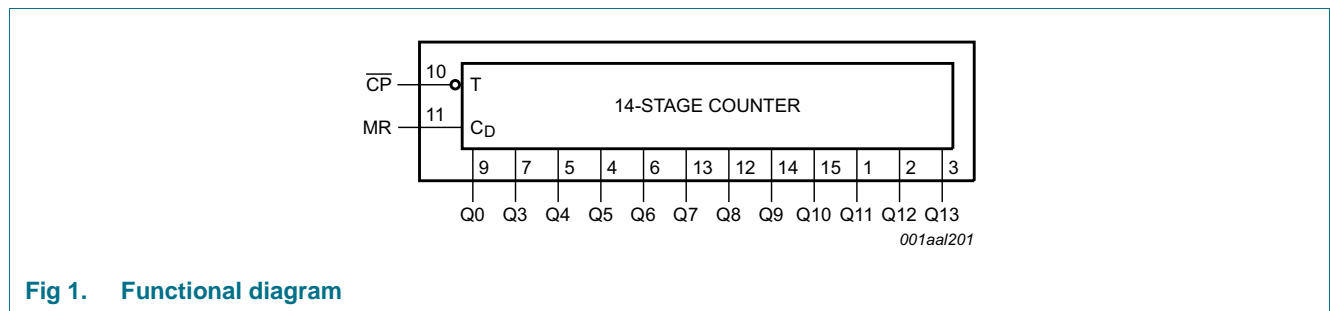


Fig 1. Functional diagram

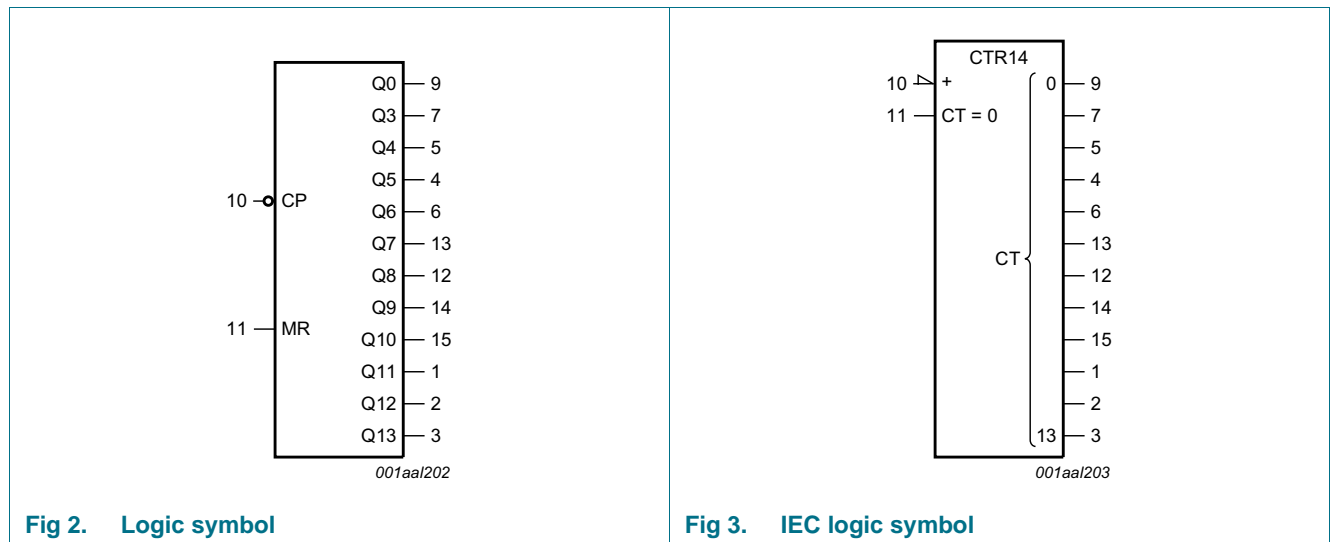


Fig 2. Logic symbol

Fig 3. IEC logic symbol

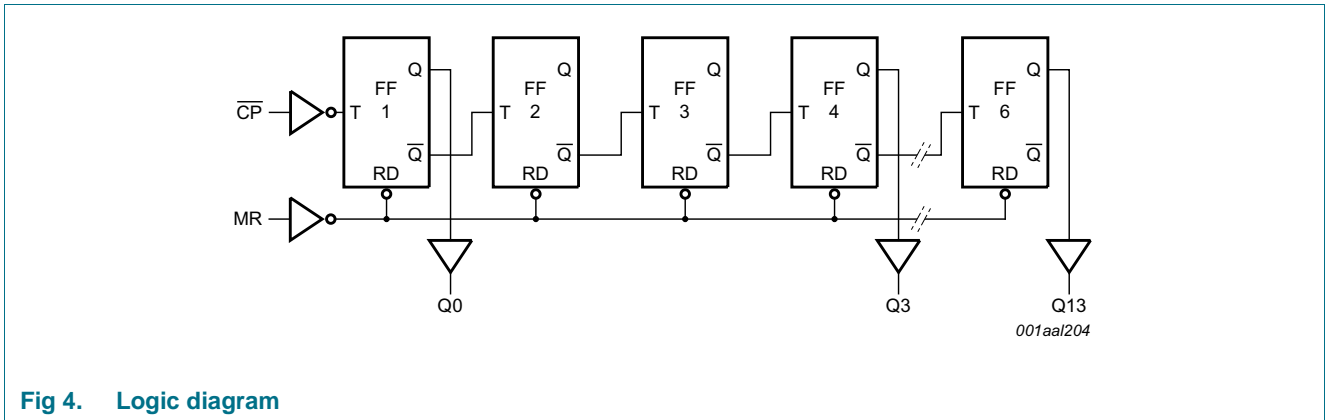


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

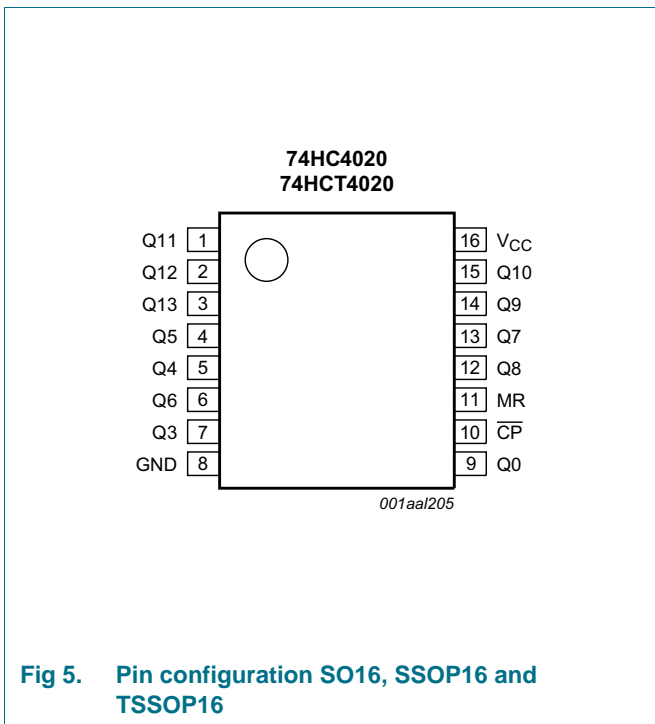


Fig 5. Pin configuration SO16, SSOP16 and TSSOP16

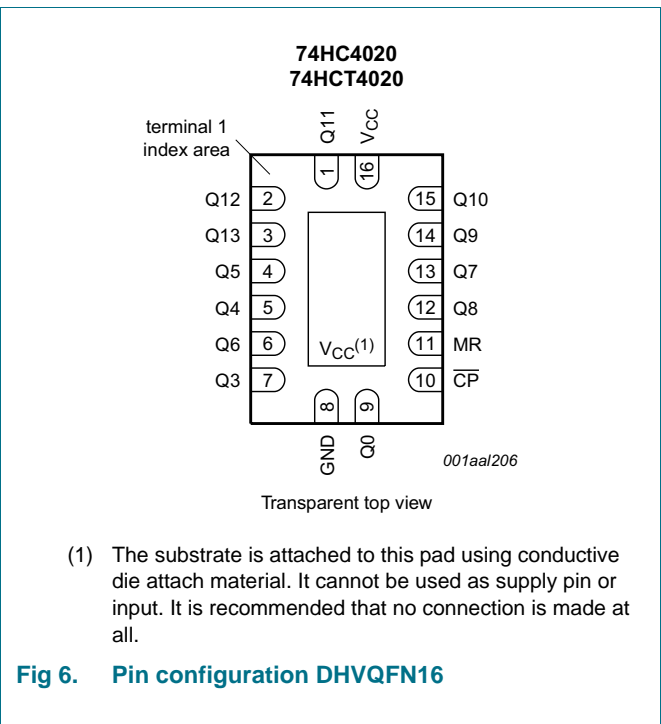


Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--|---|
| Q0, Q3 to Q13 | 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3 | output |
| GND | 8 | ground (0 V) |
| CP | 10 | clock input (HIGH-to-LOW, edge-triggered) |
| MR | 11 | master reset input (active HIGH) |
| V _{CC} | 16 | positive supply voltage |

7. Functional description

Table 3. Function table

| Input | | Output |
|-------|----|---------------|
| CP | MR | Q0, Q3 to Q13 |
| ↑ | L | no change |
| ↓ | L | count |
| X | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

7.1 Timing diagram

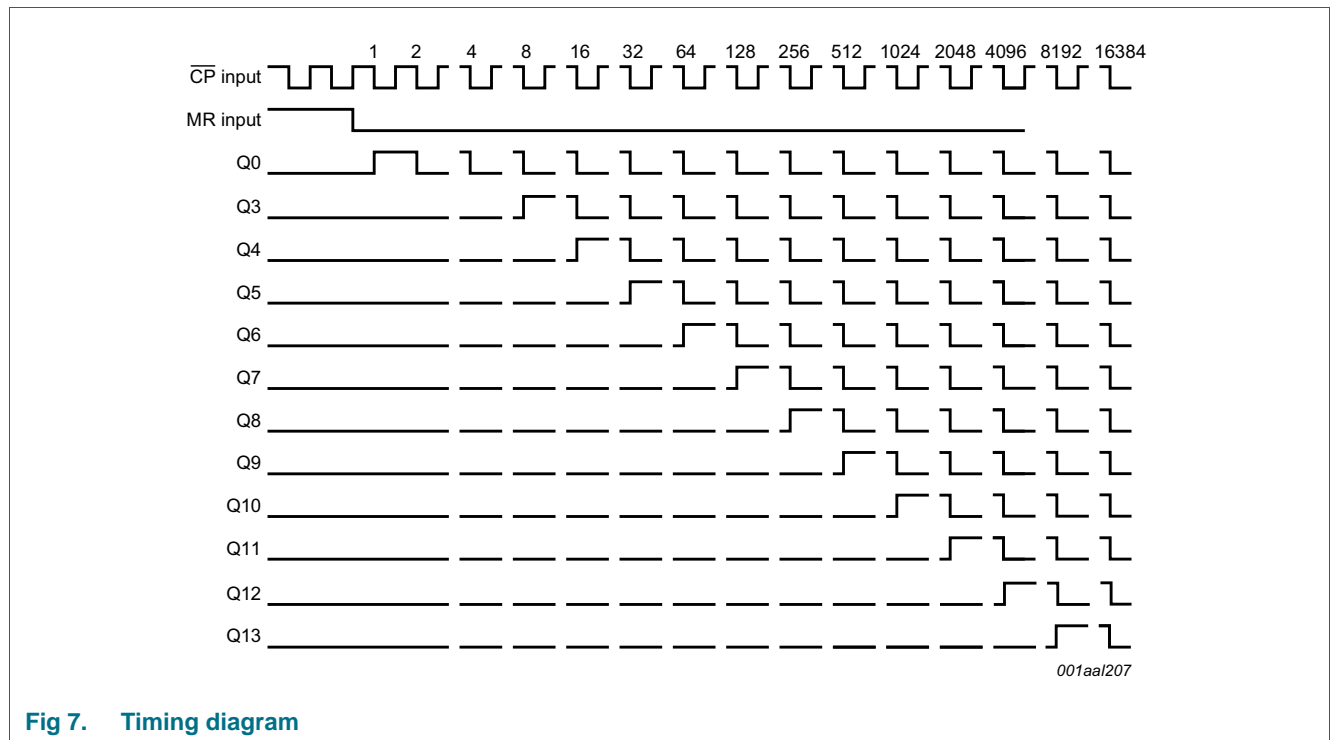


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA |
| I _{OK} | output clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA |
| I _O | output current | -0.5 V < V _O < V _{CC} + 0.5 V | - | ±25 | mA |
| I _{CC} | supply current | | - | ±50 | mA |
| I _{GND} | ground current | | - | ±50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [1] | | | |
| | | SO16, SSOP16, TSSOP16 and DHVQFN16 packages | - | 500 | mW |

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | 74HC4020 | | | 74HCT4020 | | | Unit |
|------------------|-------------------------------------|-----------------------------------|----------|------|-----------------|-----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| Δt/ΔV | input transition rise and fall rate | except for Schmitt trigger inputs | | | | | | | |
| | | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|----------------|---|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC4020 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = −20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = −20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = −20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = −4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| | | I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT4020 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = −20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = −4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | pin MR | - | 110 | 396 | - | 495 | - | 539 | μA |
| | | pin $\overline{\text{CP}}$ | - | 85 | 306 | - | 383 | - | 417 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristicsGND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC4020 | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Q0; see Figure 8 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V; C _L = 50 pF | - | 39 | 140 | - | 175 | - | 210 | ns |
| | | V _{CC} = 4.5 V; C _L = 50 pF | - | 14 | 28 | - | 35 | - | 42 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 11 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V; C _L = 50 pF | - | 11 | 24 | - | 30 | - | 36 | ns |
| | | Qn to Qn+1; see Figure 9 | | | | | | | | |
| | | V _{CC} = 2.0 V; C _L = 50 pF | - | 22 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V; C _L = 50 pF | - | 8 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 6 | - | - | - | - | - | ns |
| V _{CC} = 6.0 V; C _L = 50 pF | - | 6 | 13 | - | 16 | - | 19 | ns | | |
| t _{PHL} | HIGH to LOW propagation delay | MR to Qn; see Figure 8 | | | | | | | | |
| | | V _{CC} = 2.0 V; C _L = 50 pF | - | 55 | 170 | - | 215 | - | 225 | ns |
| | | V _{CC} = 4.5 V; C _L = 50 pF | - | 20 | 34 | - | 43 | - | 51 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 17 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V; C _L = 50 pF | - | 16 | 29 | - | 37 | - | 43 | ns |
| t _t | transition time | Qn; see Figure 8 ^[2] | | | | | | | | |
| | | V _{CC} = 2.0 V; C _L = 50 pF | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V; C _L = 50 pF | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V; C _L = 50 pF | - | 6 | 13 | - | 16 | - | 19 | ns |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_W | pulse width | \overline{CP} HIGH or LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 16 | 4 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V; $C_L = 50$ pF | 14 | 3 | - | 17 | - | 20 | - | ns |
| | | MR HIGH; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 16 | 6 | - | 20 | - | 24 | - | ns |
| t_{rec} | recovery time | MR to \overline{CP} ; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | 50 | 6 | - | 65 | - | 75 | - | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 10 | 2 | - | 13 | - | 15 | - | ns |
| f_{max} | maximum frequency | see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | 6.0 | 30 | - | 4.8 | - | 4.0 | - | MHz |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 30 | 92 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 101 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | 3 | - | 19 | - | - | - | - | - | pF |
| | | | | | | | | | | |
| 74HCT4020 | | | | | | | | | | |
| t_{pd} | propagation delay | \overline{CP} to Q0; see Figure 8 1 | | | | | | | | |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | - | 18 | 36 | - | 45 | - | 54 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| | | Qn to Qn+1; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | - | 8 | 15 | - | 19 | - | 22 | ns |
| t_{PHL} | HIGH to LOW propagation delay | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 6 | - | - | - | - | - | ns |
| | | MR to Qn; see Figure 8 | | | | | | | | |
| t_t | transition time | $V_{CC} = 4.5$ V; $C_L = 50$ pF | - | 22 | 45 | - | 56 | - | 68 | ns |
| | | Qn; see Figure 8 2 | | | | | | | | |
| t_W | pulse width | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 19 | - | - | - | - | - | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | \overline{CP} HIGH or LOW; see Figure 8 | | | | | | | | |
| t_{rec} | recovery time | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | MR HIGH; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 20 | 8 | - | 25 | - | 30 | - | ns |
| t_{rec} | recovery time | MR to \overline{CP} ; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 10 | 2 | - | 13 | - | 15 | - | ns |

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------|-------------------------------|---------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f_{max} | maximum frequency | see Figure 8 | | | | | | | | |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | 25 | 47 | - | 20 | - | 17 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 52 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | [3] | - | 20 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_i is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

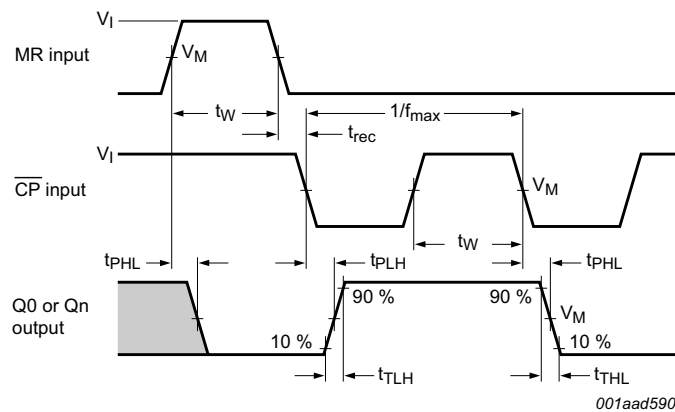
f_o = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

12. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Clock timing, propagation delays, pulse widths and measurement points

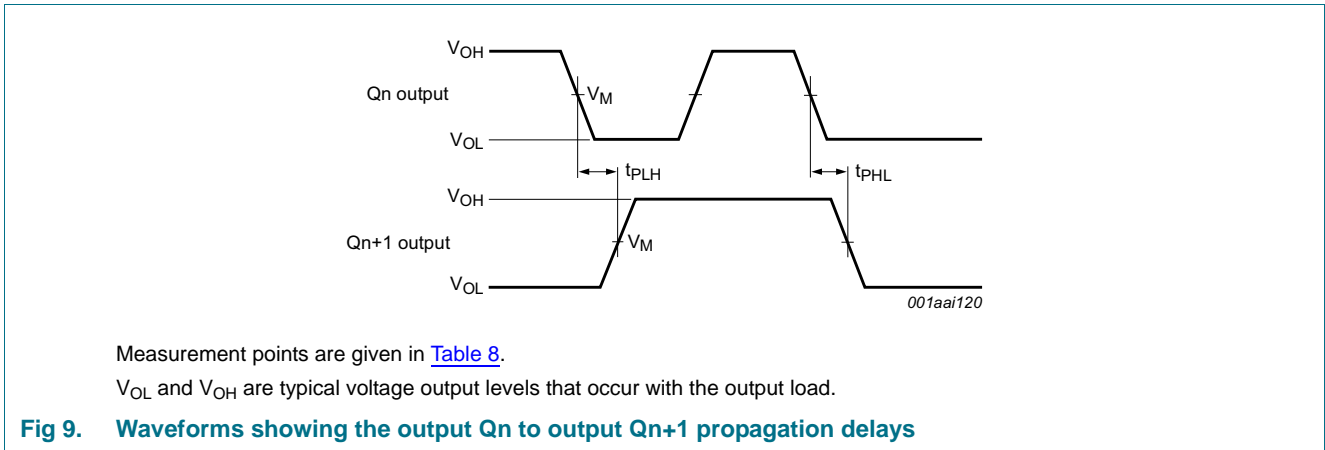
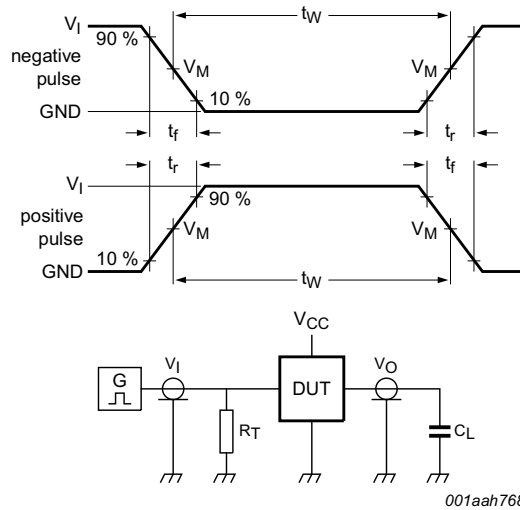


Table 8. Measurement points

| Type | Input | Output |
|-----------|---------------------|---------------------|
| | V_M | V_M |
| 74HC4020 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74HCT4020 | 1.3 V | 1.3 V |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load |
|-----------|----------|------------|--------------|
| | V_I | t_r, t_f | C_L |
| 74HC4020 | V_{CC} | 6 ns | 15 pF, 50 pF |
| 74HCT4020 | 3 V | 6 ns | 15 pF, 50 pF |

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

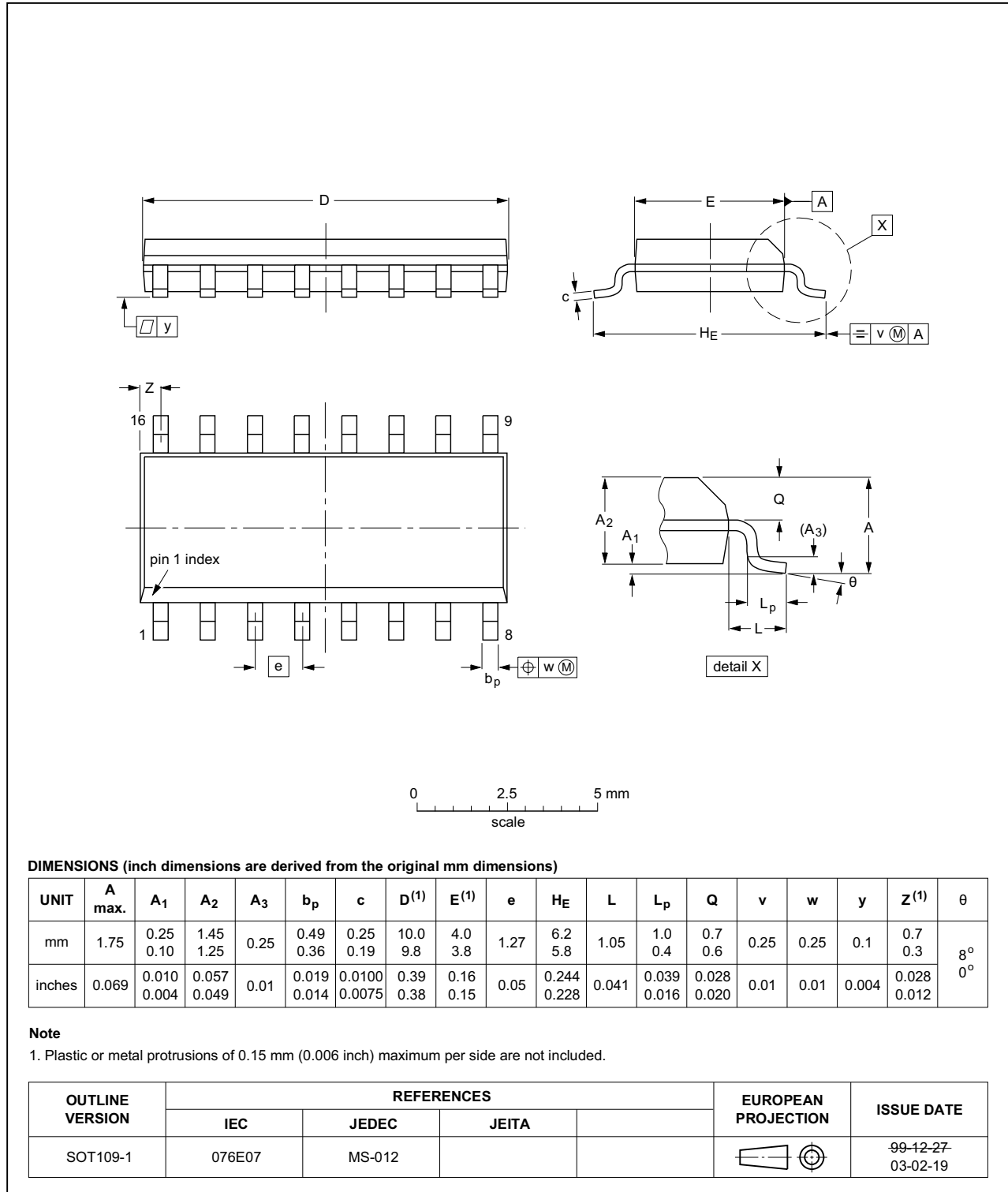


Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

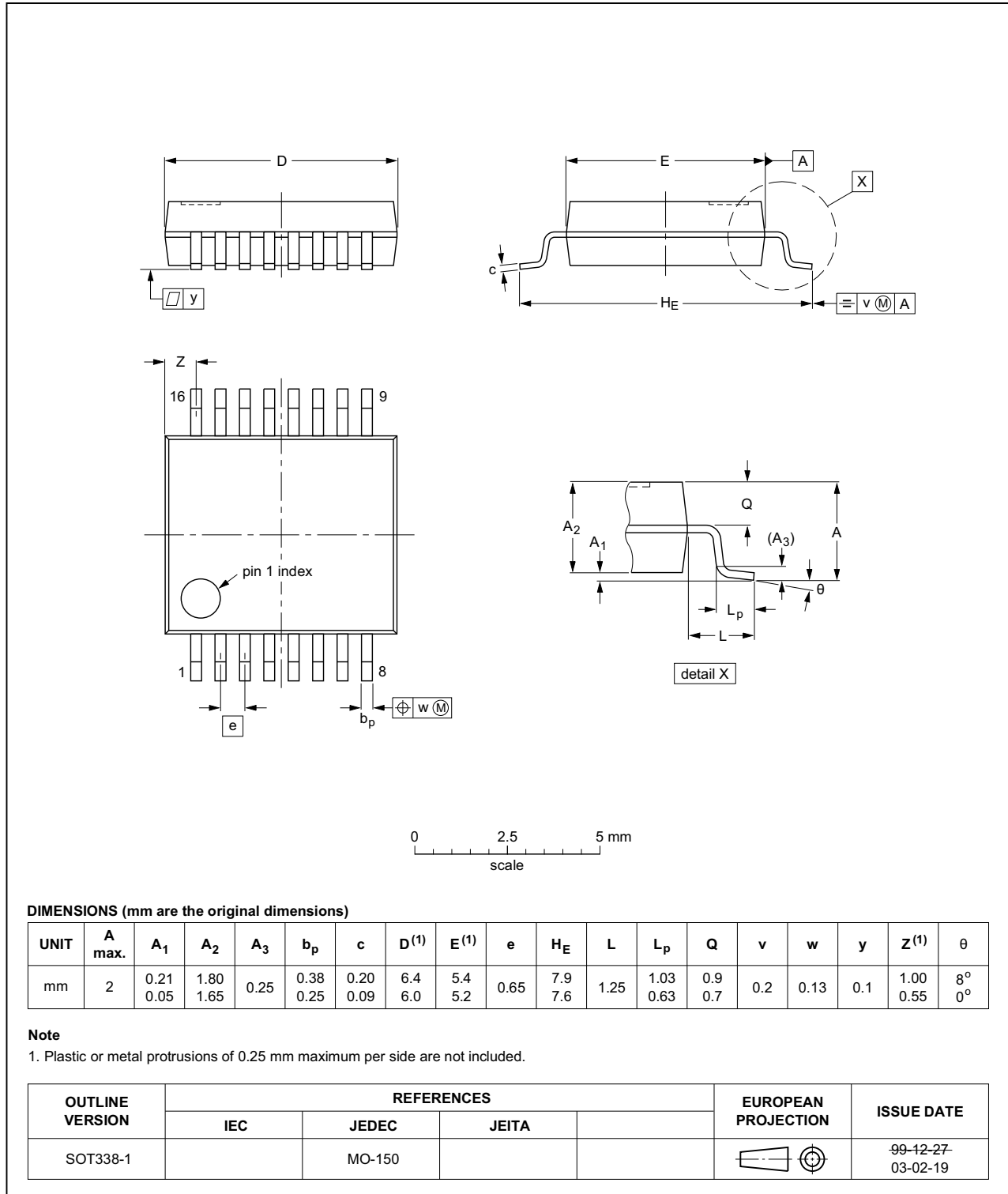


Fig 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

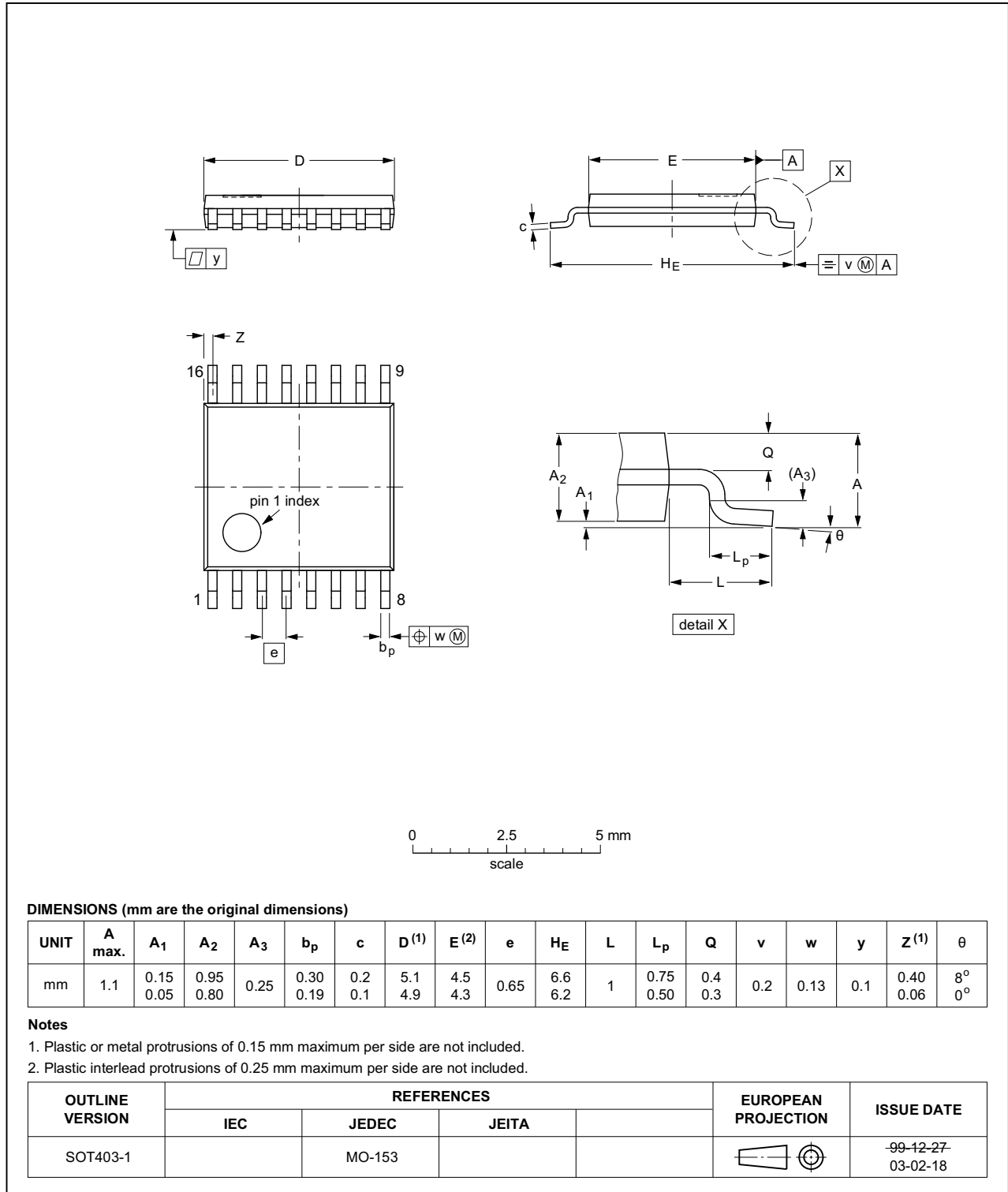


Fig 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

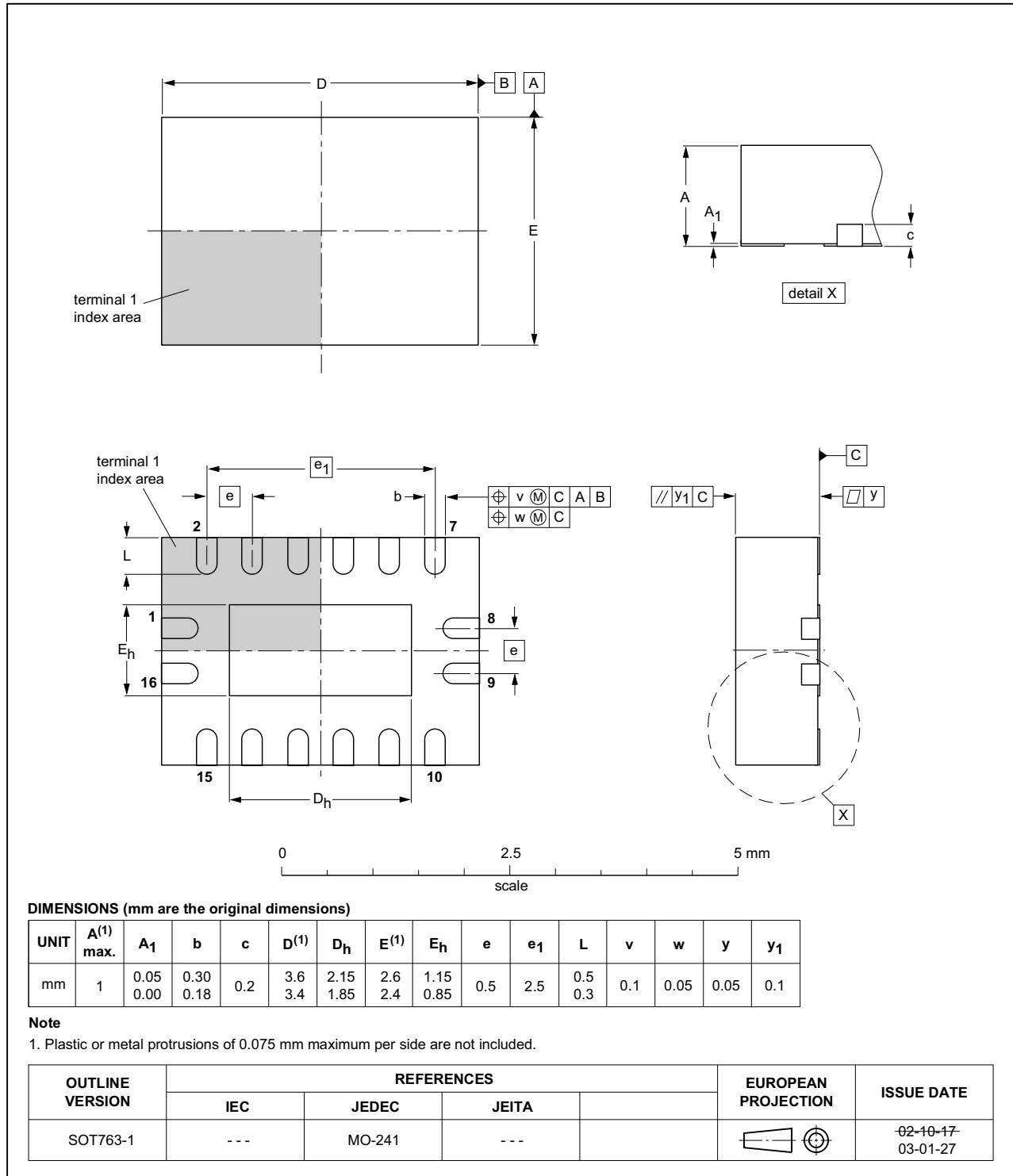


Fig 14. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

| Acronym | Abbreviation |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |

15. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--|-----------------------|---------------|----------------------|
| 74HC_HCT4020 v.6 | 20160203 | Product data sheet | - | 74HC_HCT4020 v.5 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC4020N and 74HCT4020N (SOT38-4) removed. | | | |
| 74HC_HCT4020 v.5 | 20120806 | Product data sheet | - | 74HC_HCT4020 v.4 |
| Modifications: | <ul style="list-style-type: none"> Measurement points added to figure 8 (errata). | | | |
| 74HC_HCT4020 v.4 | 20111213 | Product data sheet | - | 74HC_HCT4020 v.3 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74HC_HCT4020 v.3 | 20100120 | Product data sheet | - | 74HC_HCT4020_CNV v.2 |
| 74HC_HCT4020_CNV v.2 | 19970901 | Product specification | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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