



# THE DATASHEET OF SN74AC14D

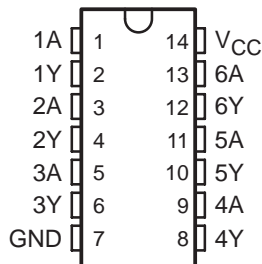


# SN54AC14, SN74AC14 HEX SCHMITT-TRIGGER INVERTERS

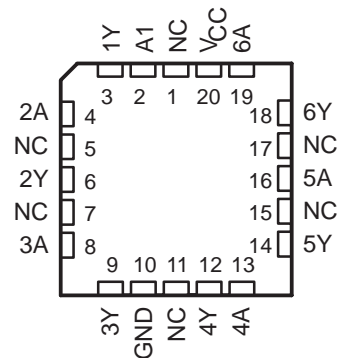
SCAS522G – AUGUST 1995 – REVISED AUGUST 2008

- 2-V to 6-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 6 V
- Max  $t_{pd}$  of 9.5 ns at 5 V

SN54AC14 ... J OR W PACKAGE  
SN74AC14 ... D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AC14 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$ . Because of the Schmitt action, they have different input threshold levels for positive-going ( $V_{T+}$ ) and for negative-going ( $V_{T-}$ ) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC14N	SN74AC14N
	SOIC – D	Tube	SN74AC14D	AC14
		Tape and reel	SN74AC14DR	
	SOP – NS	Tape and reel	SN74AC14NSR	AC14
	SSOP – DB	Tape and reel	SN74AC14DBR	AC14
TSSOP – PW	Tube	SN74AC14PW	AC14	
	Tape and reel	SN74AC14PWR		
-55°C to 125°C	CDIP – J	Tube	SNJ54AC14J	SNJ54AC14J
	CFP – W	Tube	SNJ54AC14W	SNJ54AC14W
	LCCC – FK	Tube	SNJ54AC14FK	SNJ54AC14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54AC14, SN74AC14 HEX SCHMITT-TRIGGER INVERTERS

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FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AC14		SN74AC14		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V		-12	-12	mA
		$V_{CC} = 4.5$ V		-24	-24	
		$V_{CC} = 5.5$ V		-24	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	12	mA
		$V_{CC} = 4.5$ V		24	24	
		$V_{CC} = 5.5$ V		24	24	
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AC14, SN74AC14 HEX SCHMITT-TRIGGER INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC14		SN74AC14		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>T+</sub> Positive-going threshold		3 V	0.8	1.8	2.2	0.8	2.2	0.8	2.2	V	
		4.5 V	1.5	2.6	3.2	1.5	3.2	1.5	3.2		
		5.5 V	1.6	3.2	3.9	1.6	3.9	1.6	3.9		
V <sub>T-</sub> Negative-going threshold		3 V	0.5	0.8	1	0.5	1.2	0.5	1	V	
		4.5 V	0.9	1.4	1.8	0.9	1.8	0.9	1.8		
		5.5 V	1.1	1.8	2.3	1.1	2.3	1.1	2.3		
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		3 V	0.3	1	1.2	0.3	1.2	0.3	1.2	V	
		4.5 V	0.4	1.2	1.4	0.4	1.4	0.4	1.4		
		5.5 V	0.5	1.4	1.6	0.5	1.6	0.5	1.6		
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9		V	
		4.5 V	4.4			4.4		4.4			
		5.5 V	5.4			5.4		5.4			
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.48			
		4.5 V	3.86			3.7		3.8			
	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.7		3.8			
		5.5 V	4.86			4.7		4.8			
I <sub>OH</sub> = -50 mA†	5.5 V				3.85						
I <sub>OH</sub> = -75 mA†	5.5 V						3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V	0.002		0.1	0.1		0.1		V	
		4.5 V	0.001		0.1	0.1		0.1			
		5.5 V	0.001		0.1	0.1		0.1			
	I <sub>OL</sub> = 12 mA	3 V				0.36		0.5			0.44
		4.5 V				0.36		0.5			0.44
	I <sub>OL</sub> = 24 mA	4.5 V				0.36		0.5			0.44
		5.5 V				0.36		0.5			0.44
I <sub>OL</sub> = 50 mA†	5.5 V						1.65				
I <sub>OL</sub> = 75 mA†	5.5 V								1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V				±0.1		±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				2		40		20	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5							pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.5	6	13.5	1	16	1.5	15	ns
t <sub>PHL</sub>			1.5	6	11.5	1	14	1.5	13	



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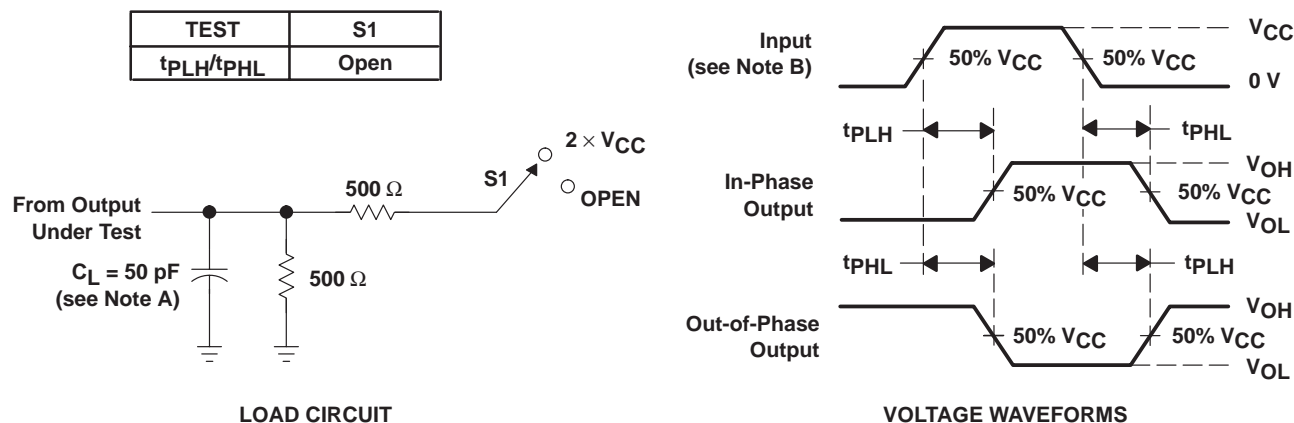
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1.5	5	10	1.5	12	1.5	11	ns
$t_{PHL}$			1.5	5	8.5	1.5	10	1.5	9.5	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	25	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87624012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK	<a href="#">Samples</a>
5962-8762401CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J	<a href="#">Samples</a>
5962-8762401DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W	<a href="#">Samples</a>
5962-8762401VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401VC A SNV54AC14J	<a href="#">Samples</a>
5962-8762401VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401VD A SNV54AC14W	<a href="#">Samples</a>
5962-8762402VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762402VC A SNV54AC14J	<a href="#">Samples</a>
5962-8762402VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762402VD A SNV54AC14W	<a href="#">Samples</a>
SN74AC14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC14N	<a href="#">Samples</a>
SN74AC14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC14NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SN74AC14PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14	<a href="#">Samples</a>
SNJ54AC14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87624012A SNJ54AC 14FK	<a href="#">Samples</a>
SNJ54AC14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J	<a href="#">Samples</a>
SNJ54AC14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC14, SN54AC14-SP, SN74AC14 :**

- Catalog: [SN74AC14](#), [SN54AC14](#)
  
- Automotive: [SN74AC14-Q1](#), [SN74AC14-Q1](#)
  
- Military: [SN54AC14](#)
  
- Space: [SN54AC14-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Military - QML certified for Military and Defense Applications
  
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC14DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AC14DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74AC14NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AC14PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

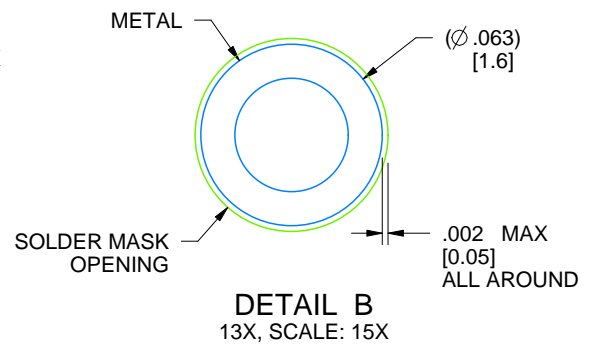
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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