



**THE DATASHEET OF  
SN74145N**



# SN54145, SN54LS145, SN74145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

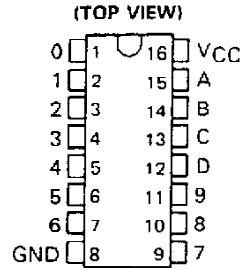
SDLS051

MARCH 1974 — REVISED MARCH 1988

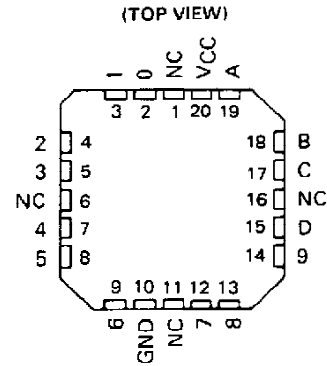
FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145 . . . 35 mW Typical

SN54145, SN54LS145 . . . J OR W PACKAGE  
SN74145 . . . N PACKAGE  
SN74LS145 . . . D OR N PACKAGE



SN54LS145 . . . FK PACKAGE



NC : No internal connection

FUNCTION TABLE

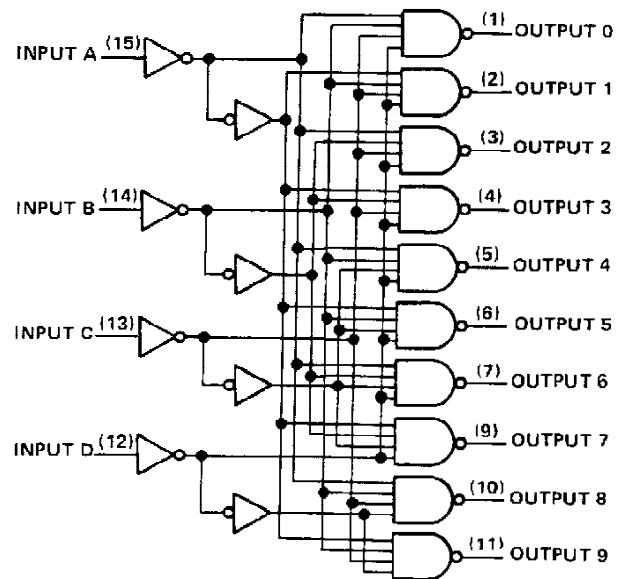
| NO.     | INPUTS |   |   |   | OUTPUTS |   |   |   |   |   |   |   |   |   |
|---------|--------|---|---|---|---------|---|---|---|---|---|---|---|---|---|
|         | D      | C | B | A | 0       | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0       | L      | L | L | L | L       | H | H | H | H | H | H | H | H | H |
| 1       | L      | L | L | H | H       | L | H | H | H | H | H | H | H | H |
| 2       | L      | L | H | L | H       | H | L | H | H | H | H | H | H | H |
| 3       | L      | L | H | H | H       | H | H | L | H | H | H | H | H | H |
| 4       | L      | H | L | L | H       | H | H | H | L | H | H | H | H | H |
| 5       | L      | H | L | H | H       | H | H | H | H | L | H | H | H | H |
| 6       | L      | H | H | L | H       | H | H | H | H | H | L | H | H | H |
| 7       | L      | H | H | H | H       | H | H | H | H | H | H | L | H | H |
| 8       | H      | L | L | L | H       | H | H | H | H | H | H | H | L | H |
| 9       | H      | L | L | H | H       | H | H | H | H | H | H | H | H | L |
| INVALID | H      | L | H | L | H       | H | H | H | H | H | H | H | H | H |
|         | H      | L | H | H | H       | H | H | H | H | H | H | H | H | H |
|         | H      | H | L | L | H       | H | H | H | H | H | H | H | H | H |
|         | H      | H | L | H | H       | H | H | H | H | H | H | H | H | H |
|         | H      | H | H | L | H       | H | H | H | H | H | H | H | H | H |

H = high level (off), L = low level (on)

## description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

## logic diagram



Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 855010 • DALLAS, TEXAS 75265

# SN54LS145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)         | 7 V            |
| Input voltage                                 | 5.5 V          |
| Maximum current into any output (off-state)   | 1 mA           |
| Operating free-air temperature range: SN54145 | -55°C to 125°C |
| SN74145                                       | 0°C to 70°C    |
| Storage temperature range                     | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

|  | SN54145 |     |     | SN74145 |     |      | UNIT |
|--|---------|-----|-----|---------|-----|------|------|
|  | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| Supply voltage, $V_{CC}$               | 4.5     | 5   | 5.5 | 4.75    | 5   | 5.25 | V    |
| Off-state output voltage, $V_{O(off)}$ | 15      |     |     | 15      |     |      | V    |
| Operating free-air temperature, $T_A$  | -55     |     | 125 | 0       |     | 70   | °C   |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS†   | MIN     | TYP‡ | MAX  | UNIT          |
|--|--|---------|------|------|---------------|
| $V_{IH}$ High-level input voltage            |  | 2       |      |      | V             |
| $V_{IL}$ Low-level input voltage             |  |         |      | 0.8  | V             |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$   |         |      | -1.5 | V             |
| $I_{O(off)}$ Off-state output current        | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = 0.8 \text{ V}$ , $V_{O(off)} = 15 \text{ V}$ |         |      | 250  | $\mu\text{A}$ |
| $V_{O(on)}$ On-state output voltage          | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = 0.8 \text{ V}$                               |         | 0.5  | 0.9  | V             |
|  |  |         |      | 0.4  | V             |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$  |         |      | 1    | mA            |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$  |         |      | 40   | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$  |         |      | -1.6 | mA            |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX}$ . See Note 2   |         |      |      | mA            |
|  |  | SN54145 | 43   | 62   |               |
|  |  | SN74145 | 43   | 70   |               |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

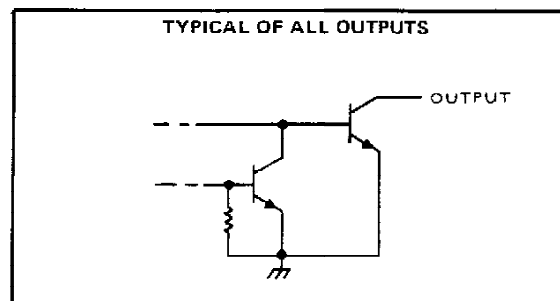
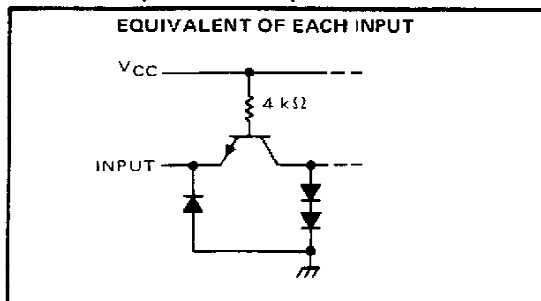
NOTE 2:  $I_{CC}$  is measured with all inputs grounded and outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER  | TEST CONDITIONS   | MIN | MAX | UNIT |
|--|---|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $C_L = 15 \text{ pF}$ , $R_L = 100 \Omega$ , See Note 3 |     | 50  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output |   |     | 50  | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54145, SN74145 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage                                   | 7 V            |
| Operating free-air temperature range: SN54LS145 | -55°C to 125°C |
| SN74LS145                                       | 0°C to 70°C    |
| Storage temperature range                       | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

|  | SN54LS145 |     |     | SN74LS145 |     |      | UNIT |
|--|-----------|-----|-----|-----------|-----|------|------|
|  | MIN       | NOM | MAX | MIN       | NOM | MAX  |      |
| Supply voltage, $V_{CC}$               | 4.5       | 5   | 5.5 | 4.75      | 5   | 5.25 | V    |
| Off-state output voltage, $V_{O(off)}$ | 15        |     |     | 15        |     |      | V    |
| Operating free-air temperature, $T_A$  | -55       |     |     | 125       |     |      | °C   |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS†  | SN54LS145                |      |     | SN74LS145 |      |     | UNIT |
|--|---|--------------------------|------|-----|-----------|------|-----|------|
|  |   | MIN                      | TYP‡ | MAX | MIN       | TYP‡ | MAX |      |
| $V_{IH}$ High-level input voltage            |   | 2                        |      |     | 2         |      |     | V    |
| $V_{IL}$ Low-level input voltage             |   | 0.7                      |      |     | 0.8       |      |     | V    |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$   | -1.5                     |      |     | -1.5      |      |     | V    |
| $I_{O(off)}$ Off-state output current        | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 15 \text{ V}$ | 250                      |      |     | 250       |      |     | µA   |
| $V_{O(on)}$ On-state output voltage          | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$                        | $I_{OL} = 12 \text{ mA}$ | 0.25 | 0.4 | 0.25      | 0.4  | V   |      |
|  |   | $I_{OL} = 24 \text{ mA}$ |      |     | 0.35      | 0.5  |     |      |
|  |   | $I_{OL} = 80 \text{ mA}$ |      |     | 2.3       | 3    |     |      |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$  | 0.1                      |      |     | 0.1       |      |     | mA   |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$  | 20                       |      |     | 20        |      |     | µA   |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$  | -0.4                     |      |     | -0.4      |      |     | mA   |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX},$ See Note 2   | 7                        | 13   |     |           | 7    | 13  | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

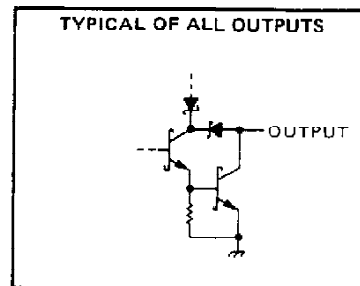
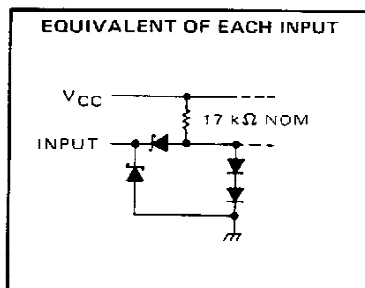
NOTE 2:  $I_{CC}$  is measured with all inputs grounded and outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

| PARAMETER  | TEST CONDITIONS                                     | MIN | MAX | UNIT |
|--|---|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $C_L = 45 \text{ pF}, R_L = 665 \Omega,$ See Note 3 | 50  |     | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output |   | 50  |     | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

### schematic of inputs and outputs



**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)            | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-8508401VEA  | ACTIVE        | CDIP         | J                  | 16   | 25             | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-8508401VE<br>A<br>SNV54LS145J | <a href="#">Samples</a> |
| 85084012A        | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 85084012A<br>SNJ54LS<br>145FK      | <a href="#">Samples</a> |
| 8508401EA        | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 8508401EA<br>SNJ54LS145J           | <a href="#">Samples</a> |
| 8508401FA        | ACTIVE        | CFP          | W                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 8508401FA<br>SNJ54LS145W           | <a href="#">Samples</a> |
| SN54LS145J       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | SN54LS145J                         | <a href="#">Samples</a> |
| SN74145N         | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | SN74145N                           | <a href="#">Samples</a> |
| SN74LS145D       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LS145                              | <a href="#">Samples</a> |
| SN74LS145DG4     | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LS145                              | <a href="#">Samples</a> |
| SN74LS145DR      | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LS145                              | <a href="#">Samples</a> |
| SN74LS145DRE4    | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LS145                              | <a href="#">Samples</a> |
| SN74LS145N       | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | SN74LS145N                         | <a href="#">Samples</a> |
| SN74LS145NE4     | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | SN74LS145N                         | <a href="#">Samples</a> |
| SN74LS145NSR     | ACTIVE        | SO           | NS                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 74LS145                            | <a href="#">Samples</a> |
| SNJ54145J        | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | SNJ54145J                          | <a href="#">Samples</a> |
| SNJ54LS145FK     | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 85084012A<br>SNJ54LS<br>145FK      | <a href="#">Samples</a> |
| SNJ54LS145J      | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 8508401EA<br>SNJ54LS145J           | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)  | Samples        |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|--------------------------|----------------|
| SNJ54LS145W      | ACTIVE        | CFP          | W                  | 16   | 1              | TBD             | A42                     | N / A for Pkg Type   | -55 to 125   | 8508401FA<br>SNJ54LS145W | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54145, SN54LS145, SN54LS145-SP, SN74145, SN74LS145 :**

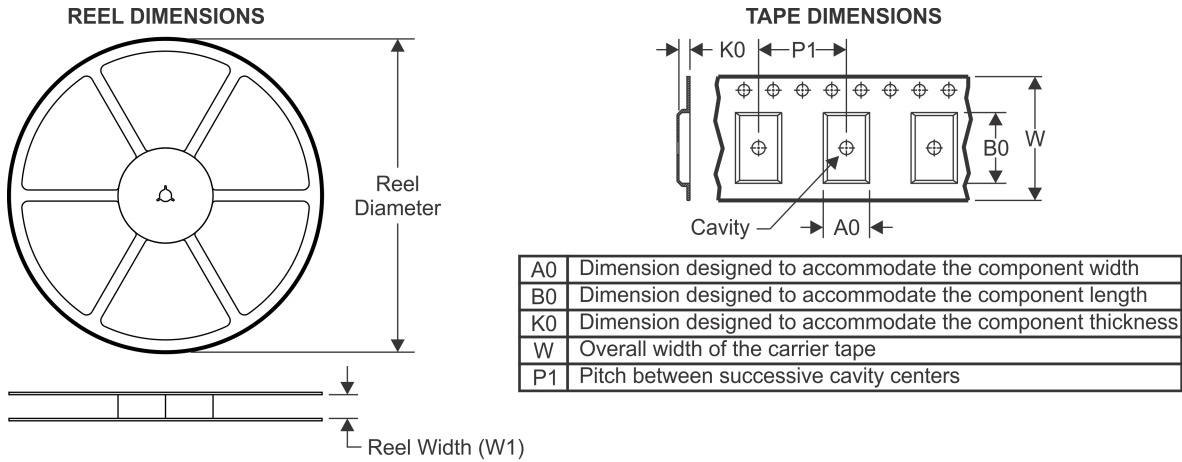
● Catalog: [SN74145](#), [SN74LS145](#), [SN54LS145](#)

- Military: [SN54145](#), [SN54LS145](#)
- Space: [SN54LS145-SP](#)

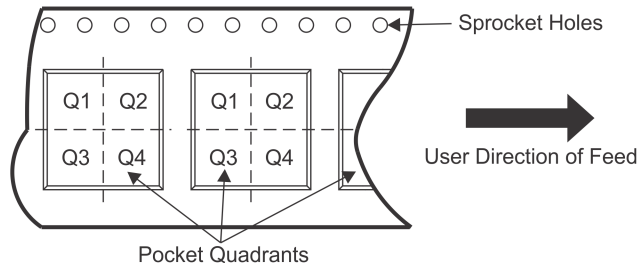
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS145DR | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

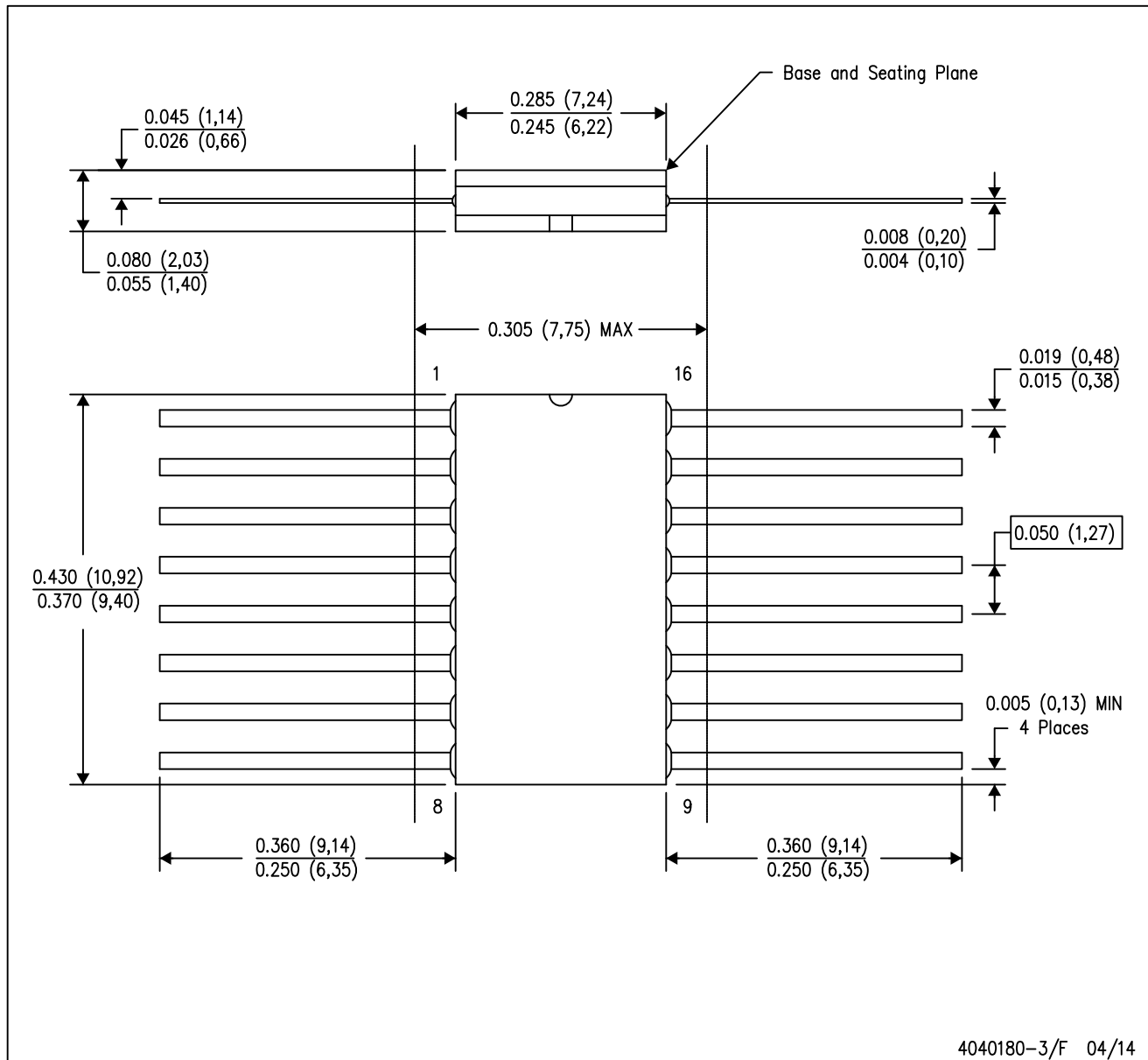


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS145DR | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

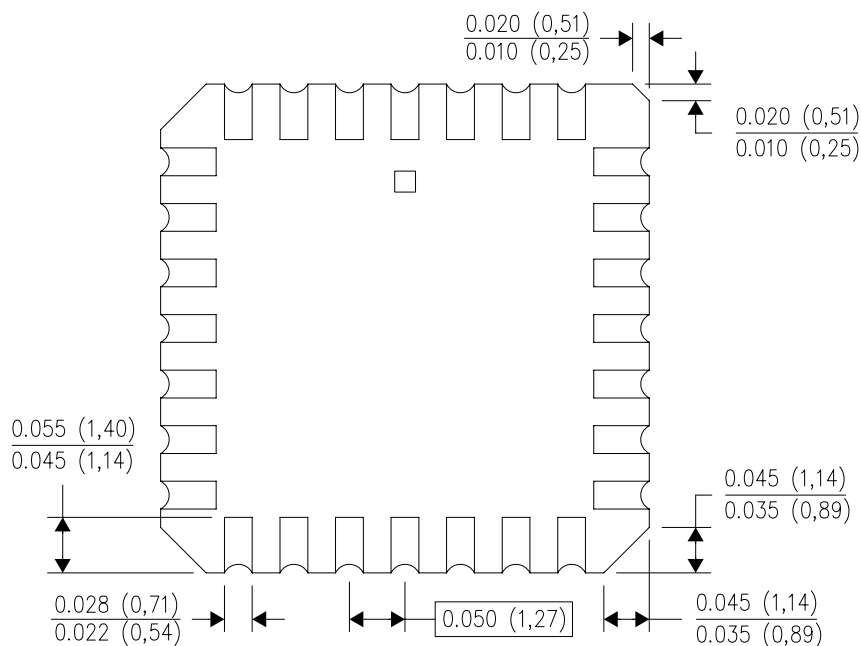
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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