



FAST CMOS 8-BIT IDENTITY COMPARATOR

74FCT521AT/CT

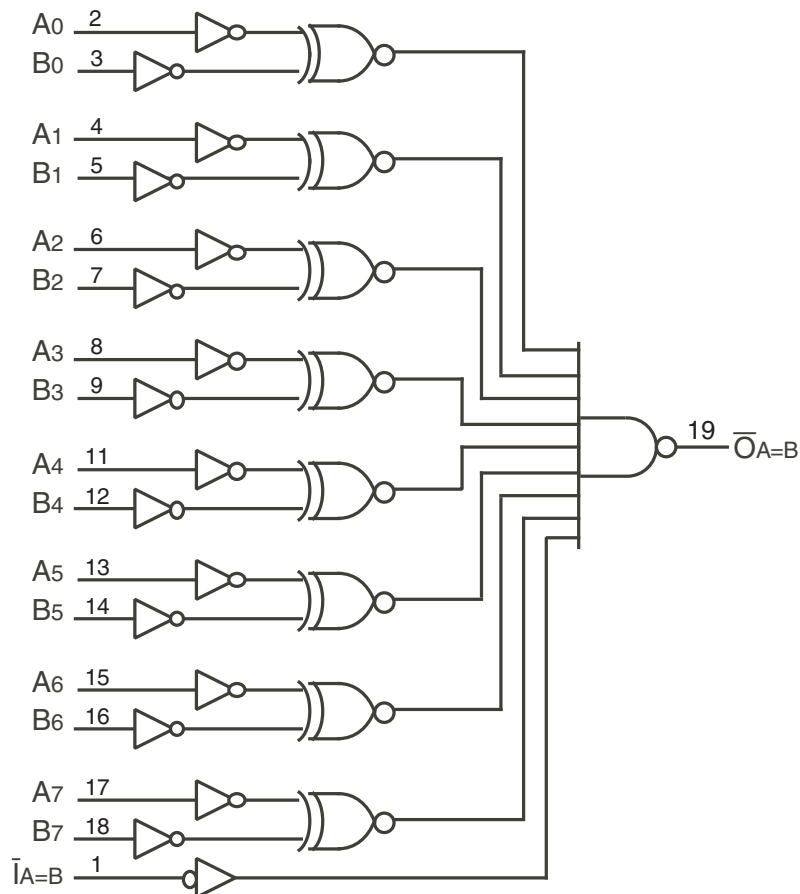
FEATURES:

- A and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The IDT74FCT521T is an 8-bit identity comparator built using an advanced dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a low output when the two words match bit for bit. The expansion input $\bar{A} = B$ also serves as an active low enable input.

FUNCTIONAL BLOCK DIAGRAM

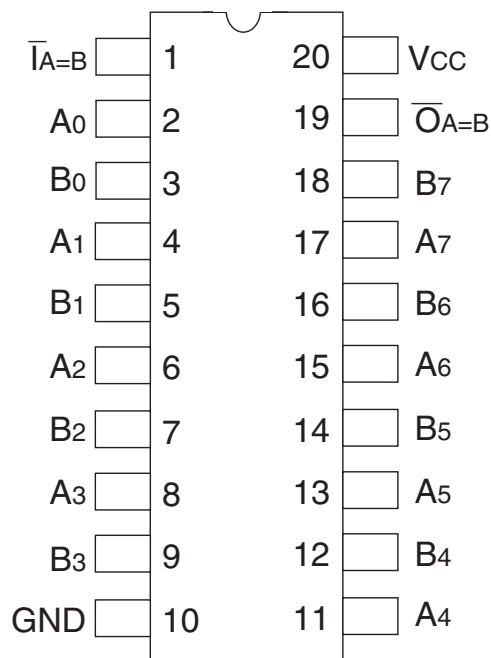


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INDUSTRIAL TEMPERATURE RANGE

MAY 2019

PIN CONFIGURATION



TOP VIEW

| Package Type | Package Code | Order Code |
|--------------|--------------|------------|
| QSOP | PCG20 | QG |
| SOIC | PSG20 | SOG |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--------------------------------------|-----------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to VCC+0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -60 to +120 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
- Inputs and VCC terminals only.
- Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN | Input Capacitance | VIN = 0V | 6 | 10 | pF |
| COUT | Output Capacitance | VOUT = 0V | 8 | 12 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|-----------|--|
| A0 - A7 | Word A Inputs |
| B0 - B7 | Word B Inputs |
| IA = B | Expansion or Enable Input (Active LOW) |
| OA = B | Identity Output (Active LOW) |

FUNCTION TABLE⁽¹⁾

| Inputs | | Output |
|--------|--------|--------|
| IA = B | A, B | OA = B |
| L | A = B* | L |
| L | A ≠ B | H |
| H | A = B* | H |
| H | A ≠ B | H |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
*A0 = B0, A1 = B1, A2 = B2, etc.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------|-----------------------------------|---|-------------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| I_{IH} | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_I = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{IL} | Input LOW Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_I = 0.5\text{V}$ | — | — | ± 1 | μA |
| I_I | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$ | | — | — | ± 1 | μA |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | | — | -0.7 | -1.2 | V |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | | -60 | -120 | -225 | mA |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -8\text{mA}$ | 2.4 | 3.3 | — | V |
| | | | $I_{OH} = -15\text{mA}$ | 2 | 3 | — | |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 48\text{mA}$ | — | 0.3 | 0.5 | V |
| V_H | Input Hysteresis | — | | — | 200 | — | mV |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC} | | — | 0.01 | 1 | mA |

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|---|--|-------------------------------------|------|---------------------|------|------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$ | | — | 0.5 | 2 | mA |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 0.15 | 0.25 | mA/ MHz |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ One Bit Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 1.5 | 3.5 | mA |
| | | | $V_{IN} = 3.4V$ $V_{IN} = GND$ | — | 1.8 | 4.5 | |

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Output Frequency

N_i = Number of Outputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

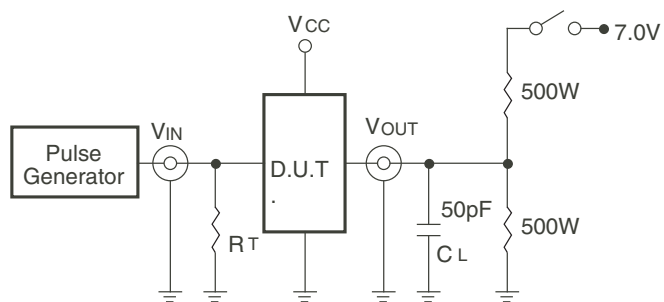
| Symbol | Parameter | Condition ⁽¹⁾ | 74FCT521AT | | 74FCT521CT | | Unit |
|-----------|-----------------------------|--|---------------------|------|---------------------|------|------|
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| t_{PLH} | Propagation Delay | $C_L = 50\text{pF}$ $R_L = 500\Omega$ | 1.5 | 7.2 | 1.5 | 4.5 | ns |
| t_{PHL} | Ax or Bx to $\bar{O}_A = B$ | | | | | | |
| t_{PLH} | Propagation Delay | $\bar{I}_A = B$ to $\bar{O}_A = B$ | 1.5 | 6 | 1.5 | 4.1 | ns |
| t_{PHL} | | | | | | | |

NOTES:

1. See test circuit and waveforms.

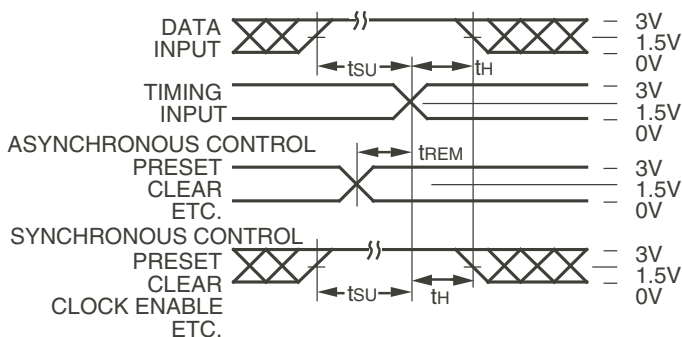
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



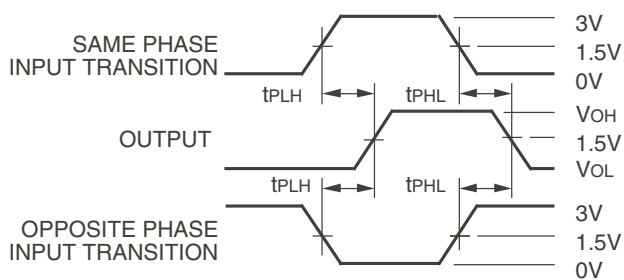
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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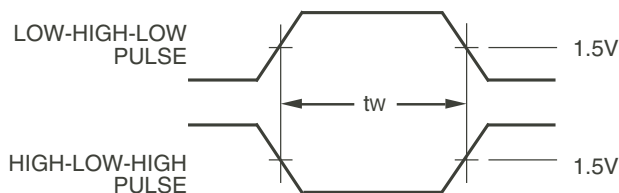
Propagation Delay

SWITCH POSITION

| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

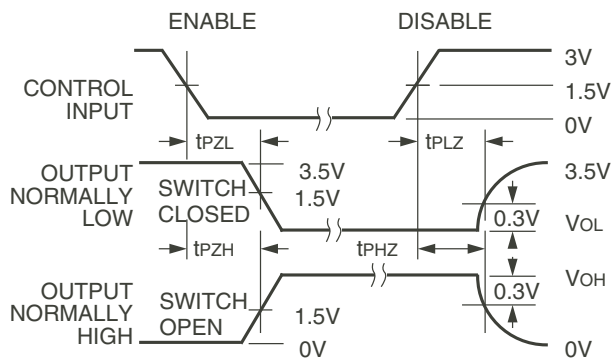
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link



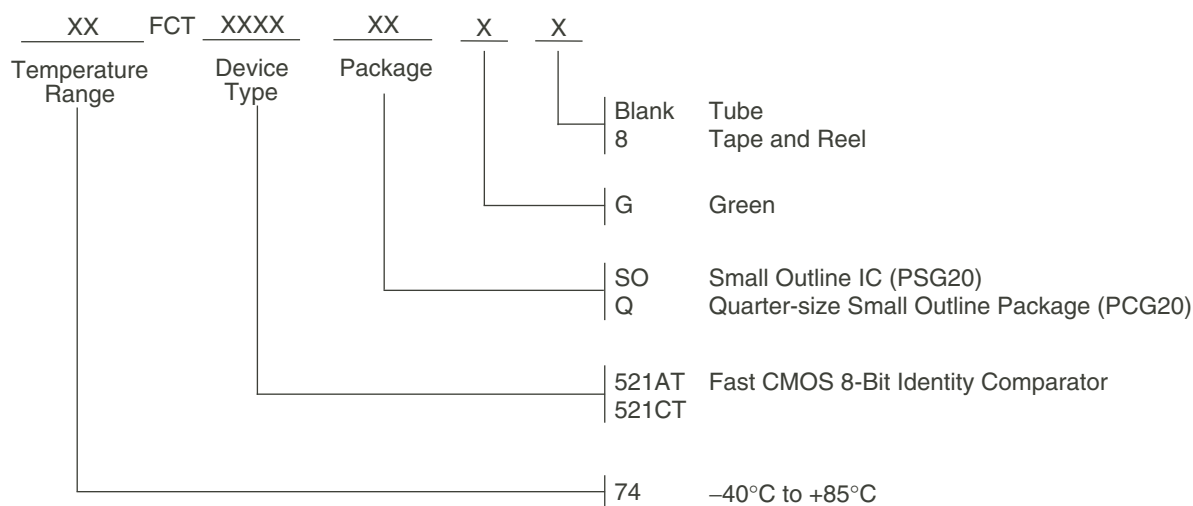
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Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



Orderable Part Information

| Speed Grade | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|-------------|-------------------|-----------|-----------|-------------|
| A | 74FCT521ATQG | PCG20 | QSOP | I |
| | 74FCT521ATQG8 | PCG20 | QSOP | I |
| | 74FCT521ATSOG | PSG20 | SOIC | I |
| | 74FCT521ATSOG8 | PSG20 | SOIC | I |
| C | 74FCT521CTQG | PCG20 | QSOP | I |
| | 74FCT521CTQG8 | PCG20 | QSOP | I |
| | 74FCT521CTSOG | PSG20 | SOIC | I |
| | 74FCT521CTSOG8 | PSG20 | SOIC | I |

Datasheet Document History

| | | |
|------------|----------|--|
| 10/03/2009 | Pg. 6 | Updated the ordering information by removing the "IDT" notation and non RoHS part. |
| 05/10/2018 | Pg. 2, 6 | Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram by deleting PYG package and adding Tube, Tape and Reel. Added new table of orderable part information. |
| 05/03/2019 | Pg. 6 | Updated ordering information diagram. |



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