



3.3V CMOS 16-BIT REGISTER (3-STATE)

IDT74FCT163374A/C

FEATURES:

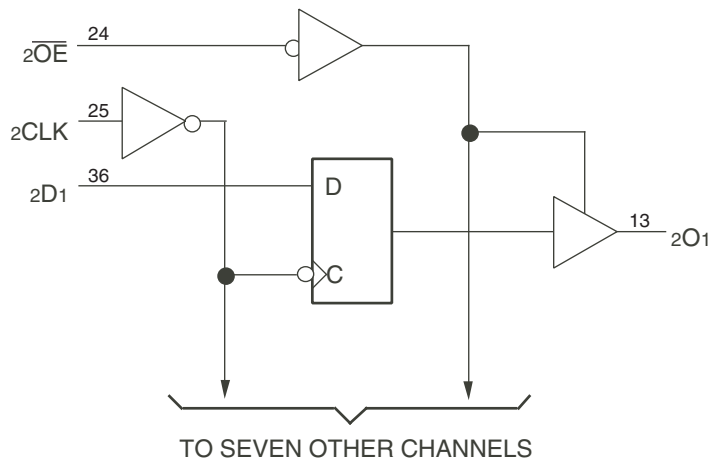
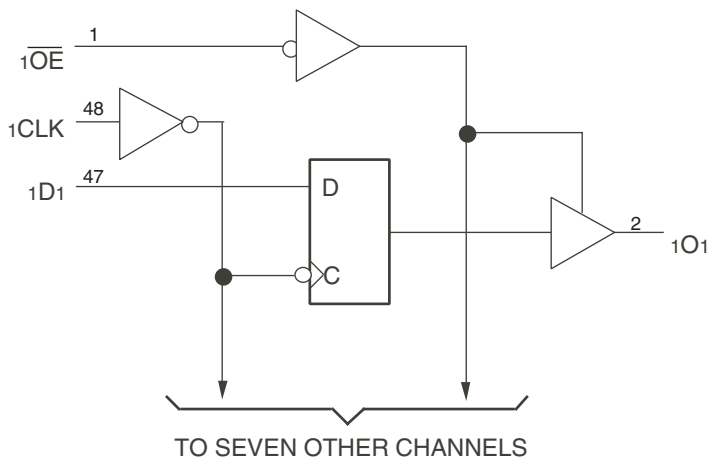
- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range, or $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components
- Available in SSOP and TSSOP packages

DESCRIPTION:

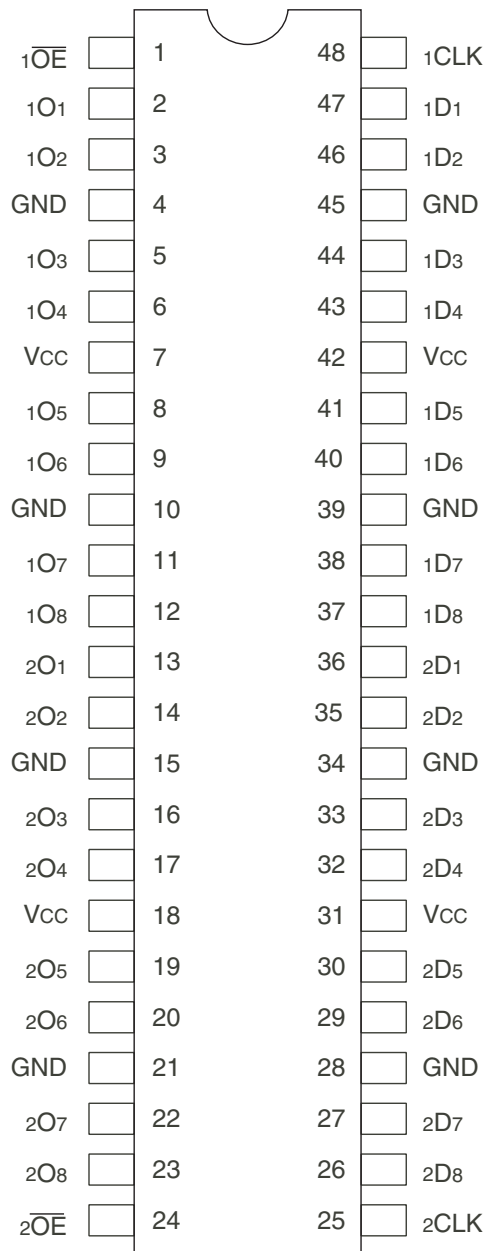
The FCT163374 16-bit edge-triggered D-type register is built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable (\overline{xOE}) and clock ($xCLK$) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The inputs of FCT163374 can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PAG48	PAG
SSOP	PVG48	PVG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOU = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs
xOE	3-State Output Enable Input (Active LOW)

FUNCTION TABLE⁽¹⁾

Function	Inputs			Outputs
	xDx	xCLK	xOE	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	5.5	V	
	Input HIGH Level (I/O pins)		2	—	V _{CC} +0.5		
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _I = 5.5V	—	—	±1	
	Input HIGH Current (I/O pins)						V _I = V _{CC}
I _{IL}	Input LOW Current (Input pins)		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins)						V _I = GND
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	
I _{OZL}			V _O = GND	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA	
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -0.1mA	V _{CC} -0.2	—	—	
		V _{IN} = V _{IH} or V _{IL}					I _{OH} = -3mA
		V _{CC} = 3V	I _{OH} = -8mA	2.4 ⁽⁵⁾	3	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min.	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	—	—	0.2
				I _{OL} = 16mA	—	0.2	0.4
				I _{OL} = 24mA	—	0.3	0.55
		V _{CC} = 3V	I _{OL} = 24mA	—	0.3	0.5	
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	—	—	—	—	
							—
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.1	10	μA	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC}-0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$		—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	50	75	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $f_i = 5\text{MHz}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.5	0.8	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $f_i = 2.5\text{MHz}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.5	$3.8^{(5)}$	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2.5	$4^{(5)}$	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

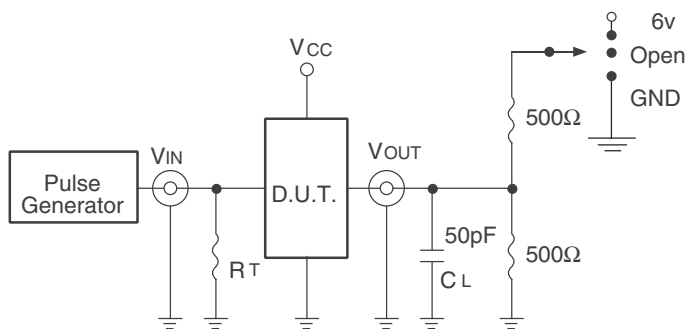
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽²⁾	FCT163374A		FCT163374C		Unit
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2	6.5	2	5.2	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	6.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	5.5	1.5	5	ns
t _{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2	—	2	—	ns
t _H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	ns
t _w	xCLK Pulse Width HIGH		5	—	5	—	ns
t _{sk(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	ns

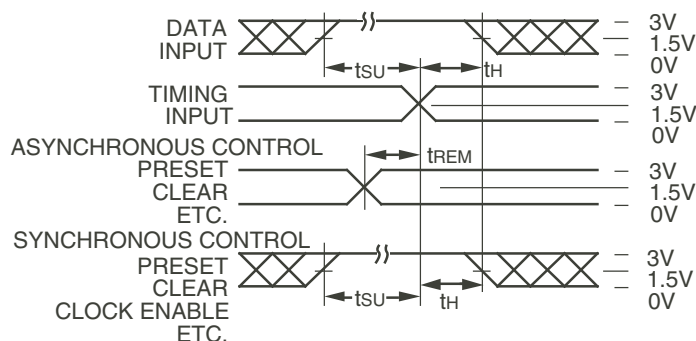
NOTES:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

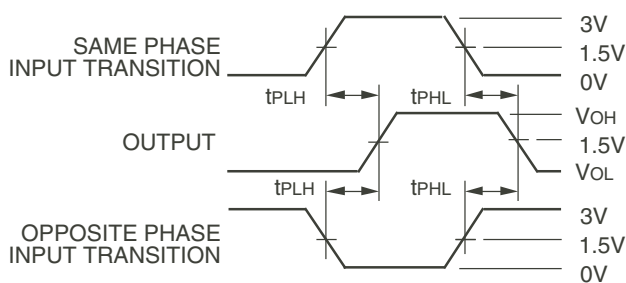
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



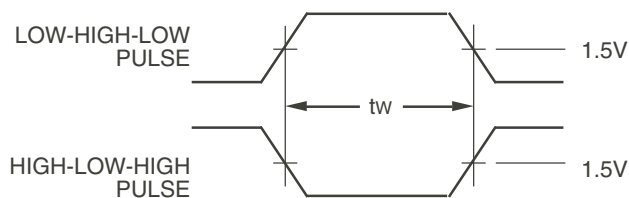
Propagation Delay

SWITCH POSITION

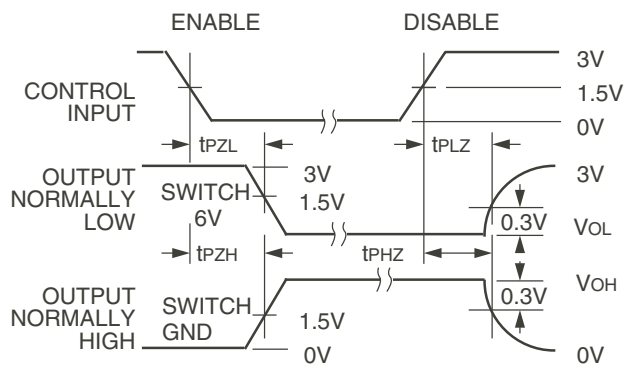
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

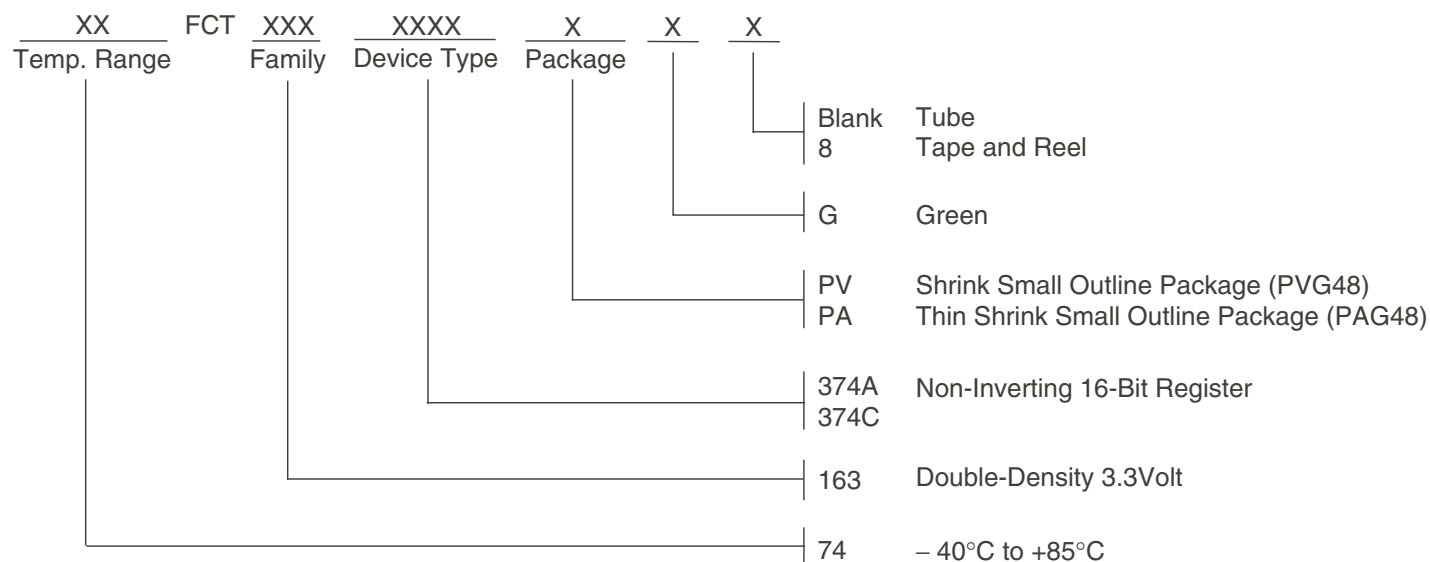


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.
3. If VCC is below 3V, input voltage swings should be adjusted not to exceed VCC.

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT163374APAG	PAG48	TSSOP	I
	74FCT163374APAG8	PAG48	TSSOP	I
	74FCT163374APVG	PVG48	SSOP	I
	74FCT163374APVG8	PVG48	SSOP	I
C	74FCT163374CPAG	PAG48	TSSOP	I
	74FCT163374CPAG8	PAG48	TSSOP	I
	74FCT163374CPVG	PVG48	SSOP	I
	74FCT163374CPVG8	PVG48	SSOP	I

Datasheet Document History

09/10/2009	Pg.7	Updated the ordering information by removing the "IDT" notation and non RoHS part.
05/07/2018	Pg. 1, 2, 5, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added orderable part information table.



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