



THE DATASHEET OF
74F862N



DATA SHEET

74F862

Bus transceiver, inverting (3-State)

Product data
Replaces data sheet 74F862, 74F863 of 2000 Mar 24

2004 Jan 23

Bus transceiver, inverting (3-State)

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FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- High impedance NPN base inputs for reduced loading (20 μ A in HIGH and LOW states)
- I_{IL} is 20 μ A for minimum bus loading
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim dual in-line (DIP) 300 mil package
- Broadside pinout
- Outputs sink 64 mA

DESCRIPTION

The 74F862 bus transceiver provides a high performance inverting bus interface for wide data/address paths of buses carrying parity.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F862	6.0 ns	150 mA

ORDERING INFORMATION

COMMERCIAL RANGE: $V_{CC} = 5 V \pm 10\%$; $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$

Type number	Package		
	Name	Description	Version
N74F862N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
N74F862D (see Note 1)	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

NOTE:

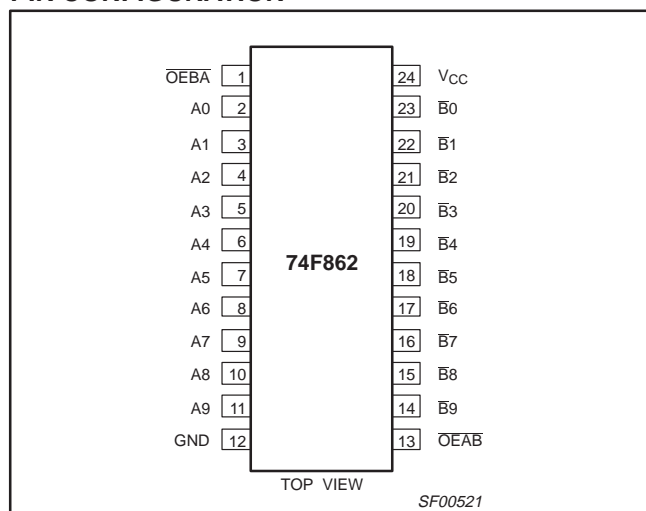
1. Thermal mounting techniques are recommended. See SMD Process Applications for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A9	Data transmit inputs	1.0/0.033	20 μ A / 20 μ A
$\bar{B}0$ – $\bar{B}9$	Data receive inputs	1.0/0.033	20 μ A / 20 μ A
$\bar{O}EBA$	Transmit output enable input	1.0/0.033	20 μ A / 20 μ A
$\bar{O}EAB$	Receive output enable input	1.0/0.033	20 μ A / 20 μ A

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the HiGH state and 0.6 mA in the LOW state.

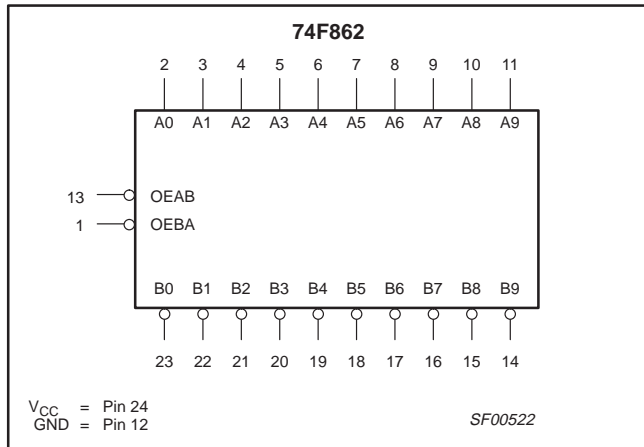
PIN CONFIGURATION



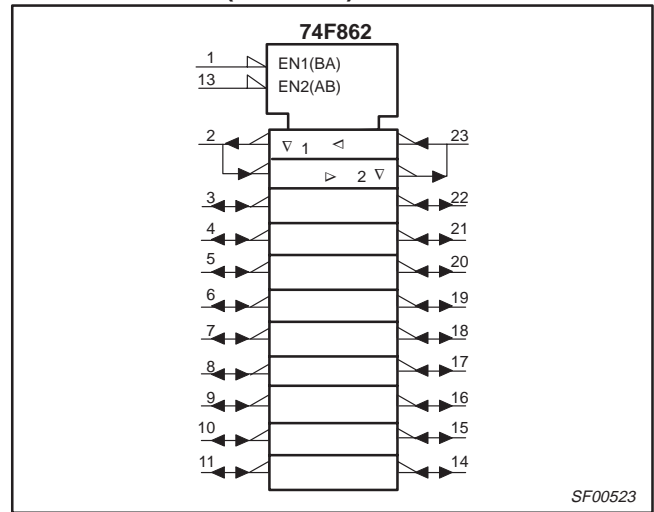
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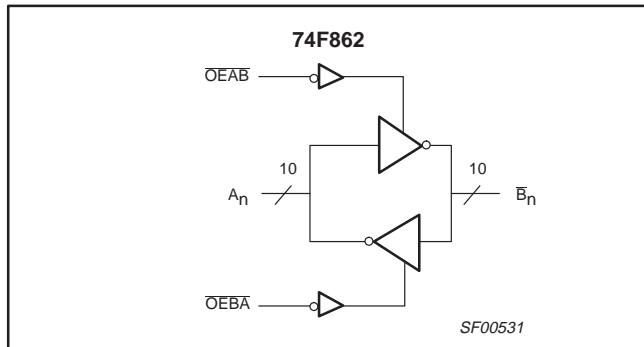
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES
OEAB	OEBA	
L	H	A data to B bus, inverted
H	L	B bus to A data, inverted
H	H	Z

H = HIGH voltage level
 L = LOW voltage level
 Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	-	-	V
V_{IL}	LOW-level input voltage	-	-	0.8	V
I_{IK}	Input clamp current	-	-	-18	mA
I_{OH}	HIGH-level output current	-	-	-24	mA
I_{OL}	LOW-level output current	-	-	64	mA
T_{amb}	Operating free-air temperature range	0	-	70	°C

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT	
					MIN	TYP ²	MAX		
V _{OH}	HIGH-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -1 mA	± 10% V _{CC}	2.4	-	-	V
					± 5% V _{CC}	2.4	3.3	-	V
			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -24 mA	± 10% V _{CC}	2.0	-	-	V
					± 5% V _{CC}	2.0	-	-	V
V _{OL}	LOW-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 48 mA	± 10% V _{CC}	-	0.38	0.55	V
				I _{OL} = 64 mA	± 5% V _{CC}	-	0.42	0.55	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}		-	-0.73	-1.2	V	
I _I	Input current at maximum input voltage	OEAB, OEBA	V _{CC} = 0.0 V, V _I = 7.0 V		-	-	100	μA	
		A _n , B _n	V _{CC} = 5.5 V, V _I = 5.5 V		-	-	1	mA	
I _{IH}	HIGH-level input current		V _{CC} = MAX, V _I = 2.7 V		-	-	20	μA	
I _{IL}	LOW-level input current		V _{CC} = MAX, V _I = 0.5 V		-	-	-20	μA	
I _{IH} + I _{OZH}	Off-state output current HIGH-level voltage applied	A _n , B _n	V _{CC} = MAX, V _O = 2.7 V		-	-	70	μA	
			V _{CC} = MAX, V _O = 0.5 V		-	-	-70	μA	
I _{IL} + I _{OZL}	Off-state output current LOW-level voltage applied	A _n , B _n	V _{CC} = MAX, V _O = 2.7 V		-	-	70	μA	
			V _{CC} = MAX, V _O = 0.5 V		-	-	-70	μA	
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		-100	-	-225	mA	
I _{CC}	Supply current total	I _{CCH}	V _{CC} = MAX		-	90	130	mA	
		I _{CCL}	V _{CC} = MAX		-	120	170	mA	
		I _{CCZ}	V _{CC} = MAX		-	130	160	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

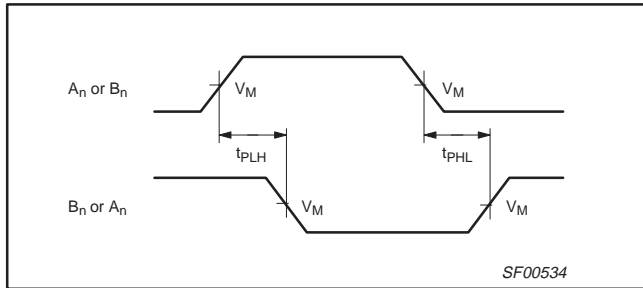
SYMBOL	PARAMETER		TEST CONDITION		LIMITS				UNIT	
					T _{amb} = +25 °C V _{CC} = 5 V C _L = 50 pF; R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = 5 V ± 10% C _L = 50 pF; R _L = 500 Ω		
					MIN	TYP	MAX	MIN		MAX
t _{PLH} t _{PHL}	Propagation delay A _n or B _n		Waveform 1		4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.0 7.0	ns
t _{PLH} t _{PHL}	Propagation delay B _n or A _n		Waveform 1		4.0 1.5	6.0 3.5	9.0 6.5	3.5 1.5	10.0 7.0	ns
t _{PZH} t _{PZL}	Output Enable time HIGH or LOW level OEBA to A _n		Waveform 2 Waveform 3		6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t _{PZH} t _{PZL}	Output Enable time HIGH or LOW level OEAB to B _n		Waveform 2 Waveform 3		6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t _{PHZ} t _{PLZ}	Output Disable time HIGH or LOW level OEBA to A _n		Waveform 2 Waveform 3		3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time HIGH or LOW level OEAB to B _n		Waveform 2 Waveform 3		3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

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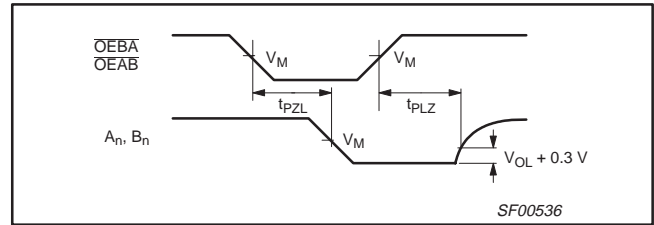
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AC WAVEFORMS

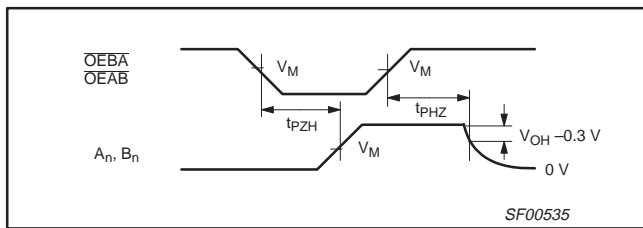
For all waveforms, $V_M = 1.5$ V.



Waveform 1. Propagation delay for inverting output



Waveform 3. 3-State Output Enable time to LOW level and Output Disable time from LOW level



Waveform 2. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

TEST CIRCUITS AND WAVEFORMS

Test Circuit for Open Collector Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

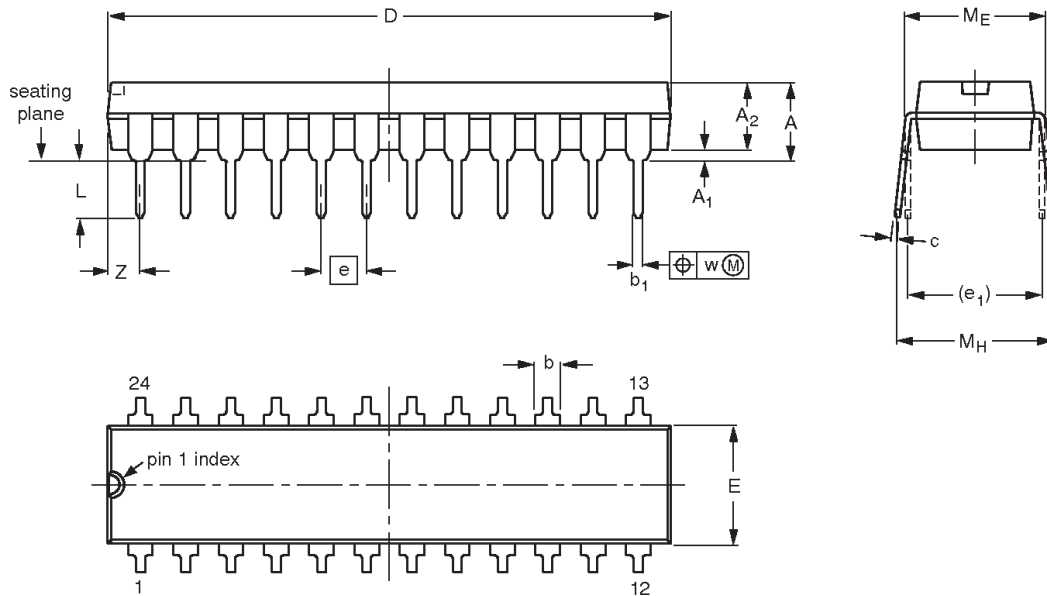
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

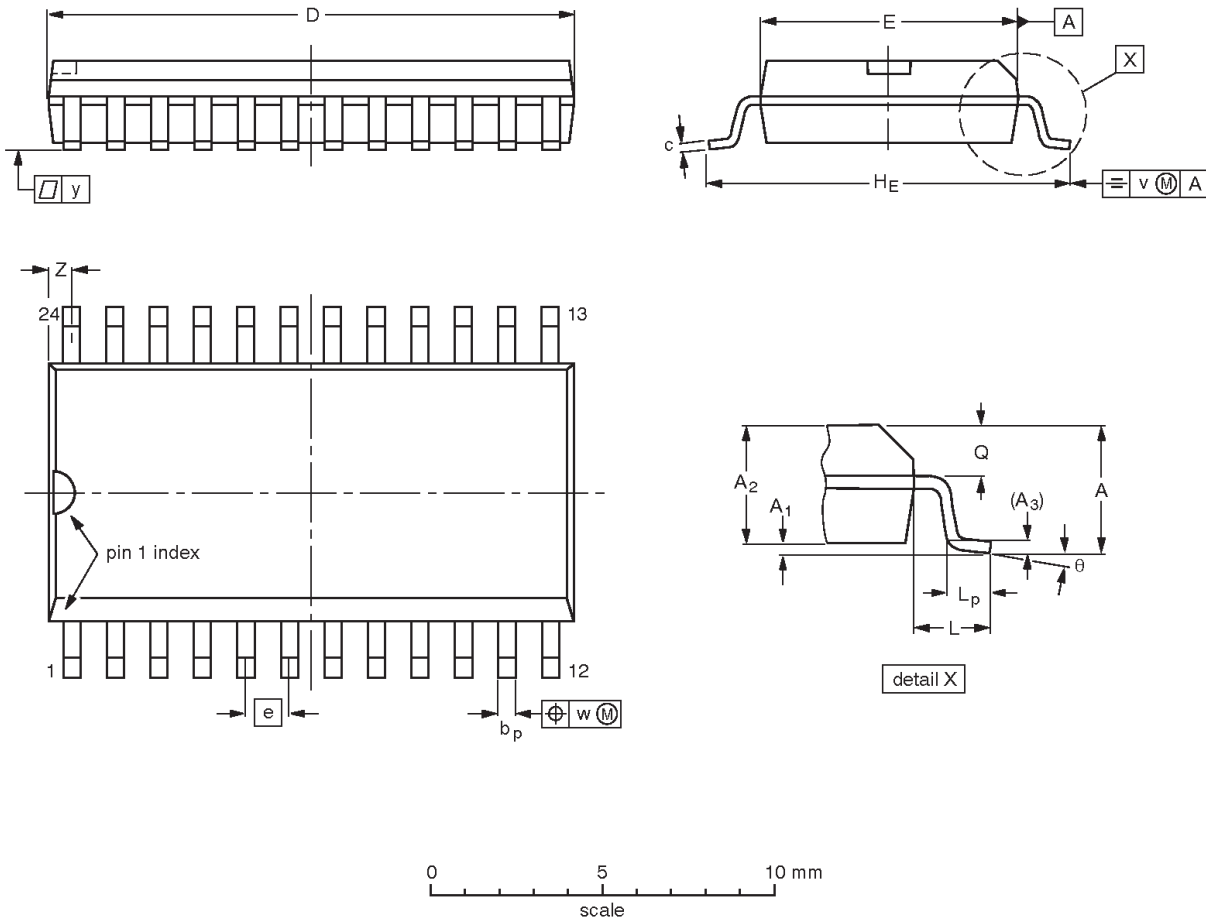
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				99-12-27 03-03-12

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				-99-12-27 03-02-19

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REVISION HISTORY

Rev	Date	Description
_5	20040123	<p>Product data (9397 750 12749). ECN 853-0881 A15378 of 22 January 2004. Replaces Product specification 74F862_74F863_4 dated 2000 Mar 24 (9397 750 06999).</p> <p>Modifications:</p> <ul style="list-style-type: none"> • Delete all references to 74F863 (product discontinued). • "Input and output loading and fan-out table" on page 2; for Pins A0 – A9 and $\bar{B}0$ – $\bar{B}9$: <ul style="list-style-type: none"> – change 74F(U.L.) HIGH/LOW from "3.5/0.117" to "1.0/0.033" – change Load value HIGH/LOW from "70 μA / 70 μA" to "20 μA / 20 μA" • "DC electrical characteristics" table on page 5; V_{OL} test condition, at $\pm 10\%$ V_{CC}: change "$I_{OL} = -48$ mA" to "$I_{OL} = 48$ mA"
_4	20000324	<p>Product specification (9397 750 06999). ECN 853-0881 23378 of 24 March 2000. Supersedes data of 1999 Jan 08.</p>

Bus transceiver, inverting (3-State)

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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