THE DATASHEET OF

74F541SJX

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FAIRCHILD SEMICONDUCTOR™

April 1988
Revised October 2000

74F540 • 74F541
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The 74F540 and 74F541 are similar in function to the 74F240 and 74F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

Features

- 3-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors

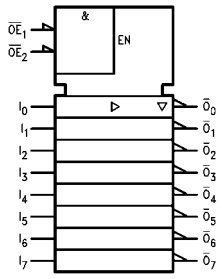
Ordering Code:

Order Number	Package Number	Package Description
74F540SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F540PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

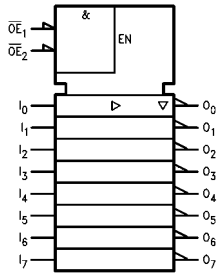
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

IEEE/IEC
74F540

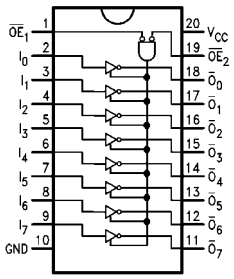


IEEE/IEC
74F541

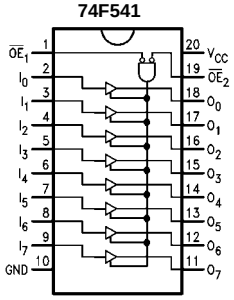


Connection Diagrams

74F540



74F541



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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA
I_n	Inputs	1.0/1.0	20 μA/–0.6 mA
O_n, $\overline{O}_n$	Outputs	600/106.6 (80)	–12 mA/64 mA (48 mA)

Truth Table

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	74F540	74F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

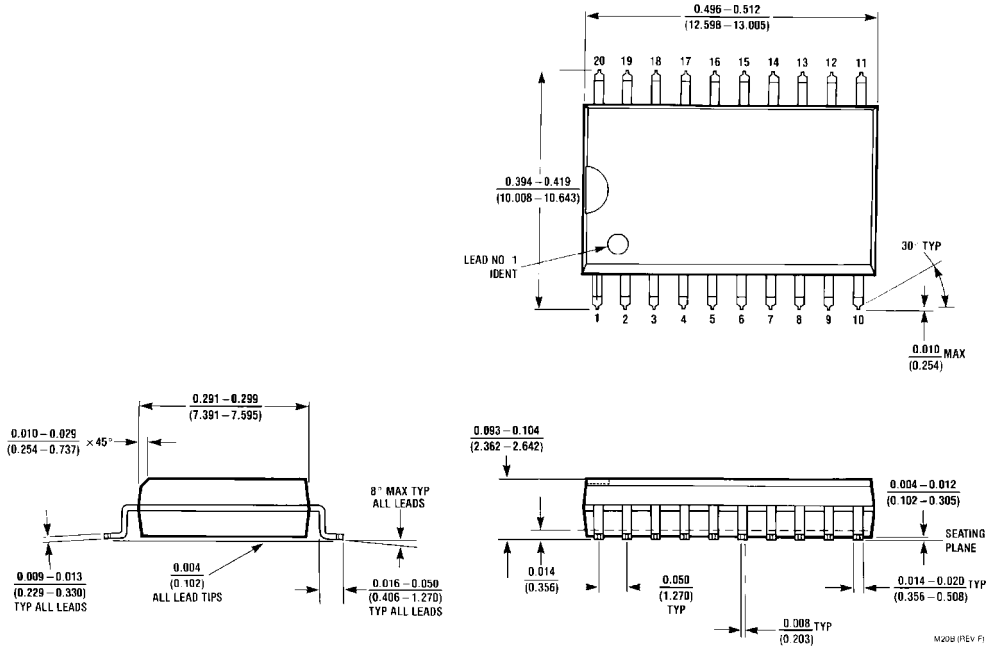
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.4					I_{OH} = −3 mA
	Voltage	10% V_{CC}	2.0			V	Min	I_{OH} = −15 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current (74F540)			11	20	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F540)			53	75	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current (74F540)			31	45	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current (74F541)			26	35	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F541)			55	75	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current (74F541)			31	55	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

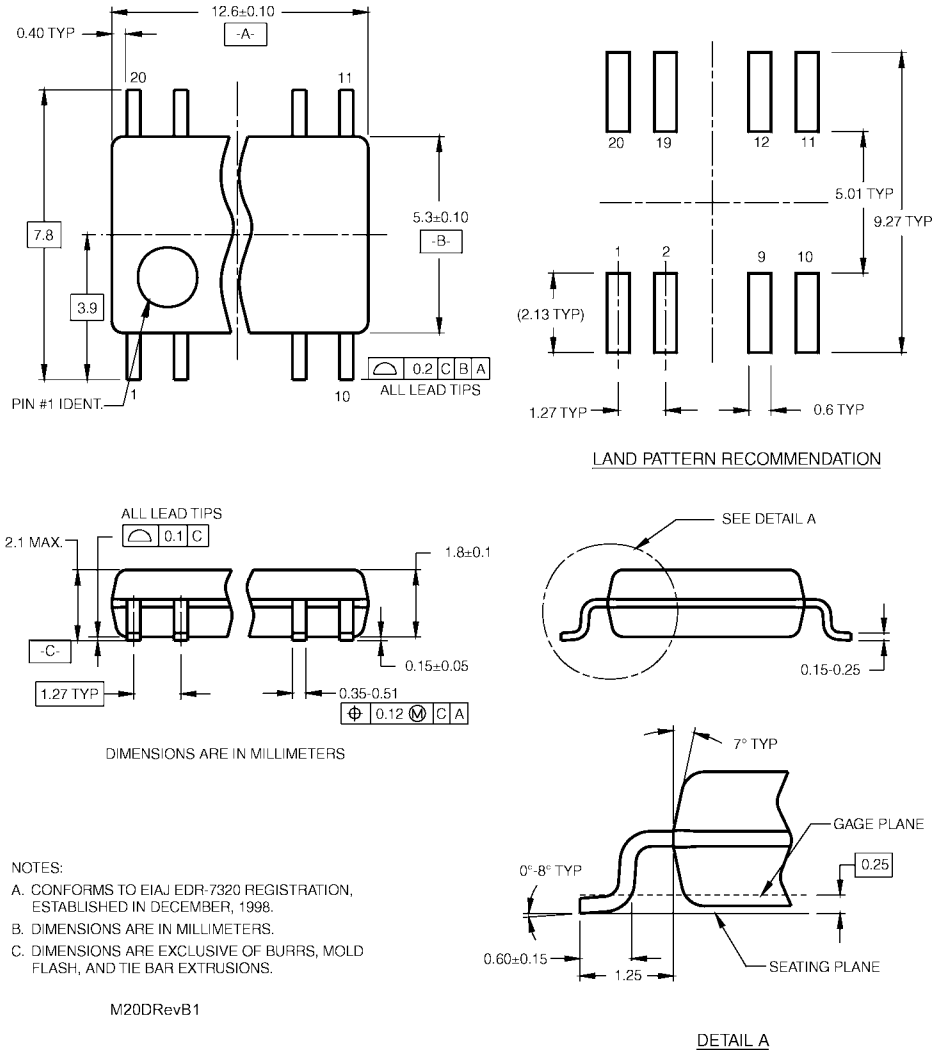
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.0	5.0	1.0	6.0	1.0	5.5	ns
t_{PHL}	Data to Output (74F540)	1.0	2.0	4.0	1.0	4.5	1.0	4.0	
t_{PZH}	Output Enable Time (74F540)	2.5	4.9	8.0	2.5	9.0	2.5	8.5	ns
t_{PZL}		3.5	5.8	10.0	3.5	11.0	3.5	10.5	
t_{PHZ}	Output Disable Time (74F540)	1.5	3.4	6.0	1.5	7.0	1.5	6.5	
t_{PLZ}		1.0	2.5	5.5	1.0	7.5	1.0	6.0	
t_{PLH}	Propagation Delay	1.5	3.3	5.5			1.5	6.0	ns
t_{PHL}	Data to Output (74F541)	1.5	2.7	5.5			1.5	6.0	
t_{PZH}	Output Enable Time (74F541)	3.0	5.8	8.0			2.5	9.5	ns
t_{PZL}		3.5	6.1	8.5			3.0	9.5	
t_{PHZ}	Output Disable Time (74F541)	1.5	3.4	6.0			1.5	6.5	
t_{PLZ}		1.5	2.9	5.5			1.5	6.0	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

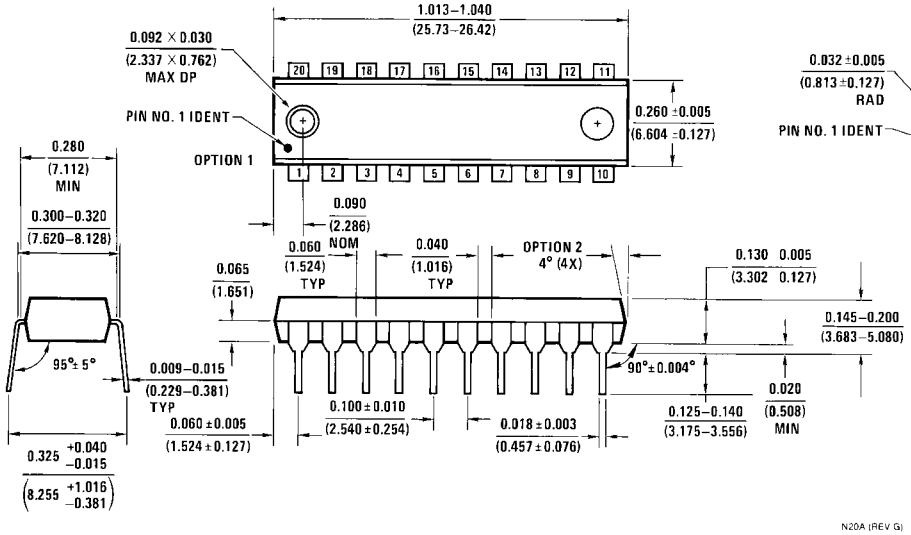
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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