



**THE DATASHEET OF
74F534N**



DATA SHEET

74F534

Octal D flip-flop, inverting (3-State)

Product specification
Supersedes data of 1999 Jan 08
IC15 Data Handbook

2000 Aug 01

Octal D flip-flop, inverting (3-State)

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FEATURES

- 8-bit positive edge-triggered register
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's \overline{Q} output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

active Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|-------------------|--------------------------------|
| 74F534 | 165MHz | 51mA |

ORDERING INFORMATION

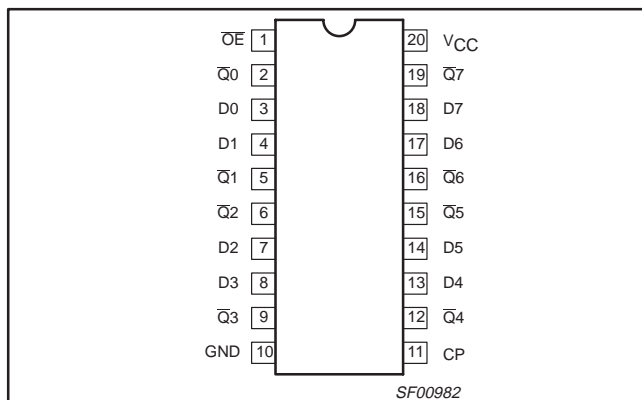
| DESCRIPTION | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | PKG DWG # |
|--------------------|--|-----------|
| 20-Pin Plastic DIP | N74F534N | SOT146-1 |
| 20-Pin Plastic SOL | N74F534D | SOT163-1 |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

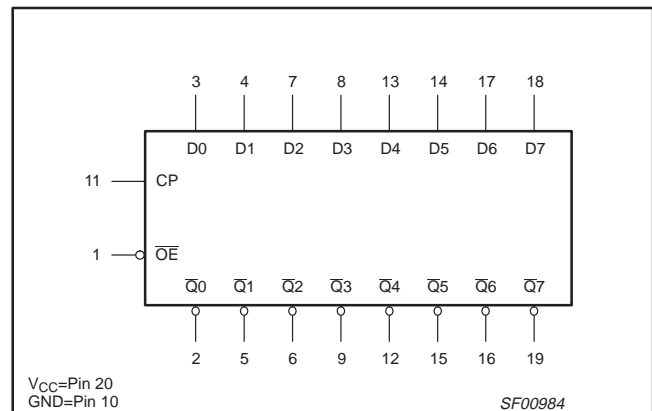
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---------------------------------|--|---------------------|---------------------|
| D0 - D7 | Data inputs | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{OE} | Output Enable input (active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| CP | Clock Pulse input (active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| $\overline{Q}0 - \overline{Q}7$ | Data outputs | 150/40 | 3.0mA/24mA |

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



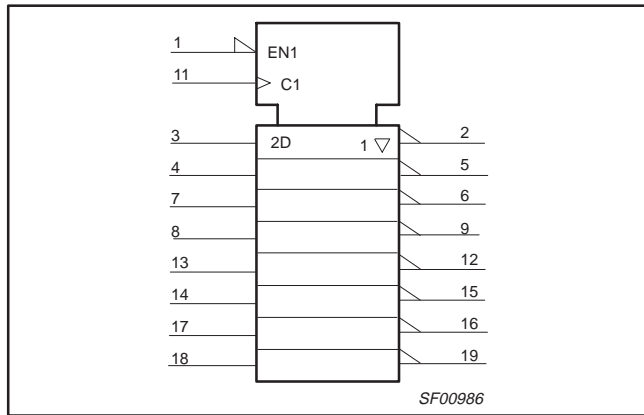
LOGIC SYMBOL



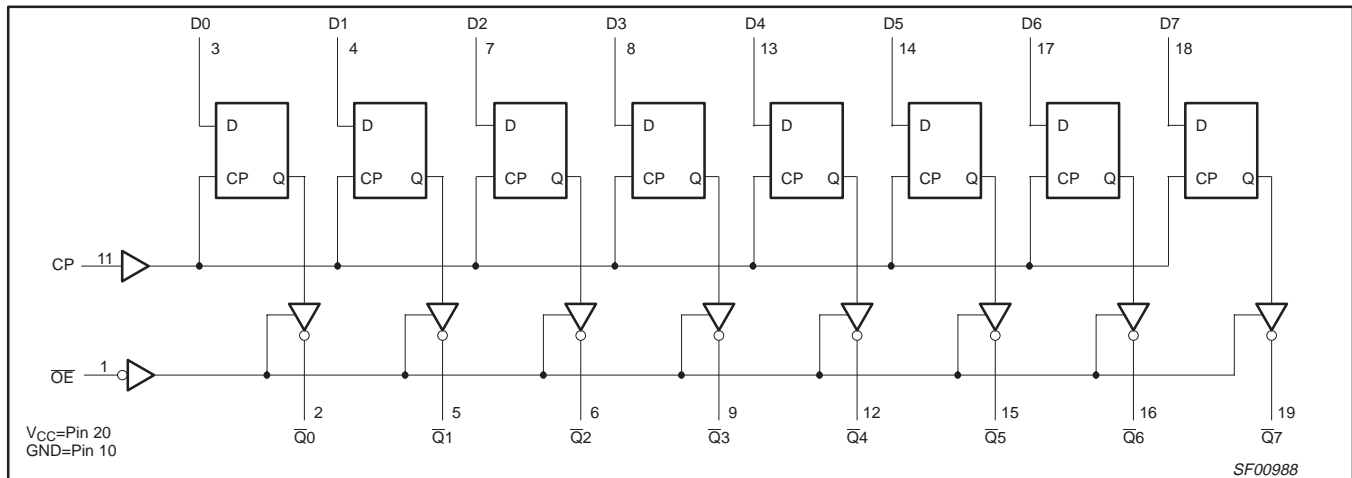
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LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODES |
|-----------------|------------|----|-------------------|---------------------------------|------------------------|
| \overline{OE} | CP | Dn | | $\overline{Q0} - \overline{Q7}$ | |
| L | \uparrow | l | L | H | Load and read register |
| L | \uparrow | h | H | L | |
| L | ∇ | X | NC | NC | Hold |
| H | ∇ | X | NC | Z | Disable outputs |
| H | \uparrow | Dn | Dn | Z | |

- H = High voltage level
- h = High voltage level one setup time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the Low-to-High clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- \uparrow = Low-to-High clock transition
- ∇ = Not a Low-to-High clock transition

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|-----------|--|-------------------|------|
| V_{CC} | Supply voltage | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | V |
| I_{IN} | Input current | -30 to +5.0 | mA |
| V_{OUT} | Voltage applied to output in High output state | -0.5 to $+V_{CC}$ | V |
| I_{OUT} | Current applied to output in Low output state | 48 | mA |
| T_{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T_{stg} | Storage temperature | -65 to +125 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|--------|-----|-----|------|
| | | MIN | TYP | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -3 | mA |
| I_{OL} | Low-level output current | | | 24 | mA |
| T_{amb} | Operating free-air temperature range | 0 | | 70 | °C |

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|------------------|--|---|---------------------|------------------|------|------|---|
| | | | MIN | TYP ² | MAX | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX | ±10%V _{CC} | 2.4 | | V | |
| | | | ±5%V _{CC} | 2.7 | 3.3 | V | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX | ±10%V _{CC} | | 0.35 | 0.50 | V |
| | | | ±5%V _{CC} | | 0.35 | 0.50 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | -0.73 | -1.2 | V | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7.0V | | | 100 | μA | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7V | | | 20 | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.5V | | | -0.6 | mA | |
| I _{OZH} | Off-state output current, High-level voltage applied | V _{CC} = MAX, V _O = 2.7V | | | 50 | μA | |
| I _{OZL} | Off-state output current, Low-level voltage applied | V _{CC} = MAX, V _O = 0.5V | | | -50 | μA | |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | -60 | | -150 | mA | |
| I _{CC} | Supply current (total) | V _{CC} = MAX, \overline{OE} =4.5V, Dn=GND | | 51 | 86 | mA | |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | UNIT | |
|--------------------------------------|---|--------------------------|---|------------|------------|--|------------|-----|
| | | | T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | | MAX |
| f _{MAX} | Maximum Clock frequency | Waveform 1 | 150 | 165 | | 135 | MHz | |
| t _{PLH} t _{PHL} | Propagation delay CP to Qn | Waveform 1 | 3.0 3.0 | 4.5 4.5 | 7.0 7.0 | 2.5 2.5 | 7.5 7.5 | ns |
| t _{PZH} t _{PZL} | Output Enable time to High or Low level | Waveform 3 Waveform 4 | 2.0 2.0 | 4.5 5.0 | 7.5 7.5 | 2.0 2.0 | 8.5 8.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable time from High or Low level | Waveform 3 Waveform 4 | 2.0 2.0 | 3.5 3.5 | 6.5 5.5 | 2.0 2.0 | 7.5 6.5 | ns |

AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | UNIT | |
|--|--------------------------------|-----------------|---|-----|-----|--|------|-----|
| | | | T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | | MAX |
| t _s (H) t _s (L) | Setup time, Dn to CP | Waveform 2 | 2.0 2.0 | | | 2.5 2.5 | ns | |
| t _h (H) t _h (L) | Hold time, Dn to CP | Waveform 2 | 0 0 | | | 0 0 | ns | |
| t _w (H) t _w (L) | CP pulse width, High or Low | Waveform 1 | 3.0 3.5 | | | 3.5 4.0 | ns | |

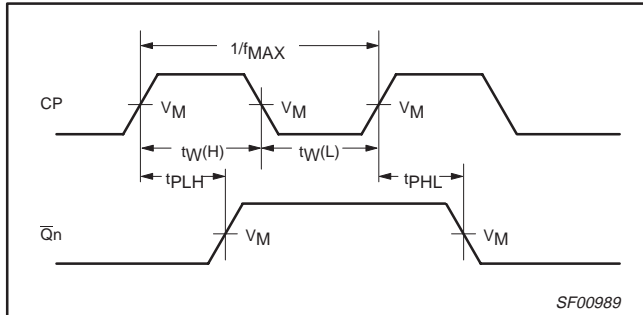
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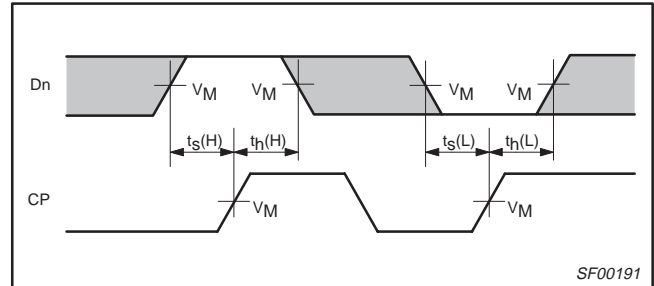
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

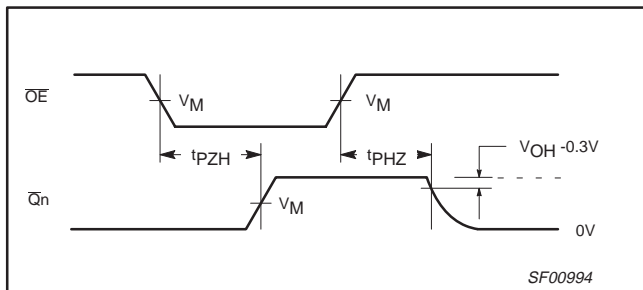
The shaded areas indicate when the input is permitted to change for predictable output performance.



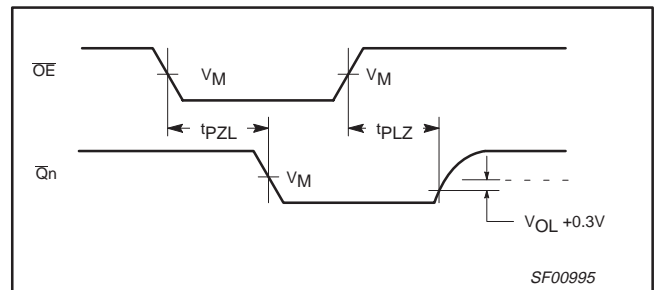
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

| SWITCH POSITION | |
|-----------------|--------|
| TEST | SWITCH |
| t_{pLZ} | closed |
| t_{pZL} | closed |
| All other | open |

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

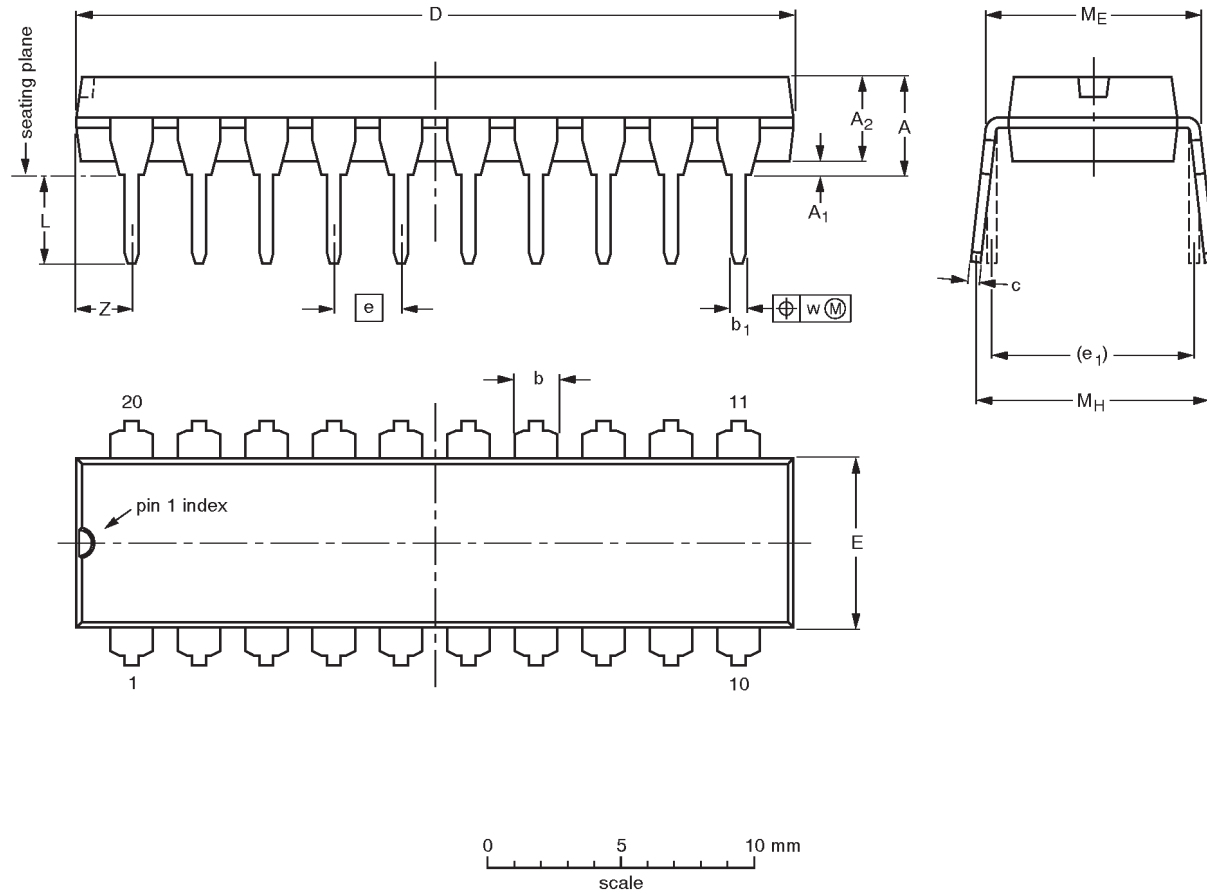
SF00777

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 0.36 0.23 | 26.92 26.54 | 6.40 6.22 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.0 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.014 0.009 | 1.060 1.045 | 0.25 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.078 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

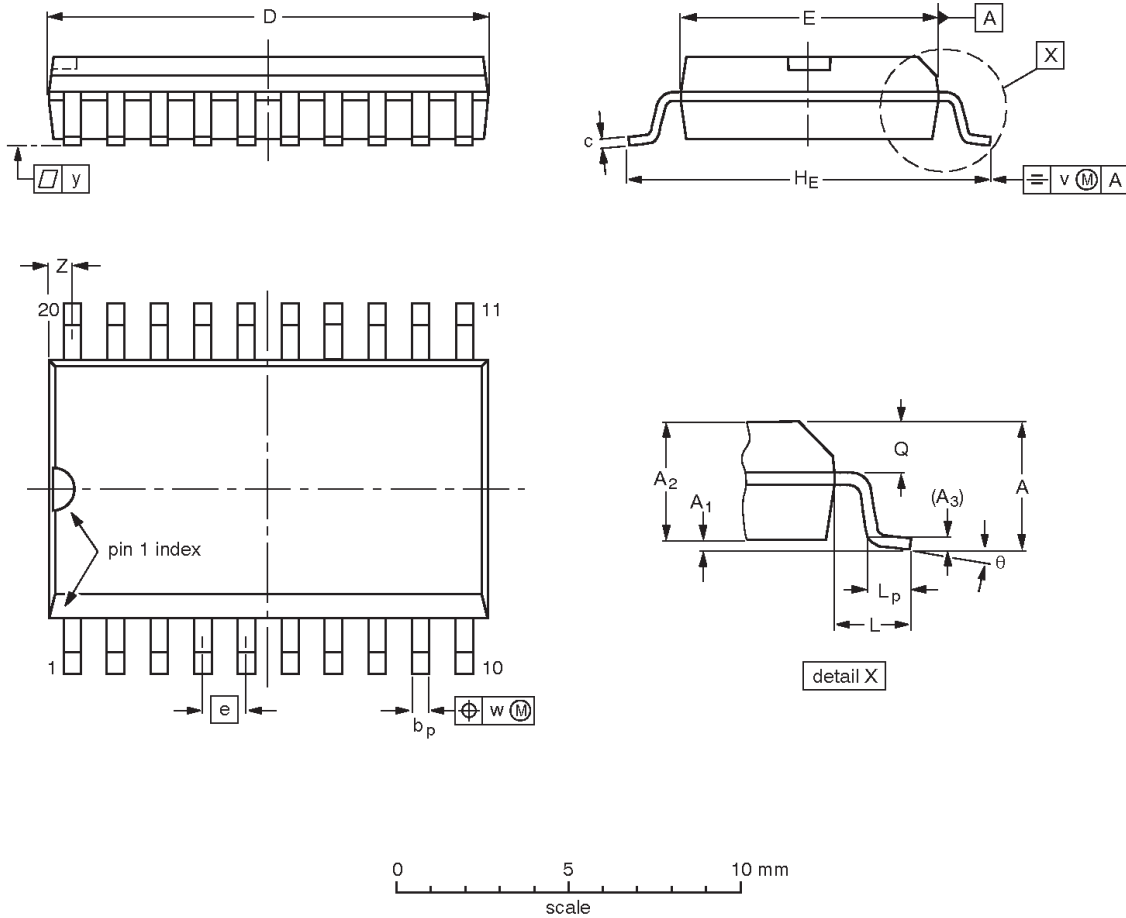
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT146-1 | | | SC603 | | | 92-11-17 95-05-24 |

Octal D flip-flop, inverting (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | 95-01-24 97-05-22 |

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NOTES

Octal D flip-flop, inverting (3-State)

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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