



**THE DATASHEET OF
74AVCH20T245DGV:11**



Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

74AVCH20T245

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 5 — 23 February 2016

Product data sheet

1. General description

The 74AVCH20T245 is a 20-bit, dual supply transceiver that enables bi-directional voltage level translation. The device can be used as two 10-bit transceivers or as a single 20-bit transceiver. It features four 10-bit input-output ports (1An, 1Bn and 2An, 2Bn), two output enable inputs ($\overline{\text{nOE}}$), two direction inputs ($\overline{\text{nDIR}}$) and dual supplies ($V_{\text{CC(A)}}$ and $V_{\text{CC(B)}}$). $V_{\text{CC(A)}}$ and $V_{\text{CC(B)}}$ can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for bi-directional voltage level translation between any of the low voltage nodes: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. The 1An and 2An ports, $\overline{\text{nOE}}$ and $\overline{\text{nDIR}}$ are referenced to $V_{\text{CC(A)}}$, the 1Bn and 2Bn ports are referenced to $V_{\text{CC(B)}}$. A HIGH on a 1DIR allows transmission from 1An to 1Bn and a LOW on 1DIR allows transmission from 1Bn to 1An. A HIGH on $\overline{\text{nOE}}$ causes the outputs to assume a HIGH impedance OFF-state.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{\text{CC(A)}}$ or $V_{\text{CC(B)}}$ are at GND level, all output ports will assume a high impedance OFF-state. The bus hold circuitry on the powered-up side always stays active.

The 74AVCH20T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range:
 - ◆ $V_{\text{CC(A)}}$: 0.8 V to 3.6 V
 - ◆ $V_{\text{CC(B)}}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:



- ◆ 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
- ◆ 260 Mbit/s (≥ 1.1 V to 3.3 V translation)
- ◆ 260 Mbit/s (≥ 1.1 V to 2.5 V translation)
- ◆ 210 Mbit/s (≥ 1.1 V to 1.8 V translation)
- ◆ 120 Mbit/s (≥ 1.1 V to 1.5 V translation)
- ◆ 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVCH20T245DGG	-40 °C to $+125$ °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
74AVCH20T245DGV	-40 °C to $+125$ °C	TSSOP56 ^[1]	plastic thin shrink small outline package; 56 leads; body width 4.4 mm	SOT481-2
74AVCH20T245BX	-40 °C to $+125$ °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body $4 \times 6 \times 0.5$ mm	SOT1134-1

[1] Also known as TVSOP56.

4. Functional diagram

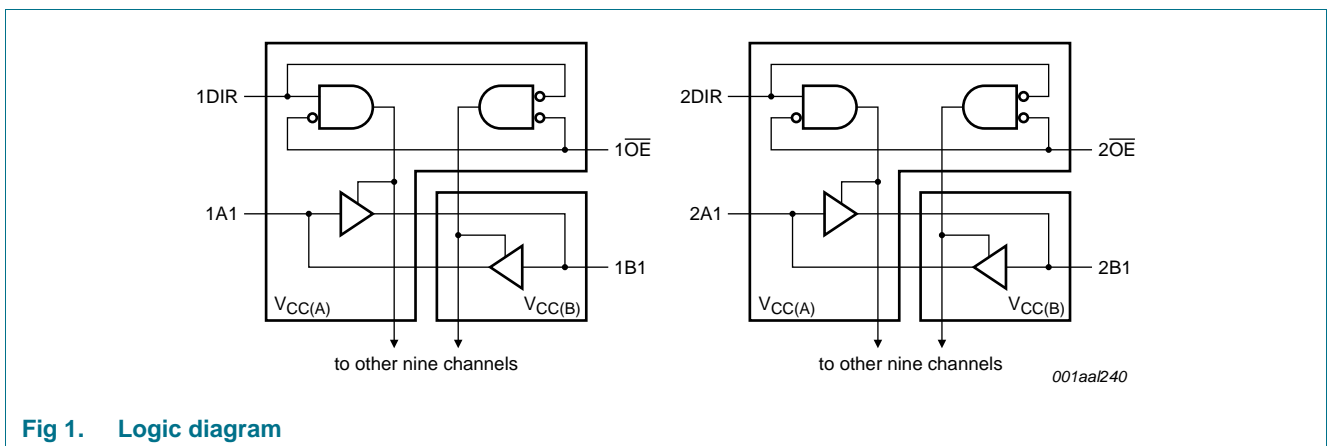


Fig 1. Logic diagram

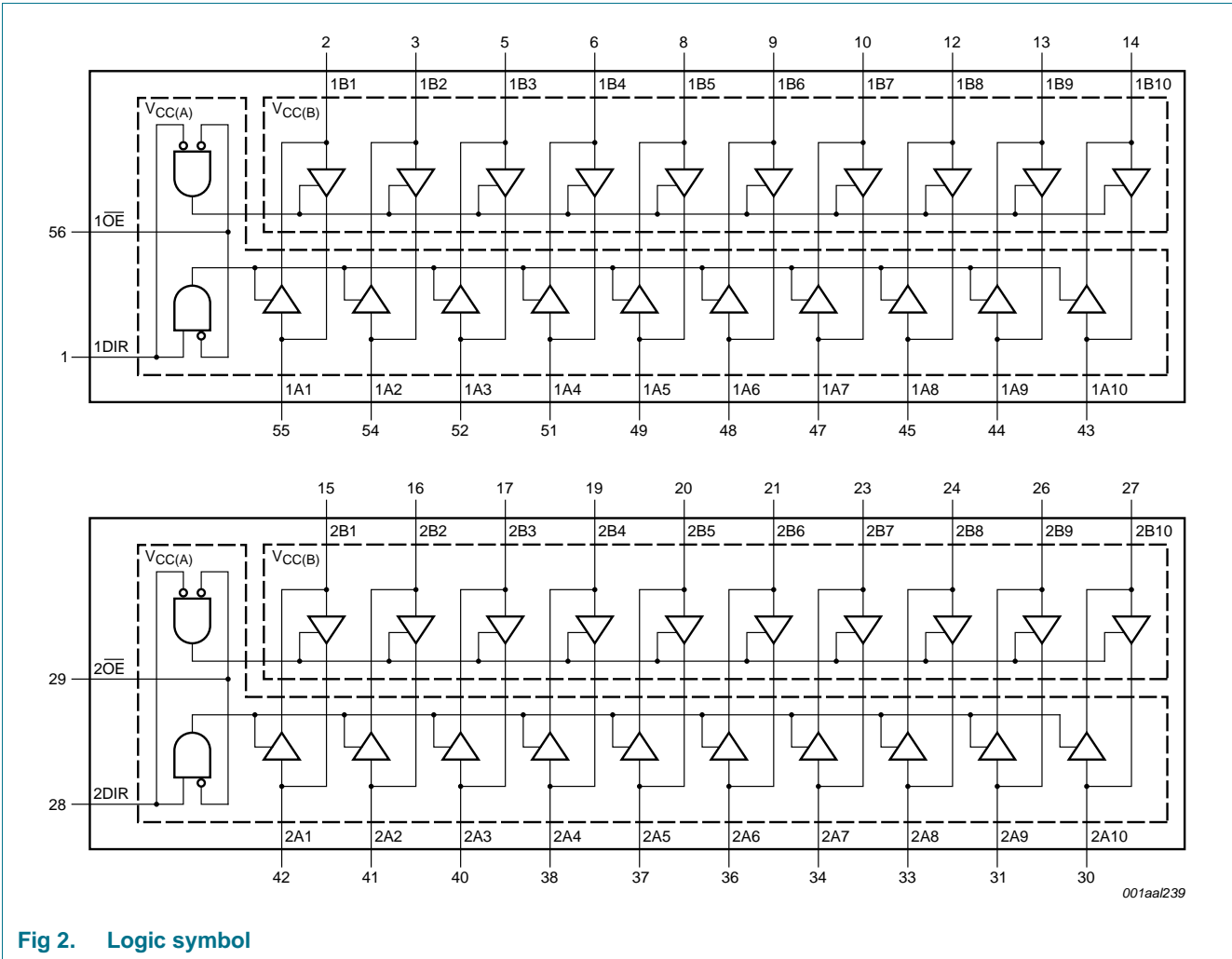


Fig 2. Logic symbol

5. Pinning information

5.1 Pinning

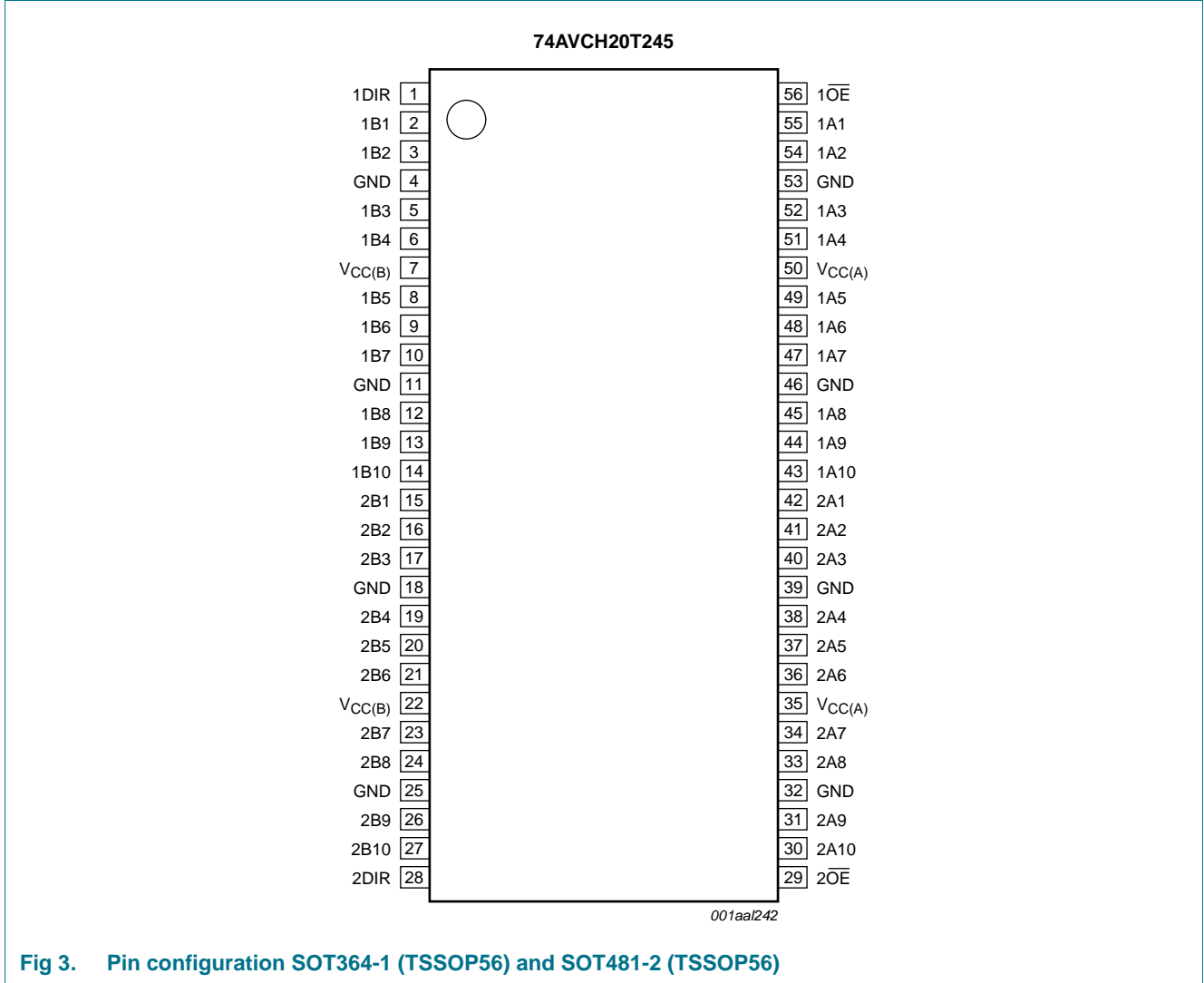
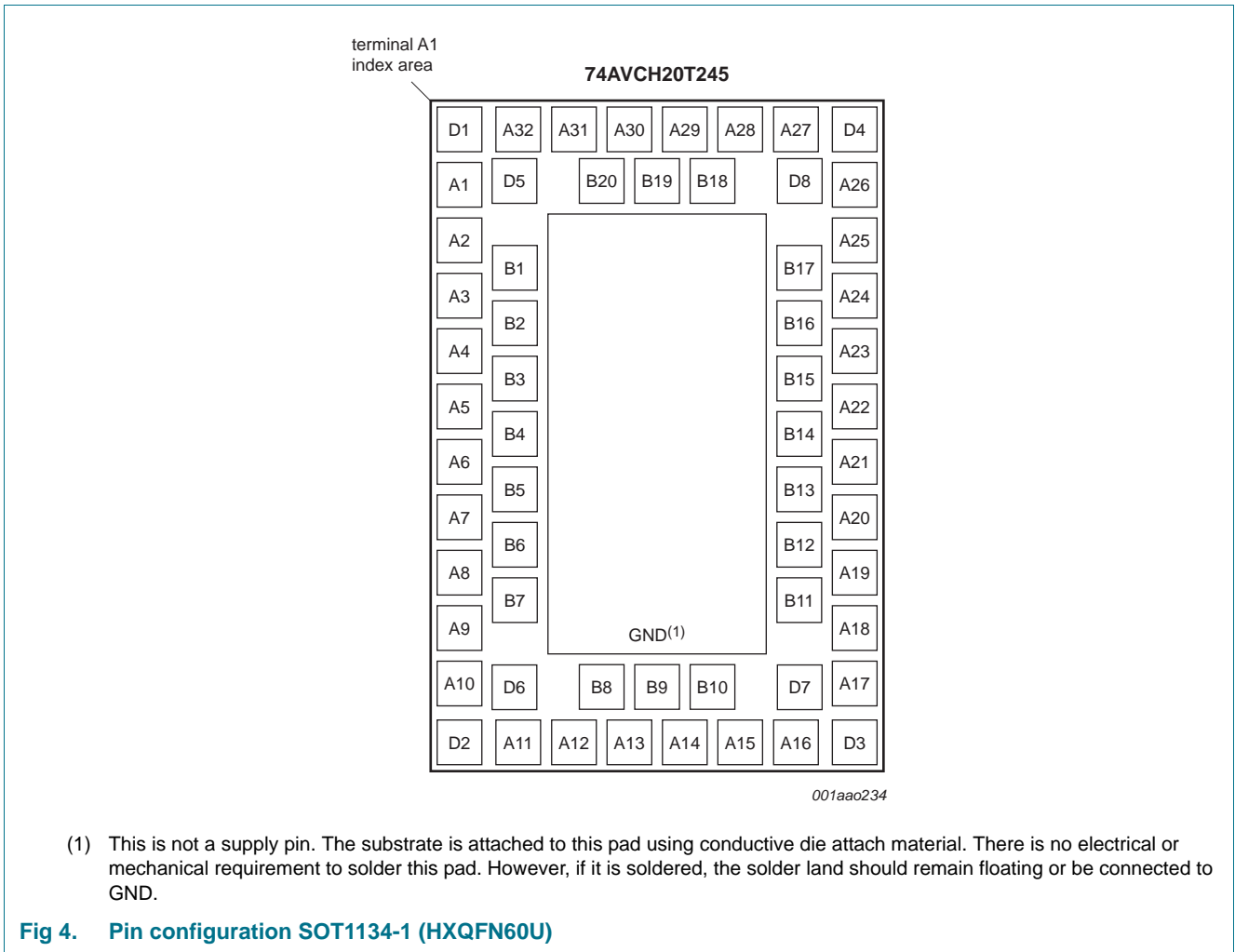


Fig 3. Pin configuration SOT364-1 (TSSOP56) and SOT481-2 (TSSOP56)



5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT364-1 and SOT481-2	SOT1134-1	
1DIR, 2DIR	1, 28	A30, A13	direction control
1B1 to 1B10	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	B20, A31, D5, D1, B1, A2, B2, A4, B3, A5	data input or output
2B1 to 2B10	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	A6, B5, A7, B6, A9, B7, D2, D6, A12, B8	data input or output
GND ^[1]	4, 11, 18, 25, 32, 39, 46, 53	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V _{CC(B)}	7, 22	A1, A10	supply voltage B (nBn inputs are referenced to V _{CC(B)})
$\overline{1OE}$, $\overline{2OE}$	56, 29	A29, A14	output enable input (active LOW)
1A1 to 1A10	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	B18, A28, D8, D4, B17, A25, B16, A23, B15, A22	data input or output
2A1 to 2A10	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	A21, B13, A20, B12, A18, B11, D3, D7, A15, B10	data input or output
V _{CC(A)}	35, 50	A17, A26	supply voltage A (nAn, \overline{nOE} and nDIR inputs are referenced to V _{CC(A)})
n.c.	-	B4, B9, B14, B19	not connected

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table^[1]

Supply voltage	Input		Input/output ^[2]	
	nOE ^[3]	nDIR ^[3]	nAn ^[3]	nBn ^[3]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND ^[2]	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] If at least one of V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into suspend mode.

[3] The nAn, nDIR and nOE input circuit is referenced to V_{CC(A)}; The nBn input circuit is referenced to V_{CC(B)}.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO}	-	± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		TSSOP56 package	-	600	mW
		HXQFN60U package	-	1000	mW

- [1] The minimum input and minimum output voltage ratings may be exceeded if the input and output clamping current ratings are observed.
- [2] V_{CCO} is the supply voltage associated with the output port.
- [3] $V_{CCO} + 0.5$ V should not exceed 4.6 V.
- [4] Above 55 °C the value of P_{tot} derates linearly with 8.0 mW/K.
- [5] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CCO}	V
		Suspend or 3-state mode	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	-	5	ns/V

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -1.5\text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 1.5\text{ mA}$; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V	
I_I	input leakage current	nDIR, nOE input; $V_I = 0\text{ V}$ or 3.6 V ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	± 0.025	± 0.25	μA	
I_{BHL}	bus hold LOW current	A or B port; $V_I = 0.42\text{ V}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$	[3]	26	-	μA	
I_{BHH}	bus hold HIGH current	A or B port; $V_I = 0.78\text{ V}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$	[4]	-24	-	μA	
I_{BHLO}	bus hold LOW overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$	[5]	27	-	μA	
I_{BHHO}	bus hold HIGH overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$	[6]	-26	-	μA	
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$	[7]	-	± 0.5	± 2.5	μA
		suspend mode A port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$	[7]	-	± 0.5	± 2.5	μA
		suspend mode B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 3.6\text{ V}$	[7]	-	± 0.5	± 2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V		-	± 0.1	± 1	μA
		B port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 0.8\text{ V}$ to 3.6 V		-	± 0.1	± 1	μA
C_I	input capacitance	nDIR, nOE input; $V_I = 0\text{ V}$ or 3.3 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$		2.0	-	pF	
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or 0 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$		4.0	-	pF	

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.

[4] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.

[5] An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.

[6] An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 7. Static characteristics [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	data input					
		V _{CCI} = 0.8 V	0.70V _{CCI}	-	0.70V _{CCI}	-	V
		V _{CCI} = 1.1 V to 1.95 V	0.65V _{CCI}	-	0.65V _{CCI}	-	V
		V _{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, n $\overline{\text{OE}}$ input					
		V _{CC(A)} = 0.8 V	0.70V _{CC(A)}	-	0.70V _{CC(A)}	-	V
		V _{CC(A)} = 1.1 V to 1.95 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
V _{IL}	LOW-level input voltage	data input					
		V _{CCI} = 0.8 V	-	0.30V _{CCI}	-	0.30V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n $\overline{\text{OE}}$ input					
		V _{CC(A)} = 0.8 V	-	0.30V _{CC(A)}	-	0.30V _{CC(A)}	V
		V _{CC(A)} = 1.1 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = -6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = -8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = -9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
		I _O = -12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	2.3	-	2.3	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
		I _O = 12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	-	0.7	-	0.7	V
I _I	input leakage current	nDIR, n $\overline{\text{OE}}$ input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	\pm 1	-	\pm 5	μ A

Table 7. Static characteristics ...continued [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{BHL}	bus hold LOW current	A or B port [3]					
		V _I = 0.49 V; V _{CC(A)} = V _{CC(B)} = 1.4 V	15	-	15	-	μA
		V _I = 0.58 V; V _{CC(A)} = V _{CC(B)} = 1.65 V	25	-	25	-	μA
		V _I = 0.70 V; V _{CC(A)} = V _{CC(B)} = 2.3 V	45	-	45	-	μA
		V _I = 0.80 V; V _{CC(A)} = V _{CC(B)} = 3.0 V	100	-	90	-	μA
I _{BHH}	bus hold HIGH current	A or B port [4]					
		V _I = 0.91 V; V _{CC(A)} = V _{CC(B)} = 1.4 V	-15	-	-15	-	μA
		V _I = 1.07 V; V _{CC(A)} = V _{CC(B)} = 1.65 V	-25	-	-25	-	μA
		V _I = 1.60 V; V _{CC(A)} = V _{CC(B)} = 2.3 V	-45	-	-45	-	μA
		V _I = 2.00 V; V _{CC(A)} = V _{CC(B)} = 3.0 V	-100	-	-100	-	μA
I _{BHLO}	bus hold LOW overdrive current	A or B port [5]					
		V _{CC(A)} = V _{CC(B)} = 1.6 V	125	-	125	-	μA
		V _{CC(A)} = V _{CC(B)} = 1.95 V	200	-	200	-	μA
		V _{CC(A)} = V _{CC(B)} = 2.7 V	300	-	300	-	μA
		V _{CC(A)} = V _{CC(B)} = 3.6 V	500	-	500	-	μA
I _{BHHO}	bus hold HIGH overdrive current	A or B port [6]					
		V _{CC(A)} = V _{CC(B)} = 1.6 V	-125	-	-125	-	μA
		V _{CC(A)} = V _{CC(B)} = 1.95 V	-200	-	-200	-	μA
		V _{CC(A)} = V _{CC(B)} = 2.7 V	-300	-	-300	-	μA
		V _{CC(A)} = V _{CC(B)} = 3.6 V	-500	-	-500	-	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V [7]	-	±5	-	±30	μA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V [7]	-	±5	-	±30	μA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V [7]	-	±5	-	±30	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	±5	-	±30	μA

Table 7. Static characteristics ...continued^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	45	-	190	μA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	35	-	140	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	35	-	140	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-5	-	-20	-	μA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	45	-	190	μA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	35	-	140	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-5	-	-20	-	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-	35	-	140	μA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	80	-	270	μA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	65	-	220	μA

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.
- [5] An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Typical total supply current (I_{CC(A)} + I_{CC(B)})

V _{CC(A)}	V _{CC(B)}							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

10. Dynamic characteristics

Table 9. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$ [1][2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C _{PD}	power dissipation capacitance	A port: (direction A to B); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction A to B); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction B to A); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction B to A); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction A to B); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction A to B); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction B to A); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction B to A); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

[2] f_i = 10 MHz; V_i = GND to V_{CC}; t_r = t_f = 1 ns; C_L = 0 pF; R_L = ∞ Ω.

Table 10. Typical dynamic characteristics at $V_{CC(A)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
t_{dis}	disable time	\overline{nOE} to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		\overline{nOE} to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
t_{en}	enable time	\overline{nOE} to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		\overline{nOE} to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 11. Typical dynamic characteristics at $V_{CC(B)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
t_{dis}	disable time	\overline{nOE} to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		\overline{nOE} to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
t_{en}	enable time	\overline{nOE} to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		\overline{nOE} to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.7	1.5	9.8	1.5	9.6	1.0	8.1	1.0	9.0	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	ns
		n $\overline{\text{OE}}$ to nBn	1.0	15.6	1.0	11.5	1.0	10.0	0.5	8.4	0.5	8.0	ns
V_{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.9	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	7.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.7	1.5	9.0	1.5	7.8	1.0	6.4	1.0	6.0	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.5	10.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.3	1.0	10.3	1.0	8.4	0.5	6.1	0.5	5.3	ns
V_{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.7	0.5	6.1	0.5	5.0	0.5	3.9	0.5	3.5	ns
		nBn to nAn	0.5	6.2	0.5	5.4	0.5	5.0	0.5	4.7	0.5	4.6	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.3	1.5	8.7	1.5	7.4	1.0	5.8	1.0	5.6	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.1	1.0	8.1	1.0	7.9	1.0	7.9	1.0	7.9	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.8	0.5	10.0	0.5	7.9	0.5	5.7	0.5	4.8	ns
V_{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.4	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3.0	ns
		nBn to nAn	0.5	5.2	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns
		n $\overline{\text{OE}}$ to nBn	1.2	10.8	1.2	8.2	1.2	6.9	1.0	5.3	1.0	5.2	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.4	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.3	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns
V_{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.2	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns
		nBn to nAn	0.5	5.1	0.5	3.9	0.5	3.5	0.5	3.0	0.5	2.9	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	ns
		n $\overline{\text{OE}}$ to nBn	1.2	10.5	1.2	8.1	1.2	6.7	1.0	5.1	0.8	5.0	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.4	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.1	1.0	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

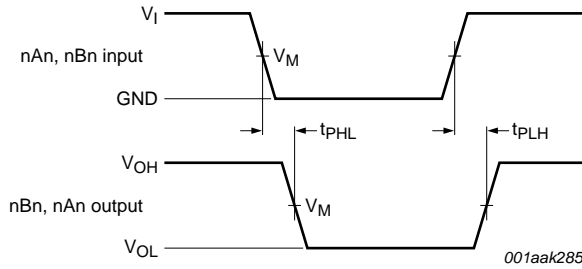
Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	14.0	1.5	10.8	1.5	10.6	1.0	9.0	1.0	9.9	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	ns
		n $\overline{\text{OE}}$ to nBn	1.0	17.2	1.0	12.7	1.0	11.0	0.5	9.3	0.5	8.8	ns
V_{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.8	0.5	7.1	0.5	6.0	0.5	4.8	0.5	4.3	ns
		nBn to nAn	0.5	7.9	0.5	7.1	0.5	6.8	0.5	6.4	0.5	6.3	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.9	1.5	9.9	1.5	8.6	1.0	7.1	1.0	6.6	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.5	11.4	1.5	11.4	1.5	11.4	1.5	11.3	1.5	11.3	ns
		n $\overline{\text{OE}}$ to nBn	1.0	15.8	1.0	11.4	1.0	9.3	0.5	6.8	0.5	5.9	ns
V_{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.6	0.5	6.8	0.5	5.5	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	6.9	0.5	6.0	0.5	5.5	0.5	5.2	0.5	5.1	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.6	1.5	8.2	1.0	6.4	1.0	6.2	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	9.0	1.0	9.0	1.0	8.7	1.0	8.7	1.0	8.7	ns
		n $\overline{\text{OE}}$ to nBn	0.5	15.2	0.5	11.0	0.5	8.7	0.5	6.3	0.5	5.3	ns
V_{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.3	0.5	6.4	0.5	5.2	0.5	3.9	0.5	3.3	ns
		nBn to nAn	0.5	5.8	0.5	4.8	0.5	4.3	0.5	3.9	0.5	3.8	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	ns
		n $\overline{\text{OE}}$ to nBn	1.2	11.9	1.2	9.1	1.2	7.6	1.0	5.9	1.0	5.8	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	6.0	0.5	6.0	0.5	5.9	0.5	5.8	0.5	5.8	ns
		n $\overline{\text{OE}}$ to nBn	0.5	14.7	0.5	10.6	0.5	8.4	0.5	5.9	0.5	4.8	ns
V_{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.1	0.5	6.3	0.5	5.1	0.5	3.8	0.5	3.2	ns
		nBn to nAn	0.5	5.7	0.5	4.3	0.5	3.9	0.5	3.3	0.5	3.2	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	ns
		n $\overline{\text{OE}}$ to nBn	1.2	11.6	1.2	9.0	1.2	7.4	1.0	5.7	0.8	5.5	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.9	0.5	4.9	0.5	4.8	0.5	4.7	0.5	4.6	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.5	1.0	10.6	0.5	8.3	0.5	5.7	0.5	4.6	ns

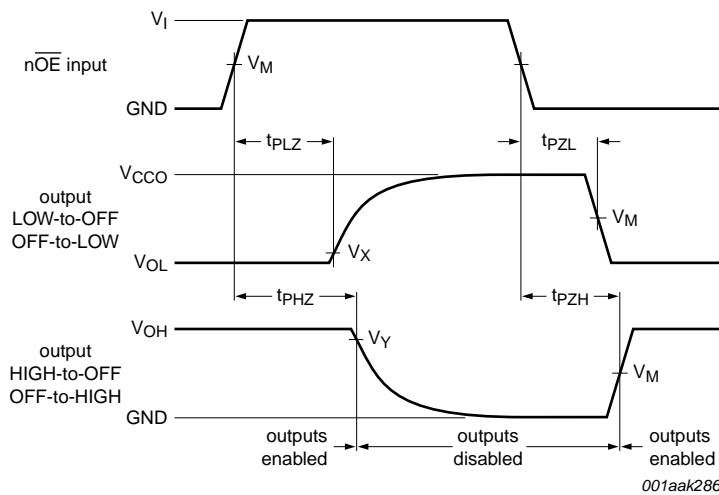
[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

11. Waveforms



Measurement points are given in [Table 14](#).
 VOL and VOH are typical output voltage levels that occur with the output load.

Fig 5. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



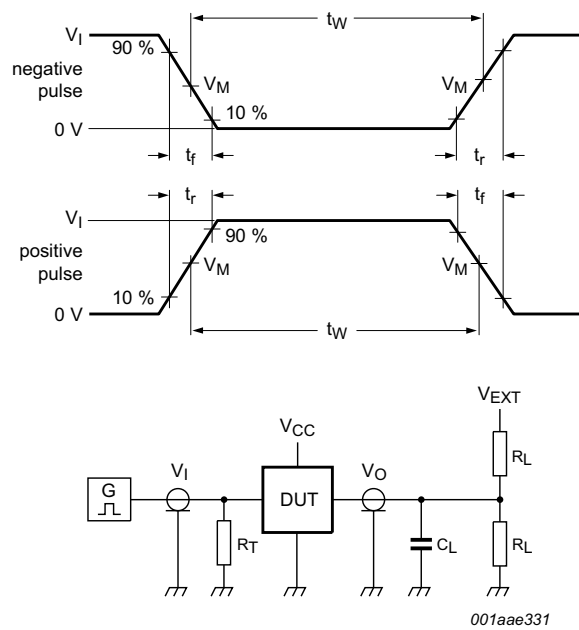
Measurement points are given in [Table 14](#).
 VOL and VOH are typical output voltage levels that occur with the output load.

Fig 6. Enable and disable times

Table 14. Measurement points

Supply voltage	Input ^[1]	Output ^[2]		
V _{CC(A)} , V _{CC(B)}	V _M	V _M	V _X	V _Y
0.8 V to 1.6 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.1 V	V _{OH} - 0.1 V
1.65 V to 2.7 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
3.0 V to 3.6 V	0.5V _{CCI}	0.5V _{CCO}	V _{OL} + 0.3 V	V _{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.
 [2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 15](#).
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance.
 V_{EXT} = External voltage for measuring switching times.

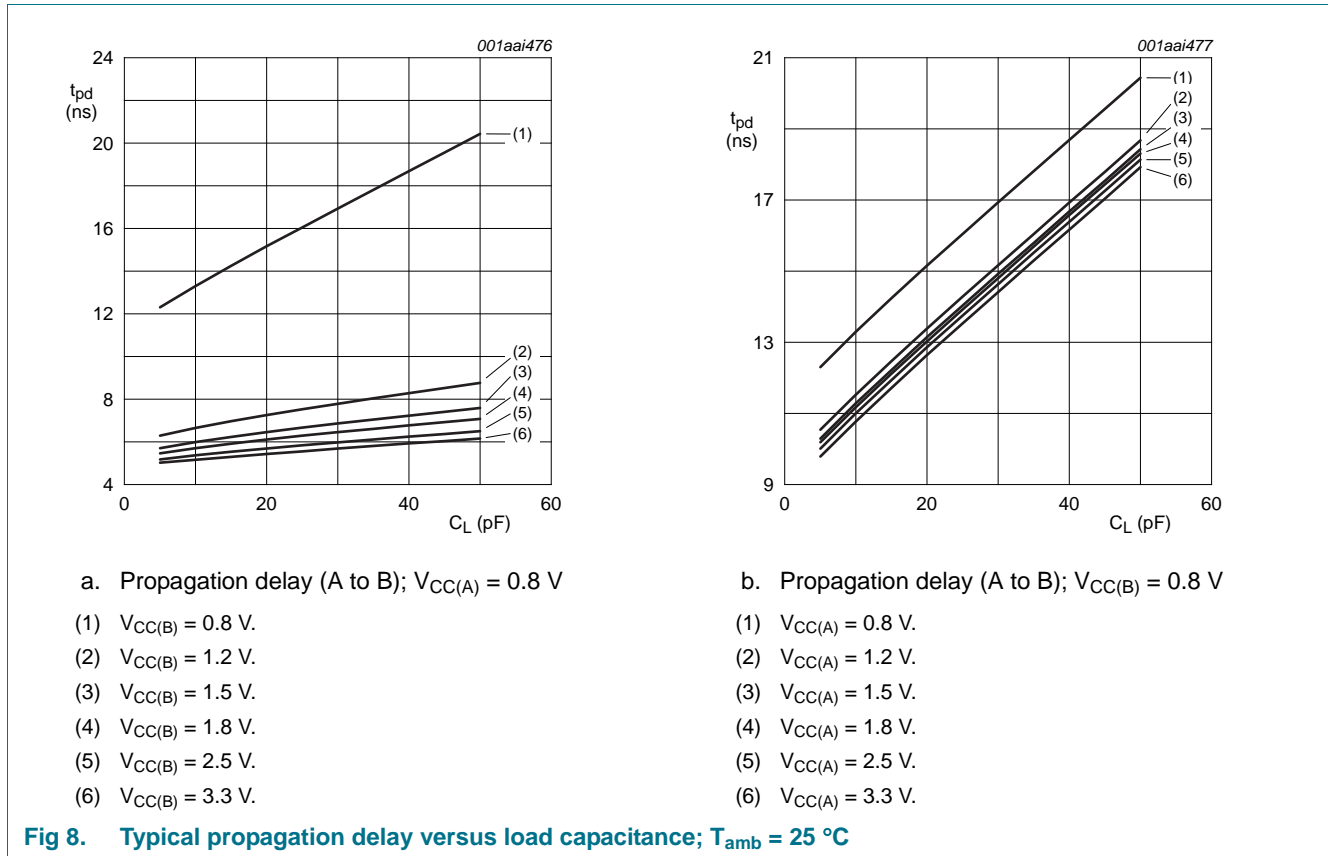
Fig 7. Test circuit for measuring switching times

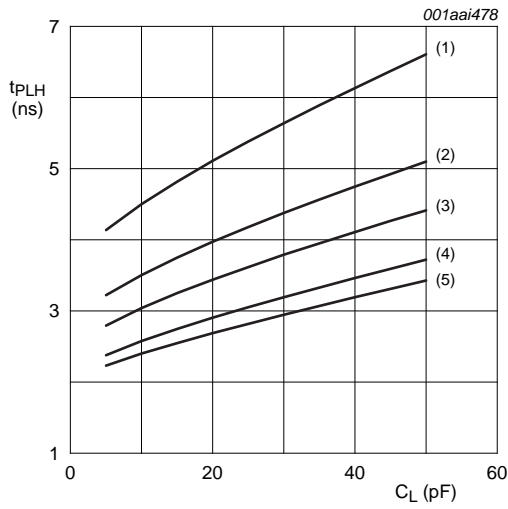
Table 15. Test data

Supply voltage	Input		Load		V_{EXT}		
	$V_{CC(I)}$ ^[1]	$\Delta t/\Delta V$ ^[2]	C_L	R_L	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ} ^[3]
0.8 V to 1.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 k Ω	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 k Ω	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 k Ω	open	GND	$2V_{CCO}$

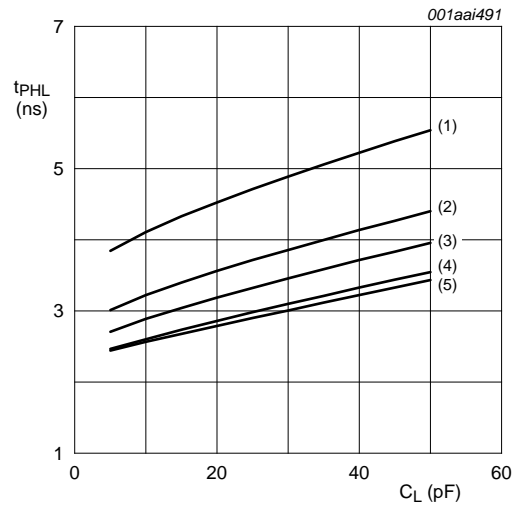
- [1] V_{CCI} is the supply voltage associated with the data input port.
- [2] $dV/dt \geq 1.0$ V/ns
- [3] V_{CCO} is the supply voltage associated with the output port.

12. Typical propagation delay characteristics

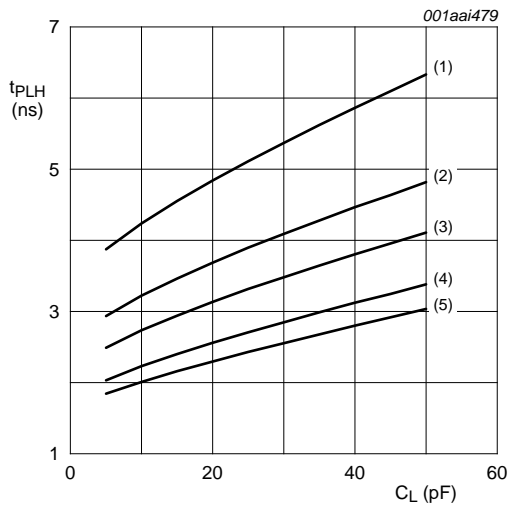




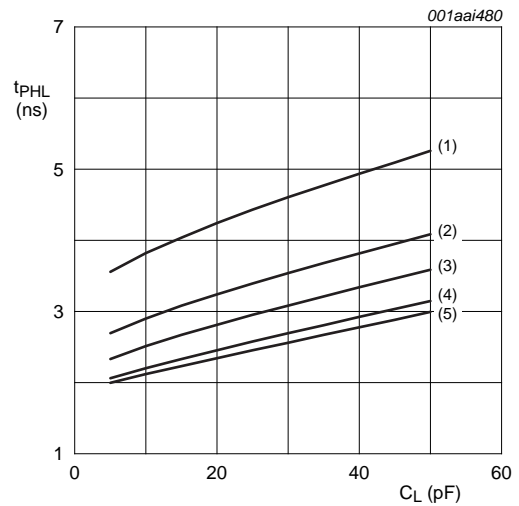
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.2\text{ V}$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.2\text{ V}$



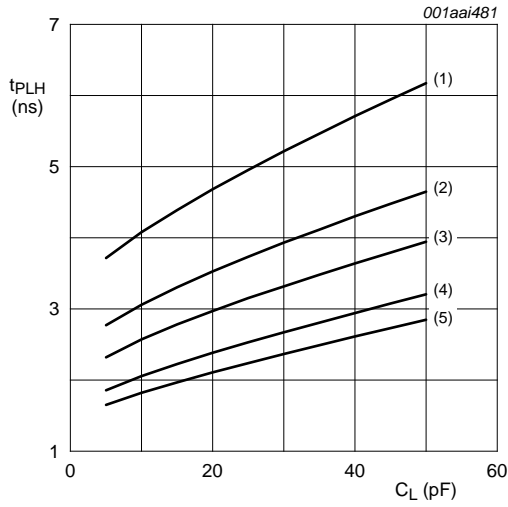
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.5\text{ V}$



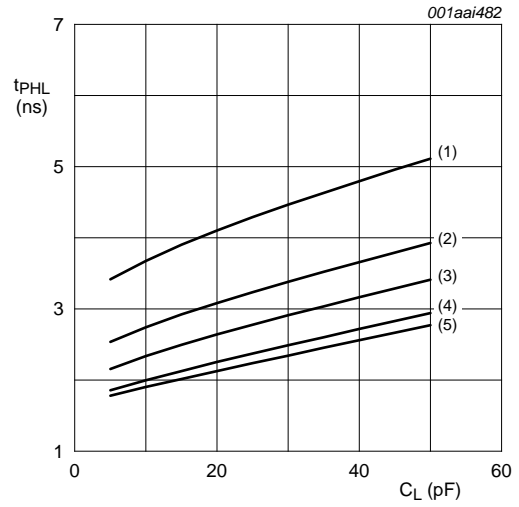
d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.5\text{ V}$

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.

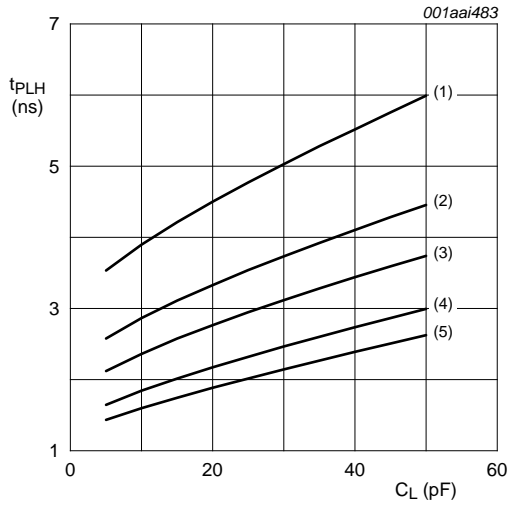
Fig 9. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$



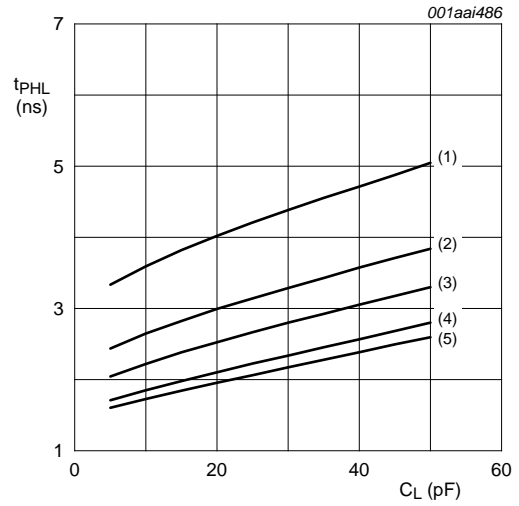
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.8\text{ V}$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.8\text{ V}$



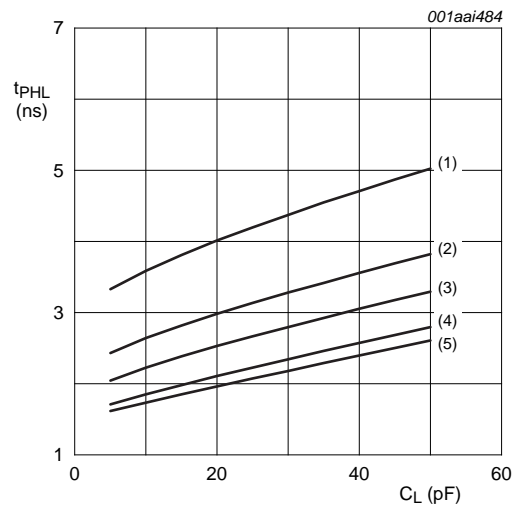
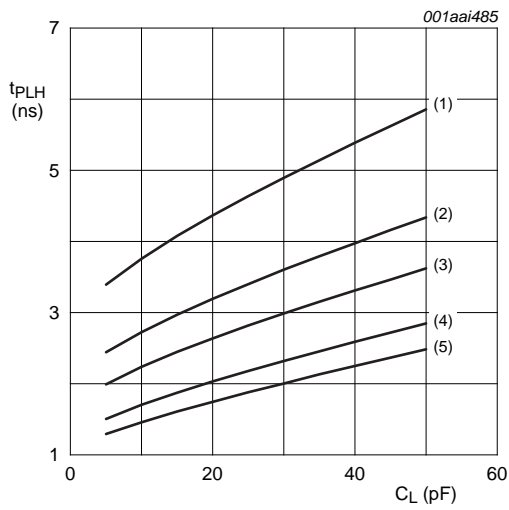
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 2.5\text{ V}$



d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 2.5\text{ V}$

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.

Fig 10. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$



a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 3.3\text{ V}$

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.

b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 3.3\text{ V}$

Fig 11. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ °C}$

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

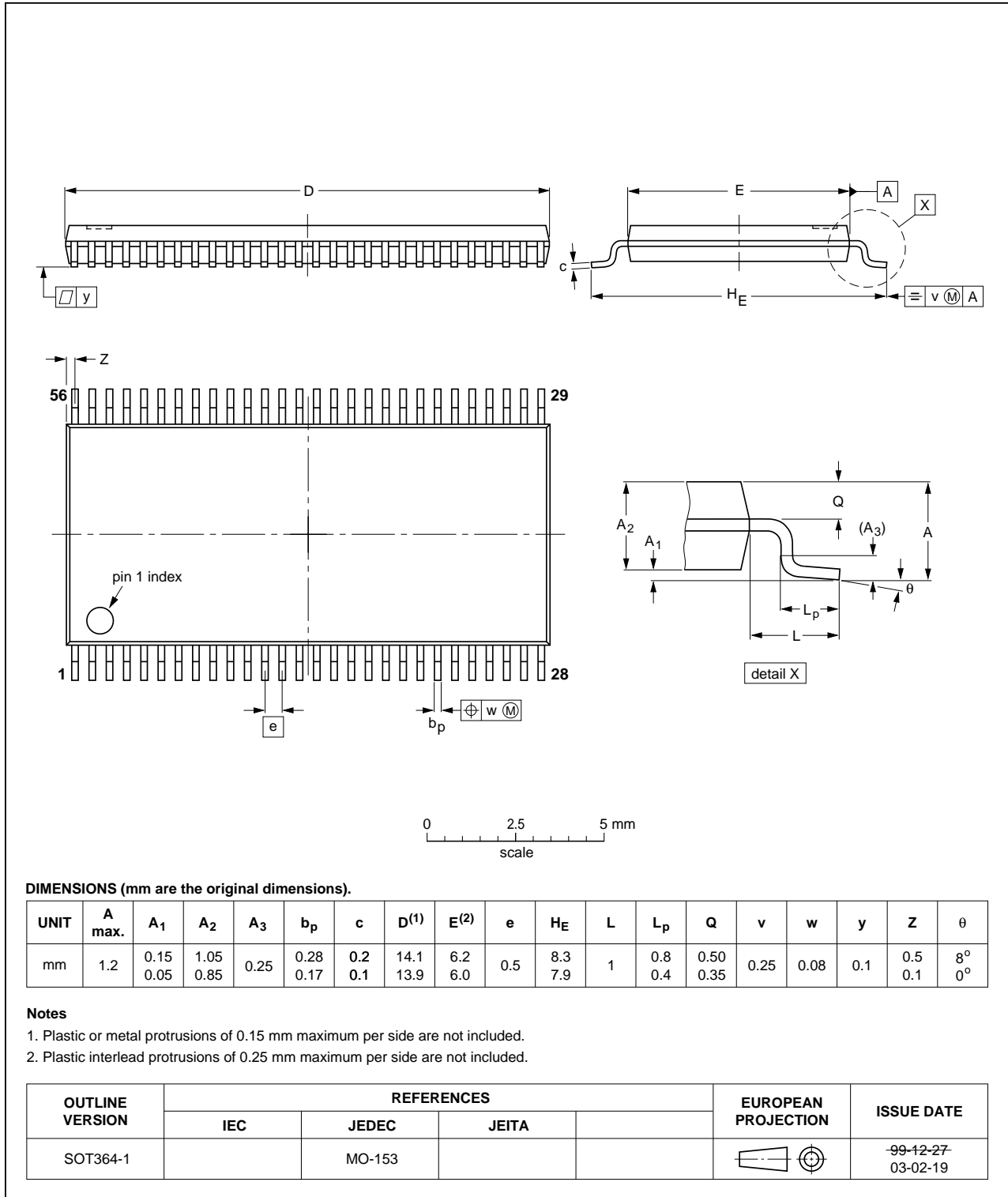


Fig 12. Package outline SOT364-1 (TSSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 4.4 mm

SOT481-2

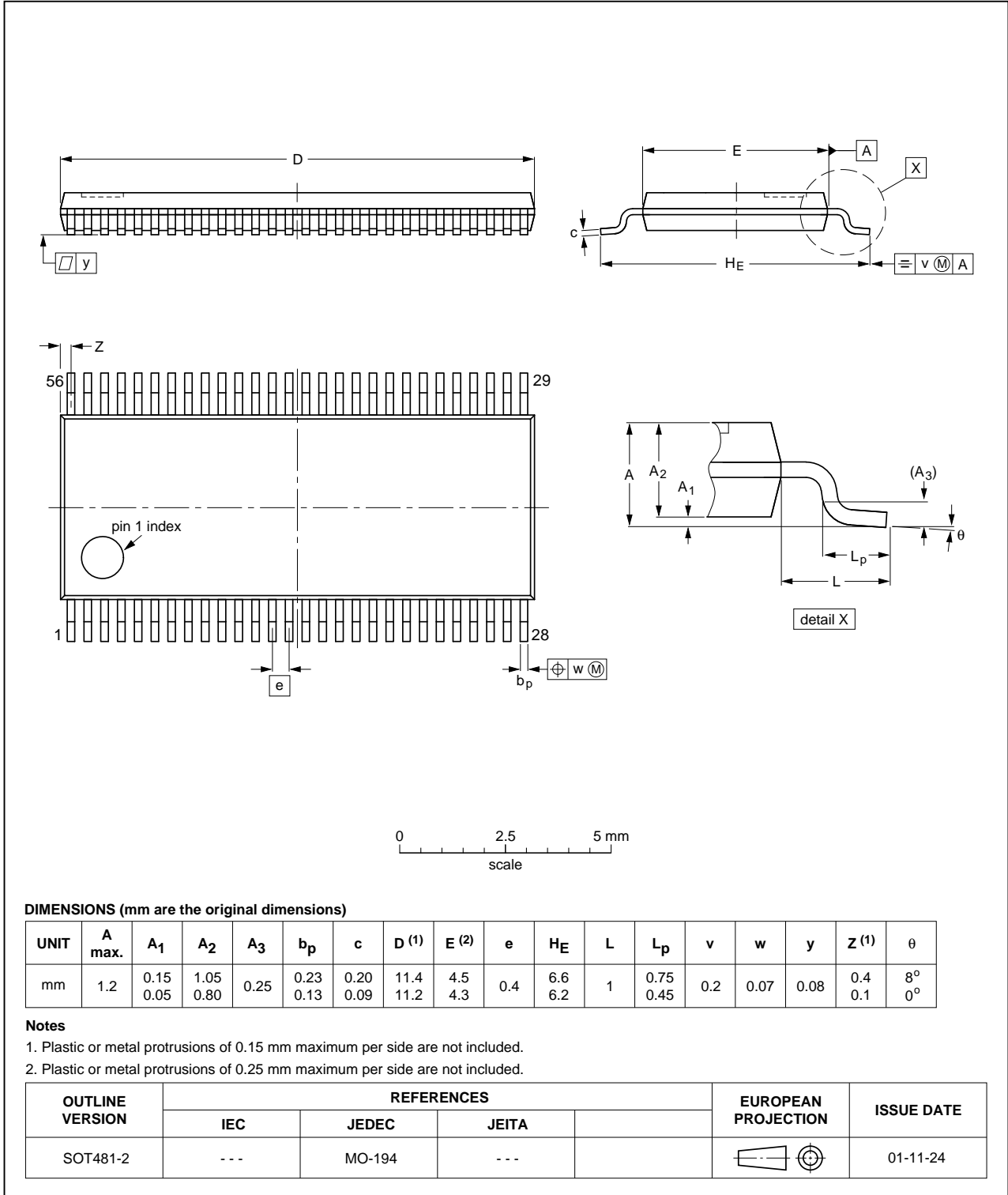


Fig 13. Package outline SOT481-2 (TSSOP56)

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.5 mm

SOT1134-1

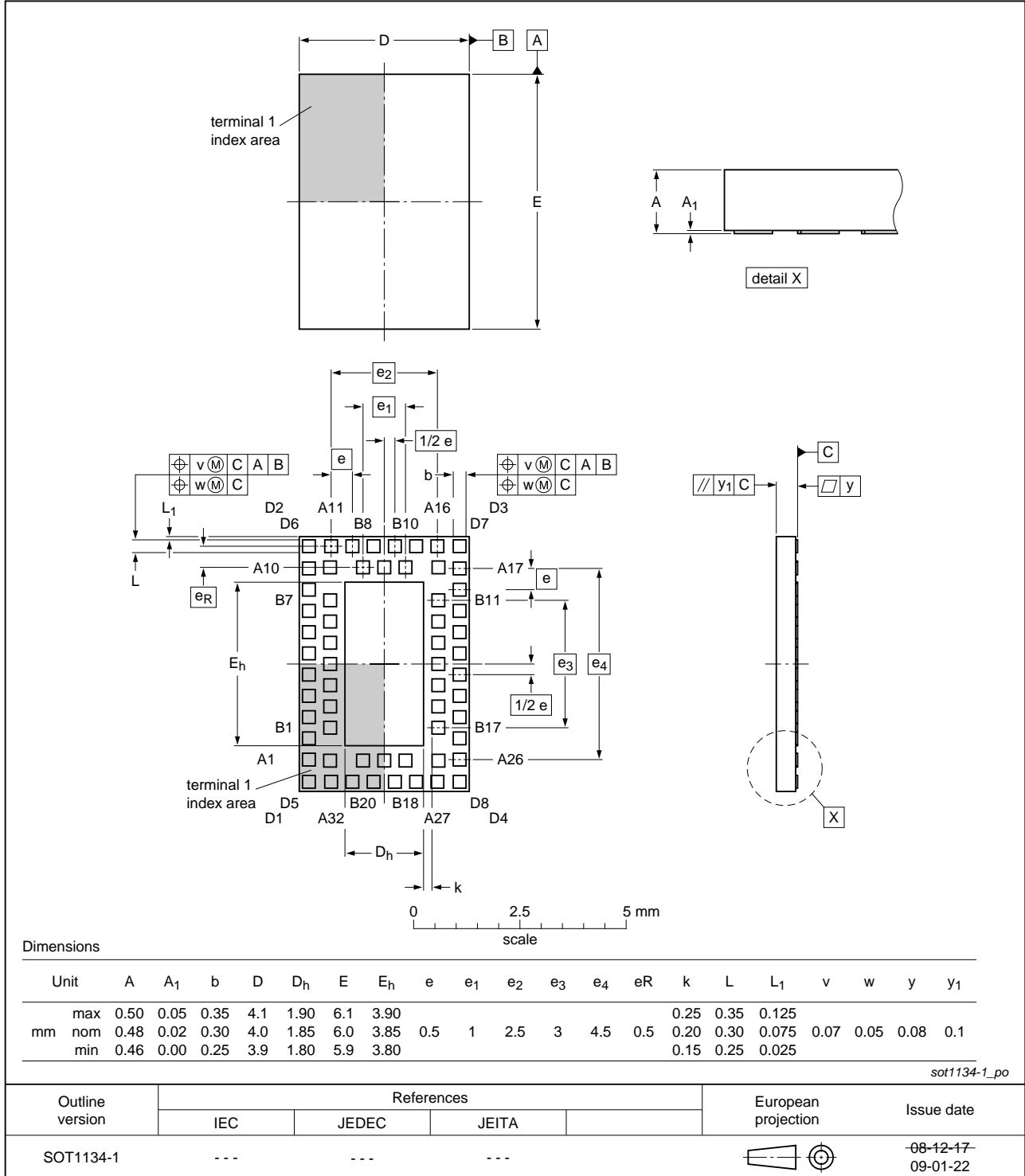


Fig 14. Package outline SOT1134-1 (HXQFN60U)

14. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH20T245 v.5	20160223	Product data sheet	-	74AVCH20T245 v.4
Modifications:	<ul style="list-style-type: none"> General description updated. 			
74AVCH20T245 v.4	20111214	Product data sheet	-	74AVCH20T245 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74AVCH20T245 v.3	20110623	Product data sheet	-	74AVCH20T245 v.2
74AVCH20T245 v.2	20100315	Product data sheet	-	74AVCH20T245 v.1
74AVCH20T245 v.1	20100113	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	6
6	Functional description	6
7	Limiting values	7
8	Recommended operating conditions	7
9	Static characteristics	8
10	Dynamic characteristics	12
11	Waveforms	16
12	Typical propagation delay characteristics ..	18
13	Package outline	22
14	Abbreviations	25
15	Revision history	25
16	Legal information	26
16.1	Data sheet status	26
16.2	Definitions	26
16.3	Disclaimers	26
16.4	Trademarks	27
17	Contact information	27
18	Contents	28

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>



For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 February 2016

Document identifier: 74AVCH20T245

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 74AVCH20T245DGV:11 on WIN SOURCE](#)
-  [NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management