

FEATURES

- Member of the Texas Instruments Widebus™ Family
- DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCAH164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCAH164245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA} .

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, then both ports are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCAH164245GR	AVCAH164245
	TVSOP – DGV	Tape and reel	SN74AVCAH164245VR	WAH4245
	VFBGA – GQL	Tape and reel	SN74AVCAH164245KR	WAH4245

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

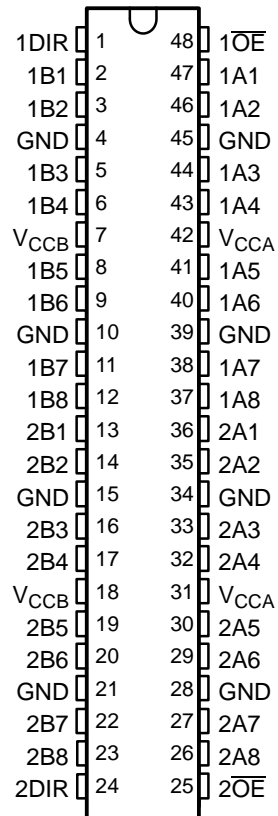
Widebus, DOC are trademarks of Texas Instruments.

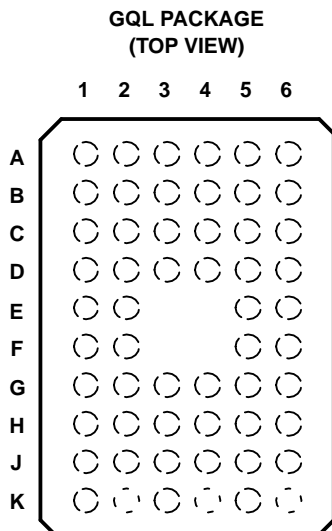
SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A–JULY 2002–REVISED JUNE 2005

TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)





TERMINAL ASSIGNMENTS⁽¹⁾

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1 \overline{OE}
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V _{CCB}	V _{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V _{CCB}	V _{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2 \overline{OE}

(1) NC – No internal connection

**FUNCTION TABLE
(EACH 8-BIT SECTION)**

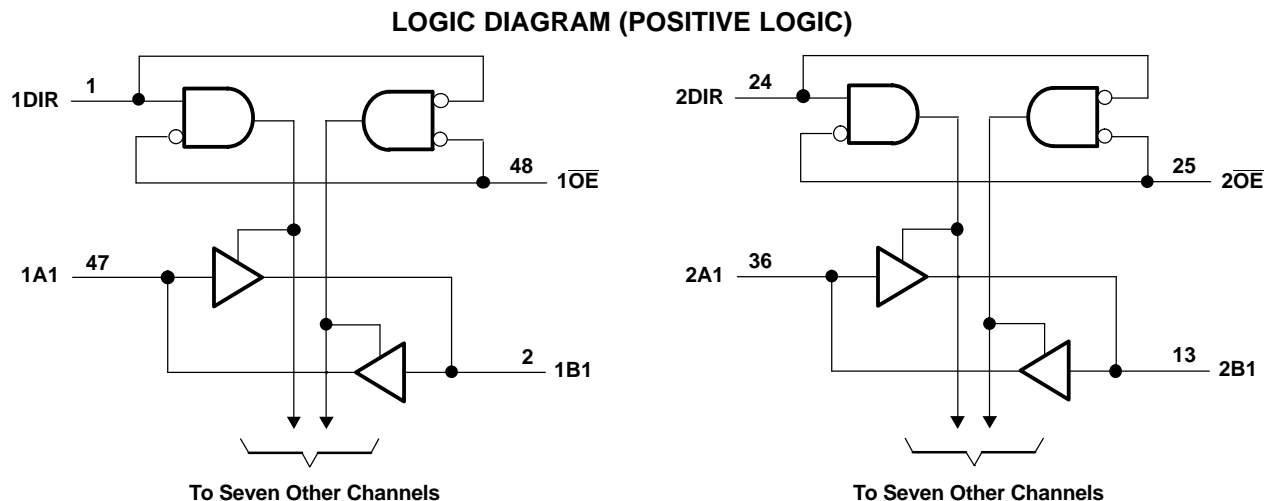
INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN74AVCAH164245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A—JULY 2002—REVISED JUNE 2005



Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{CCA} V_{CCB}	Supply voltage range	-0.5	4.6	V	
V_I	Input voltage range ⁽²⁾	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current		-50	mA	
I_{OK}	Output clamp current		-50	mA	
I_O	Continuous output current		± 50	mA	
	Continuous current through V_{CCA} , V_{CCB} , or GND		± 100	mA	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W	
		DGV package	58		
		GQL package	28		
T_{stg}	Storage temperature range	-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.4	3.6	V
V _{CCB}	Supply voltage				1.4	3.6	V
V _{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V		V _{CCI} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _{IH}	High-level input voltage	Control inputs (referenced to V _{CCA})	1.4 V to 1.95 V		V _{CCA} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Control inputs (referenced to V _{CCA})	1.4 V to 1.95 V		V _{CCA} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.4 V to 1.6 V		–2	mA
				1.65 V to 1.95 V		–4	
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–12	
I _{OL}	Low-level output current			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T _A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



SCES396A–JULY 2002–REVISED JUNE 2005

Electrical Characteristics⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	MIN	TYP ⁽³⁾	MAX	UNIT
V _{OH}			I _{OH} = -100 μA, V _I = V _{IH}	1.4 V to 3.6 V	1.4 V to 3.6 V	V _{CCO} - 0.2 V			V
			I _{OH} = -2 mA, V _I = V _{IH}	1.4 V	1.4 V	1.05			
			I _{OH} = -4 mA, V _I = V _{IH}	1.65 V	1.65 V	1.2			
			I _{OH} = -8 mA, V _I = V _{IH}	2.3 V	2.3 V	1.75			
			I _{OH} = -12 mA, V _I = V _{IH}	3 V	3 V	2.3			
V _{OL}			I _{OH} = 100 μA, V _I = V _{IL}	1.4 V to 3.6 V	1.4 V to 3.6 V				V
			I _{OH} = 2 mA, V _I = V _{IL}	1.4 V	1.4 V				
			I _{OH} = 4 mA, V _I = V _{IL}	1.65 V	1.65 V				
			I _{OH} = 8 mA, V _I = V _{IL}	2.3 V	2.3 V				
			I _{OH} = 12 mA, V _I = V _{IL}	3 V	3 V				
I _I	Control inputs	V _I = V _{CCA} or GND		1.4 V to 3.6 V	3.6 V				±2.5 μA
I _{BHL} ⁽⁴⁾			V _I = 0.49 V	1.4 V	1.4 V	11			μA
			V _I = 0.57 V	1.65 V	1.65 V	30			
			V _I = 0.7 V	2.3 V	2.3 V	45			
			V _I = 0.8 V	3 V	3 V	75			
I _{BHH} ⁽⁵⁾			V _I = 0.91 V	1.4 V	1.4 V	-11			μA
			V _I = 1.07 V	1.65 V	1.65 V	-30			
			V _I = 1.7 V	2.3 V	2.3 V	-45			
			V _I = 2 V	3 V	3 V	-75			
I _{BHLO} ⁽⁶⁾			V _I = 0 to V _{CC}	1.6 V	1.6 V	100			μA
				1.95 V	1.95 V	200			
				2.7 V	2.7 V	300			
				3.6 V	3.6 V	525			
I _{BHHO} ⁽⁷⁾			V _I = 0 to V _{CC}	1.6 V	1.6 V	-100			μA
				1.95 V	1.95 V	-200			
				2.7 V	2.7 V	-300			
				3.6 V	3.6 V	-525			
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V				μA
	B port			0 to 3.6 V	0 V				
I _{OZ} ⁽⁸⁾	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V				μA
	B port		$\overline{OE} = \text{don't care}$	0 V	3.6 V				
	A port			3.6 V	0 V				

- (1) V_{CCO} is the V_{CC} associated with the output port.
- (2) V_{CCI} is the V_{CC} associated with the input port.
- (3) All typical values are at T_A = 25°C.
- (4) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
- (5) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
- (6) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (7) An external driver must sink at least I_{BHHO} to switch this node from high to low.
- (8) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Electrical Characteristics⁽¹⁾(continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.6 V	1.6 V			20	μA
			1.95 V	1.95 V			20	
			2.7 V	2.7 V			30	
			0 V	3.6 V			–40	
			3.6 V	0 V			40	
			3.6 V	3.6 V			40	
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.6 V	1.6 V			20	μA
			1.95 V	1.95 V			20	
			2.7 V	2.7 V			30	
			0 V	3.6 V			40	
			3.6 V	0 V			–40	
			3.6 V	3.6 V			40	
C _i	Control inputs	V _I = 3.3 V or GND	3.3 V	3.3 V		4	pF	
C _{io}	A or B ports	V _O = 3.3 V or GND	3.3 V	3.3 V		5	pF	

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t _{en}	OE	A	2.6	8.4	2.7	8.2	2.3	6.3	2.1	5.6	ns
		B	2.7	8.6	3.2	10.2	3.2	10.8	3.2	10.7	
t _{dis}	OE	A	2.1	7	2.5	7	1.7	5.3	2	6.1	ns
		B	2.1	7.1	2.5	7.1	2.1	6.5	2.1	6.4	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t _{en}	OE	A	2.5	8	2.7	7.8	2.2	5.8	2	5.1	ns
		B	1.8	6.7	2.7	7.8	2.7	8.1	2.7	8.1	
t _{dis}	OE	A	2.1	6.4	2.5	6.4	1.5	4.5	1.8	5	ns
		B	2.1	6.6	2.5	6.4	2	5.5	2	5.5	

SN74AVCAH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A–JULY 2002–REVISED JUNE 2005

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	\overline{OE}	A	2.6	7.4	2.7	7.2	2.2	5.3	2	4.5	ns
		B	1.2	4.1	2.2	5.1	2.2	5.3	2.2	5.3	
t_{dis}	\overline{OE}	A	2	5.7	2.3	5.7	1.4	3.7	1.6	4	ns
		B	0.9	4.5	1.7	4.5	1.4	3.7	1.4	3.7	

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	\overline{OE}	A	2.5	7	2.6	6.9	2.1	5	1.9	4.1	ns
		B	0.8	2.6	1.9	4	2	4.1	1.9	4.1	
t_{dis}	\overline{OE}	A	1.2	5.4	2.2	5.2	1.2	3.3	1.5	3.6	ns
		B	1.2	5.4	1.7	4.4	1.5	3.6	1.5	3.6	

Operating Characteristics

V_{CCA} and $V_{CCB} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA}	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$, $f = 10\text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB}	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$, $f = 10\text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	

Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

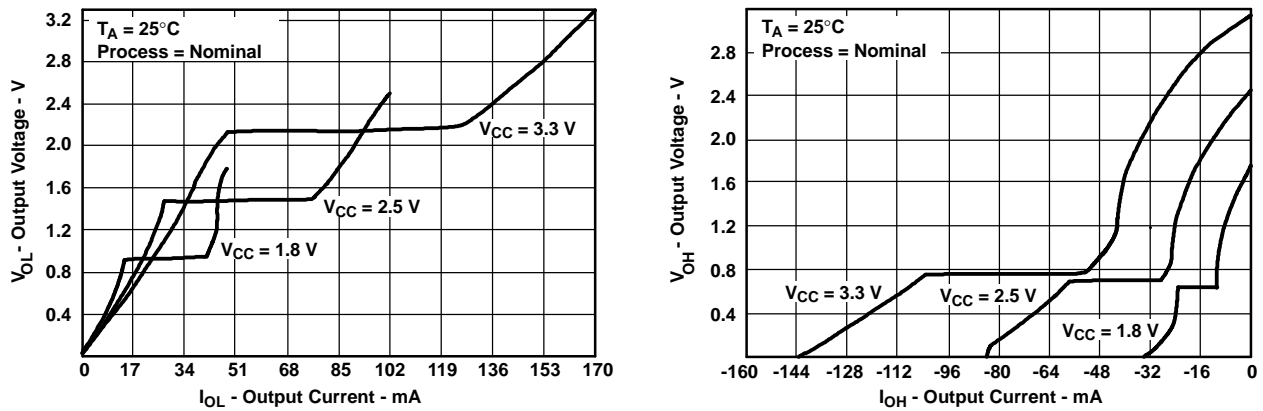
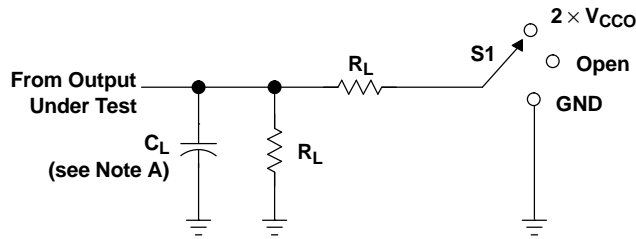


Figure 1. Output Voltage vs Output Current

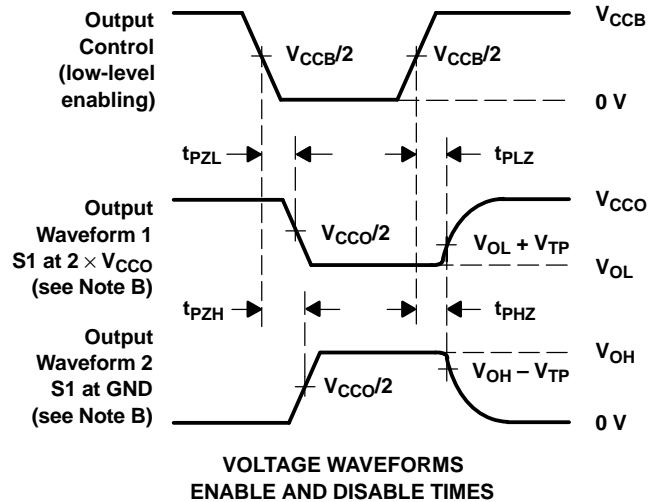
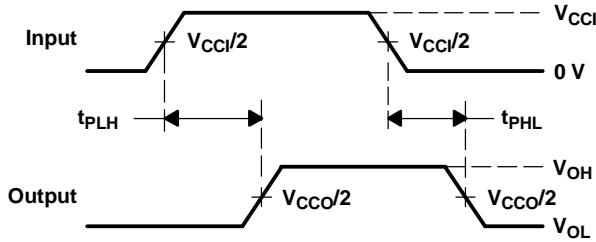
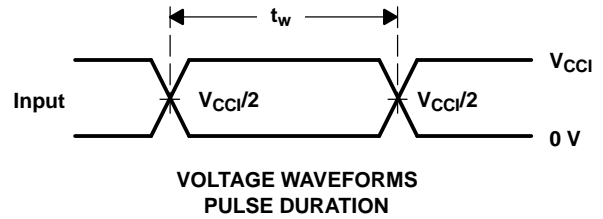
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
$1.5\text{ V} \pm 0.1\text{ V}$	15 pF	2 k Ω	0.1 V
$1.8\text{ V} \pm 0.15\text{ V}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	30 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $dv/dt \geq 1\text{ V/ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. V_{CCi} is the V_{CC} associated with the input port.
I. V_{CCo} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCAH164245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCAH164245	Samples
74AVCAH164245VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WAH4245	Samples
74AVCAH164245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WAH4245	Samples
SN74AVCAH164245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCAH164245	Samples
SN74AVCAH164245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WAH4245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCAH164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74AVCAH164245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVCAH164245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCAH164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	350.0	350.0	43.0
SN74AVCAH164245GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVCAH164245VR	TVSOP	DGV	48	2000	367.0	367.0	38.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



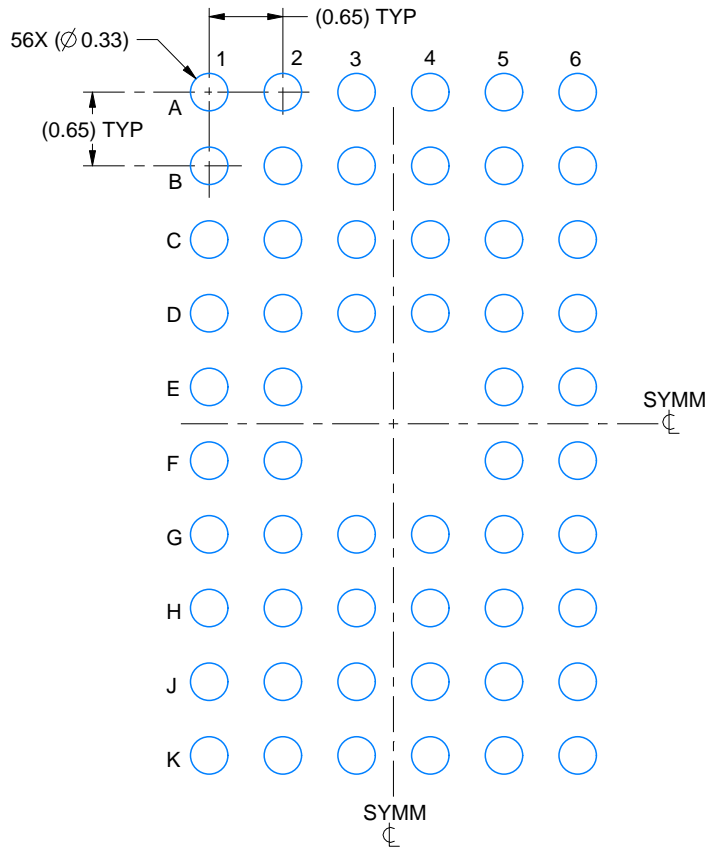
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

EXAMPLE BOARD LAYOUT

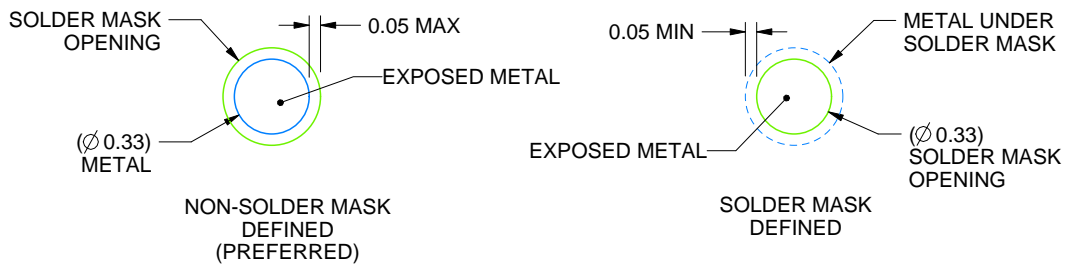
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4219711/B 01/2017

NOTES: (continued)

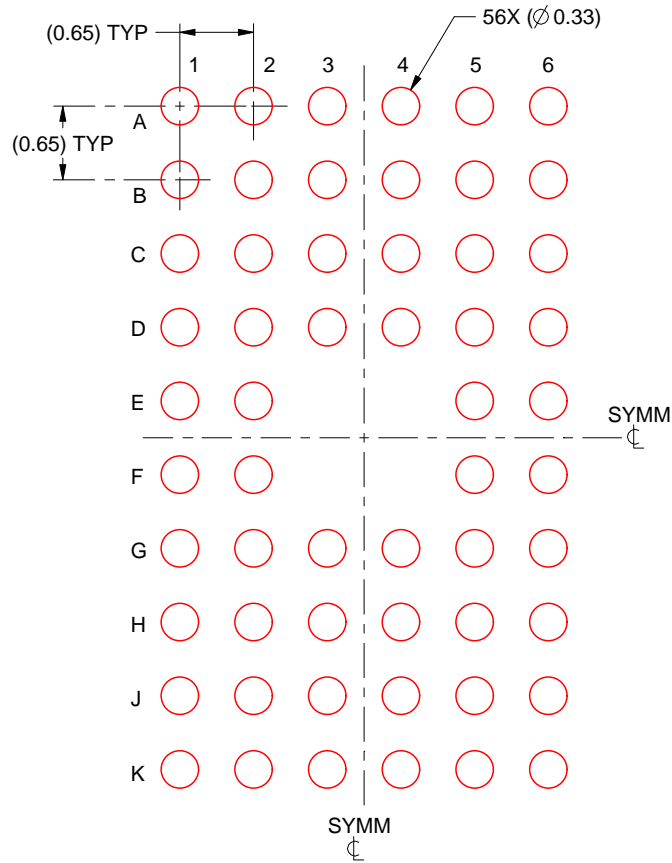
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View 74AVCAH164245ZQLR on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management