THE DATASHEET OF

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SiI9022A/SiI9024A HDMI Transmitter

Data Sheet

SiI-DS-1076-E.01

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1. General Description

The Lattice Semiconductor SiI9022A/SiI9024A HDMI® transmitter supports the High Definition Multimedia Interface (HDMI) Specification on a wide range of mobile products. High definition camcorders, digital still cameras, and personal mobile devices connect directly to a large installed base of HDMI TVs and DVI PC monitors by using the flexible audio and video interfaces provided by this ultra-low-power solution. S/PDIF or I²S inputs enable a pure digital audio connection to virtually any system audio processor or codec. This transmitter is the next generation of its family and is an enhanced replacement for the SiI9022/SiI9024 device, with lower power and enhanced features.

The SiI9024A transmitter is pre-programmed with HDCP keys and has completely self-sequencing HDCP detection and authentication, including SHA-1 for repeaters. The device supports High-bandwidth Digital Content Protection (HDCP) for devices that require secure content delivery.

1.1. Video Input

- xvYCC metadata support
- BTA-T1004 video input format
- Integrated color space converter allows direct connection to all major MPEG decoders, including those that provide only an ITU-R.656 output
- Internal DE generator supports non-embedded sync formats

1.2. HDMI Output

- HDMI, HDCP, and DVI compatible
- TMDS™ core runs at 165 MHz
- Video resolutions up to 1080p and UXGA (72-pin QFN package supports 165 MHz dual-edge mode)
- 3D-capable at 720p/60, 1080i/60, and 1080p/24 frame-pack, side-by-side, L + D, and Top-and-Bottom modes
- HDMI Type A, Type-C, and micro-D connector support

1.3. Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O with hardware protocol and arbitration logic, and requires no external calibration
- Monitor detection is supported through both Hot Plug and Receiver Sense circuits
- Single slave I²C from host, passing through to master I²C interface for DDC connection, simplifies board layout and lowers cost
- Defaults to SiI9020 transmitter register-compatible mode for operation with existing legacy software

1.4. Digital Audio Interface

- Four I²S inputs for Dolby Digital, DTS, or MPEG2 audio with programmable channel mapping (49-ball package supports one I²S input)
- DVD-Audio input (2 or up to 8 channels)
- MCLK is not required for I²S and S/PDIF
- S/PDIF input supports 2-channel PCM or compressed Dolby Digital and DTS digital
- 2:1 and 4:1 down-sampling to handle 96 kHz and 192 kHz audio streams

1.5. Power Management

- Flexible power management with hot-plug wakeup
- Ultra-low power requirement: less than 90 mW active, 150 µW standby

1.6. Packaging

- 81-ball VFBGA (4.0 × 4.0 mm) package
- 72-pin QFN (10 × 10 mm) package
- 49-ball VFBGA (4.0 × 4.0 mm) package
- Standard part covers extended (–20 °C to +85 °C) temperature range

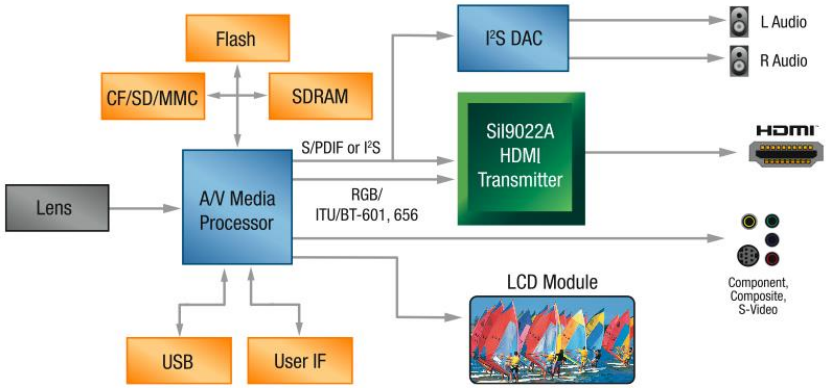

Figure 1.1. Typical Application (SiI9022A HDMI Transmitter Shown)

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1.7. Comparison of the SiI9022A/SiI9024A Device with Other HDMI Transmitters

Table 1.1 summarizes the differences among the previous Lattice Semiconductor HDMI transmitters and the SiI9022A/SiI9024A HDMI transmitters.

Table 1.1. Summary of Features

HDMI Transmitter	SiI9030	SiI9020	SiI9022	SiI9022-6	SiI9024	SiI9024-6	SiI9022A	SiI9024A	SiI9022A	SiI9024A
							VFBGA		QFN	
Video Input										
Clock duty cycle	60/40	60/40	70/30	70/30	70/30	70/30	70/30	70/30	70/30	70/30
Max frequency	150 MHz	84 MHz	82.5 MHz	165 MHz	82.5 MHz	165 MHz	165 MHz	165 MHz	165 MHz[3]	165 MHz[3]
Input signal level[2]	3.3 V	3.3 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V
Audio Input										
Max S/PDIF frequency	96 kHz	96 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz
I^2S MCLK required?	Yes	Yes	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional
S/PDIF MCLK required?	Yes	Yes	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional
DDC I^2C Bus										
Voltage Tolerance[1]	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V
HDCP										
Encryption engine	Yes	No	No	No	Yes	Yes	No	Yes	No	Yes
Auto authentication	No	No	No	No	Yes	Yes	No	Yes	No	Yes
Other										
Core power supply	1.8 V	1.8 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V
I/O power supply[2]	3.3 V	3.3 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8 V	3.3 V or 1.8V	3.3 V or 1.8 V	3.3 V or 1.8V[4]	3.3 V or 1.8 V[4]
Package	80-pin TQFP	84-ball TFBGA	84-ball TFBGA or 81-ball VFBGA	84-ball TFBGA	84-ball TFBGA or 81-ball VFBGA	84-ball TFBGA	81-ball VFBGA or 49-ball VFBGA	81-ball VFBGA or 49-ball VFBGA	72-pin QFN	72-pin QFN

Notes:

1. The DDC pads of the SiI9022A/SiI9024A device are 5 V compliant with or without IOVCC power supply. For other devices listed above, the DDC pads are 5 V tolerant only when chip IOVCC is applied
2. The SiI9022A/SiI9024A 81-ball and 72-pin package supports both 1.8 V and 3.3 V threshold-compliant operation. The 49-ball package only supports 1.8 V compliant I/O. Both devices have 3.3 V tolerant I/O when IOVCC is 1.8 V.
3. Supports up to 165 MHz dual-edge and single-edge modes.
4. For dual-edge mode above 82.5 MHz, only 3.3 V ± 10% can be used for IOVCC.

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2. Functional Description

The SiI9022A/SiI9024A HDMI transmitter provides a complete solution for transmitting HDMI-compliant digital audio and video. Specialized audio and video processing is available within the transmitter to easily and cost-effectively add HDMI capability to the consumer electronics devices. Figure 2.1 shows the functional block diagram of the chip. In the 49-ball package, DE and S/PDIF share the same pin.

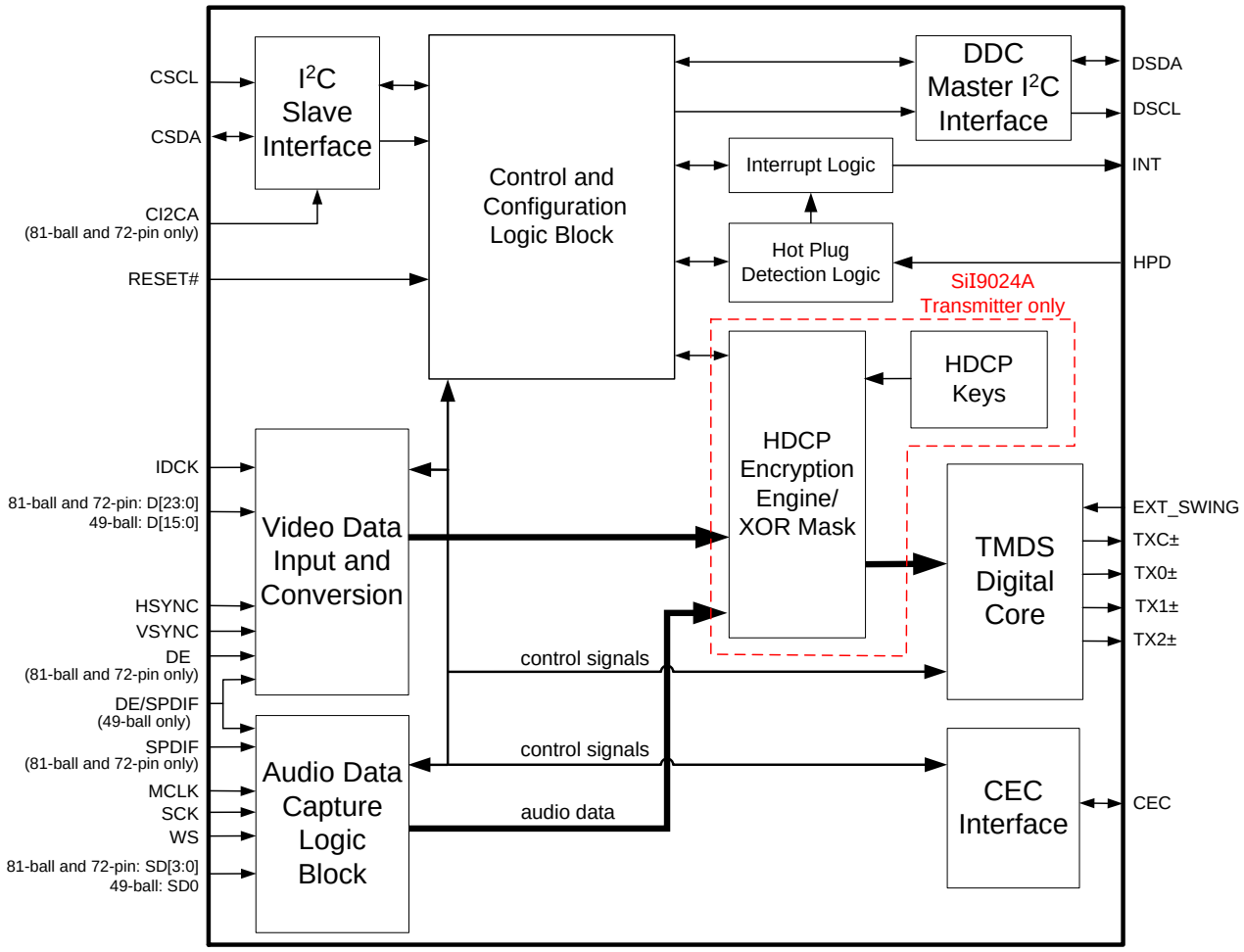

Figure 2.1. Functional Block Diagram

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2.1. Video Data Input and Conversion

Figure 2.2 shows the video data processing stages through the transmitter. Each of the processing blocks can be bypassed by setting the appropriate register bits. The HSYNC and VSYNC input signals are required, except in embedded sync modes. The DE input signal is optional, because it can be created with the DE generator using the HSYNC and VSYNC signals.

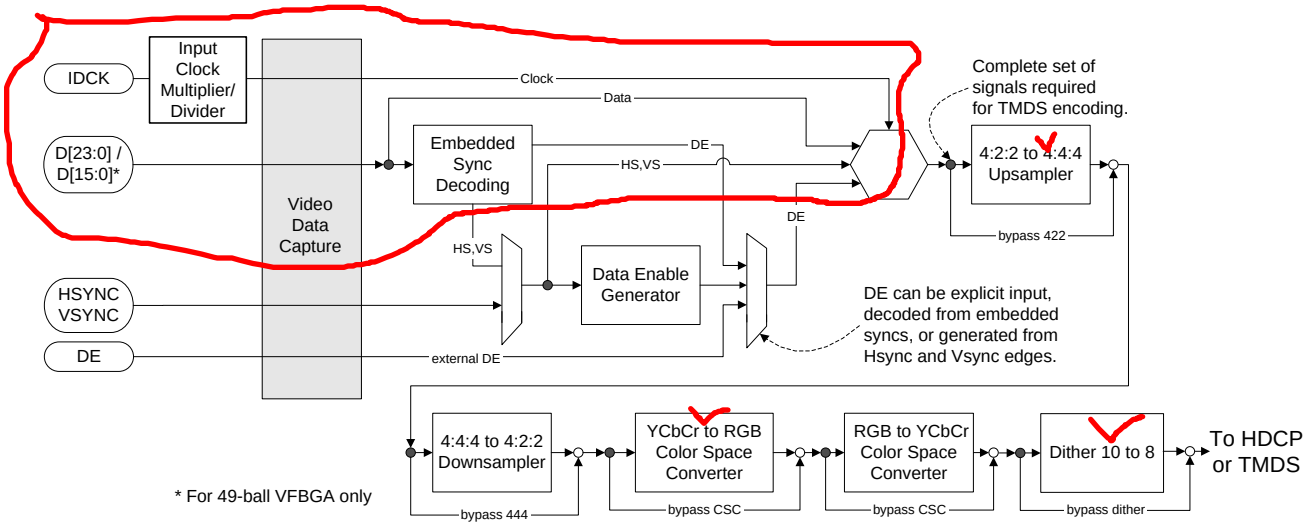

Figure 2.2. Transmitter Video Data Processing Path

2.1.1. Input Clock Multiplier/Divider

The input pixel clock can be multiplied by 2 or 4, or divided by 2 (multiplied by 0.5). Video input formats which use a 2x clock (such as YC Mux mode) can then be transmitted across the HDMI link with a 1x clock. Similarly, 1x-to-2x, 1x-to-4x, and 2x-to-4x conversions are possible.

2.1.2. Video Data Capture

The video data capture block receives uncompressed digital video through an interface ranging from 8 to 16 bits in width for the 49-ball package and from 8 to 24 bits in width for the 81-ball and 72-pin package. These interfaces have two or three 8-bit data channels, which can be configured for the video formats shown in the RGB to YCbCr Color Space Converter section on page 34. It provides a direct connection to major MPEG decoders. Registers set the bus width (8/10/12/16/20/24-bit), format, and rising/falling edge latching according to the video format sent to the transmitter. This information is passed over the HDMI link in the CEA-861D Auxiliary Video Information (AVI) InfoFrame packets.

2.1.3. Embedded Sync Decoding

The transmitter can create DE, HSYNC, and VSYNC signals using the start of active video (SAV) and end of active video (EAV) codes within the ITU-R BT.656-format video stream.

2.1.4. Data Enable Generator

The transmitter includes logic to construct a Data Enable (DE) signal from the incoming HSYNC, VSYNC, and IDCK. This signal is used to correct timing from sync extraction to conform to CEA-861D timing specifications. By programming registers, the DE signal can define the size of the active display region. This feature is particularly useful when the transmitter connects to MPEG decoders that do not provide a specific DE output signal.

2.1.5. Color Space Converter

Two color space converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by AV processors and to provide full DVI 1.0 backward compatibility. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate

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registers. See the RGB to YCbCr Color Space Converter and YCbCr to RGB Color Space Converter sections starting on page 34 for more information.

2.1.6. 4:2:2 to 4:4:4 Upsampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

2.1.7. 4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

2.1.8. Dither 10 to 8

The dither block takes the internally processed data and reduces it down to 8 bits for output.

2.2. Audio Data Capture Logic

The SiI9022A/SiI9024A device in the 81-ball and 72-pin packages have individual S/PDIF and I^{2}S (SD[3:0]) inputs for accepting digital audio input. The Feature Information section on page 34 provides more information about audio formats and available sampling frequencies.

Due to the reduced lead count, the SiI9022A/SiI9024A transmitter in the 49-ball package has certain restrictions on the audio because ball G6 is shared by both the S/PDIF and DE inputs. When the device is configured to use S/PDIF, the video format must use either the DE generator mode or one of the YC 4:2:2 embedded sync formats.

2.3. I^{2}C Slave Interface

The controller I^{2}C interface on the transmitter (signals CSCL and CSDA) is a slave interface with an operating frequency from 40 kHz to 400 kHz and with an input tolerance of up to 4.0 V when all chip operating voltages are present. The host uses this interface to configure the transmitter by reading from and writing to appropriate registers.

2.4. Control and Configuration

The register/configuration logic block incorporates all the registers required for configuring and managing the transmitter. A separate logic block handles the configuration and operation of the CEC subsystem.

2.5. DDC Master I^{2}C Interface

The transmitter has a master I^{2}C port for direct connection to the HDMI cable. DDC read and write operations are executed by reading and writing registers in the transmitter. This feature simplifies the system design and helps to lower its cost. See the DDC Support section on page 37 for more information.

2.6. Interrupt Logic

The INT signal interrupts the host processor when certain conditions arise inside the transmitter. The INT output is programmable to be either active HIGH or active LOW; see the Configuration and Control Signals section. Conditions which create an interrupt include:

- Monitor detect (either from the HPD input level, or from the Receiver Sense feature)
- VSYNC (useful for synchronizing a host processor to the vertical timing interval)
- HDCP event
- CEC event
- Audio interrupt.

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2.7. Hot Plug Detection Logic

The Hot Plug Detection Logic block determines if a receiver is connected to the SiI9022A/SiI9024A transmitter. When HIGH, the HPD signal indicates to the transmitter that the EDID of the connected receiver is readable. A HIGH voltage is at least 2.0 V, and a LOW voltage is less than 0.8 V.

2.8. HDCP Encryption Engine/XOR Mask (SiI9024A Device Only)

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support for HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selector Value (KSV) stored in the on-board ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

2.9. HDCP Key ROM (SiI9024A Device Only)

The SiI9024A transmitter comes pre-programmed with a set of production HDCP keys stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The pre-programmed HDCP keys provide the highest level of security because there is no way to read the keys once the devices are programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving samples of the transmitter.

2.10. TMDS Digital Core

The TMDS Digital Core performs 8-bit to 10-bit TMDS encoding on the audio, video, and auxiliary data received from the Dither 10 to 8 block. This data is sent through three TMDS differential data lines along with a TMDS differential clock. A resistor connected to the EXT_SWING signal controls the TMDS swing amplitude.

2.11. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC- compliant signals between CEC devices and a CEC master. A CEC controller using the Lattice Semiconductor CEC Programming Interface (CPI) is included on the chip. This controller has a high-level register interface accessible through the I^2C interface and is used to send and receive CEC commands. This controller makes CEC implementation very straightforward and removes the burden of managing bit transitions on the CEC bus from the host CPU.

The SiI9022A/SiI9024A CEC logic is self-calibrating and does not require a calibration procedure as the previous generation devices did.

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3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC	I/O supply voltage	–0.3	—	4.0	V	1, 2, 3
AVCC12	TMDS analog supply voltage	–0.3	—	1.5	V	1, 2
CVCC12	Digital core supply voltage	–0.3	—	1.5	V	1, 2, 3
V_I	Input voltage	–0.3	—	4	V	1, 2
V_O	Output voltage	–0.3	—	4	V	1, 2
V_{I5V}	Input voltage, 5 volt tolerant I/O	–0.3	—	5.5	V	1, 2, 4
V_{O5V}	Output voltage, 5 volt tolerant I/O	–0.3	—	5.5	V	1, 2, 4
T_J	Junction temperature	—	—	125	°C	—
T_{STG}	Storage temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. HPD (input), DSCL (output), DSDA (input/output).

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC	I/O supply voltage: 1.8 V host	1.62	1.8	1.98	V	2
	I/O supply voltage: 3.3 V host	3.0	3.3	3.6	V	2
AVCC12	TMDS analog supply voltage	1.08	1.2	1.32	V	1
CVCC12	Digital core supply voltage	1.08	1.2	1.32	V	1
V_{CCN}	Allowable noise on AVCC	—	—	50	mV_{P-P}	—
T_A	Ambient temperature (with power applied)	–20	25	85	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	75.3	°C/W	3, 6
		—	—	86.5	°C/W	4, 6
		—	—	28.5	°C/W	5, 6
Θ_{jc}	Ambient thermal resistance (Theta JC)	—	—	22.6	°C/W	3, 6
		—	—	22.7	°C/W	4, 6
		—	—	13.1	°C/W	5, 6

Notes:
1. CVCC12 and AVCC12 can be derived from the same power source.
2. The 81-ball and 72-pin package supports 3.3 V or 1.8 V; the 49-ball package supports 1.8 V only.
3. 81-ball package
4. 49-ball package
5. 72-pin package
6. Values for Θ_{ja} and Θ_{jc} are provided for a 4-layer PCB, Airflow at 0 m/s.

See page 69 for schematics showing decoupling and power supply regulation.

3.2.1. IOVCC Supply Voltage Requirements

The 72-pin or 81-ball package SiI9022A/SiI9024A transmitter IOVCC supply can operate at either 3.3 V or 1.8 V, depending on the input level to the IO_SEL pin provided by the host. When IOVCC = 1.8 V, the I/O is 3.3 V tolerant. However, to ensure the input/output thresholds are within specifications, the IOVCC on the SiI9022A/SiI9024A transmitter should be the same as the

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host IOVCC, and IO_SEL should be set to the correct value, as described for the signal in the Configuration and Control Signals section.

The 49-ball package is hardwired to be used with IOVCC = 1.8 V only.

3.3. DC Specifications

3.3.1. Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 3.3. DC Digital I/O Specifications: IOVCC = 1.8 V

In the 81-ball and 72-pin package, IO_SEL is tied to 1.8 V.

Symbol	Parameter	Signal Type	Signal Name[3]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level input voltage	LVTTL	CEC_D CI2CA IO_SEL	—	1.2	—	—	V	—
V_{IL}	LOW-level input voltage			—	—	—	0.60	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	IDCK HS VS DE D[23:0]	—	—	—	0.68	V	—
V_{TH+}	LOW to HIGH threshold				1.25	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	MCLK SCK SD[3:0] WS SPDIF	—	—	—	0.45	V	—
V_{TH+}	LOW to HIGH threshold				1.20	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	HPD	—	—	—	0.65	V	—
V_{TH+}	LOW to HIGH threshold				1.9	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	RESET#	—	—	—	0.50	V	—
V_{TH+}	LOW to HIGH threshold				1.2	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	CSCL CSDA	—	—	—	0.50	V	—
V_{TH+}	LOW to HIGH threshold				1.32	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	DSCL DSDA	—	—	—	1.5	V	—
V_{TH+}	LOW to HIGH threshold				3.0	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	CEC_A	—	—	—	0.51	V	—
V_{TH+}	LOW to HIGH threshold				1.15	—	—	V	
V_{OH}	HIGH-level output voltage	LVTTL	INT	—	1.4	—	—	V	4
V_{OL}	LOW-level output voltage				—	—	0.3	V	
V_{OLOD}	LOW-level output voltage	Open Drain	INT	—	—	—	0.3	V	4
V_{CINL}	Input clamp voltage	—	—	I_{CL} = –18 mA	—	—	GND – 0.8	V	2, 5
V_{CIPL}	Input clamp voltage	—	—	I_{CL} = 18 mA	—	—	V_{CC} + 0.8	V	2, 5
I_{IL}	Input leakage current	—	—	High impedance	–10	—	10	µA	2, 9
I_{OL}	Output drive current	Open Drain	DSCL DSDA	V_{OUT} = 0.4 V	3	—	—	mA	6, 8
I_{OL}	Output drive current	Open Drain	CSCL CSDA	V_{OUT} = 0.4 V	4	—	—	mA	6, 8
I_{OL}	Output drive current	Open Drain	CEC_A	V_{OUT} = 0.4 V	3.5	—	—	mA	
I_{OL}	Output drive current	Open Drain	CEC_D	V_{OUT} = 0.4 V	2.0	—	—	mA	
I_{OL}	Output drive current	LVTTL	INT	V_{OUT} = 0.4 V	4	—	—	mA	6
I_{OH}	Output drive current	LVTTL	INT	V_{OUT} = 1.4 V	4	—	—	mA	—

Note: See notes under Table 3.4.

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Table 3.4. DC Digital I/O Specifications: IOVCC = 3.3 V

In the 81-ball and 72-pin package, IO_SEL is connected to ground.

Symbol	Parameter	Signal Type	Signal Name[3]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level input voltage	LVTTL	CEC_D CI2CA IO_SEL	—	2.0	—	—	V	—
V_{IL}	LOW-level input voltage				—	—	0.80	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	IDCK HS VS DE D[23:0]	—	—	—	1.25	V	—
V_{TH+}	LOW to HIGH threshold				2.1	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	MCLK SCK SD[3:0] WS SPDIF	—	—	—	0.75	V	—
V_{TH+}	LOW to HIGH threshold				1.80	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	HPD	—	—	—	0.80	V	—
V_{TH+}	LOW to HIGH threshold				1.85	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	RESET#	—	—	—	0.85	V	—
V_{TH+}	LOW to HIGH threshold				1.75	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	CSCL CSDA	—	—	—	0.70	V	—
V_{TH+}	LOW to HIGH threshold				1.77	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	DSCL DSDA	—	—	—	1.5	V	—
V_{TH+}	LOW to HIGH threshold				3.0	—	—	V	
V_{TH-}	HIGH to LOW threshold	Schmitt	CEC_A	—	—	—	0.8	V	—
V_{TH+}	LOW to HIGH threshold				1.83	—	—	V	
V_{OH}	HIGH-level output voltage	LVTTL	INT	—	2.4	—	—	V	4
V_{OL}	LOW-level output voltage				—	—	0.4	V	
V_{OLOD}	LOW-level output voltage	Open Drain	INT	—	—	—	0.4	V	4, 8
V_{CINL}	Input clamp voltage	—	—	I_{CL} = –18 mA	—	—	GND – 0.8	V	2, 5
V_{CIPL}	Input clamp voltage	—	—	I_{CL} = 18 mA	—	—	VCC + 0.8	V	2, 5
I_{IL}	Input leakage current	—	—	High impedance	–10	—	10	µA	2, 9
I_{OL}	Output drive current	Open Drain	DSCL, DSDA	V_{OUT} = 0.4 V	3	—	—	mA	7, 8
I_{OL}	Output drive current	Open Drain	CSCL, CSDA	V_{OUT} = 0.4 V	4	—	—	mA	7, 8
I_{OL}	Output drive current	Open Drain	CEC_A	V_{OUT} = 0.4 V	3.5	—	—	mA	
I_{OL}	Output drive current	Open Drain	CEC_D	V_{OUT} = 0.4 V	2.0	—	—	mA	
I_{OL}	Output drive current	LVTTL	INT	V_{OUT} = 0.4 V	4	—	—	mA	7
I_{OH}	Output drive current	LVTTL	INT	V_{OUT} = 2.4 V	4	—	—	mA	—

Notes to Table 3.3 and Table 3.4:

1. Guaranteed by characterization unless otherwise noted.
2. These limits are guaranteed by design.
3. See the Ball and Pin Diagrams and Descriptions starting on page 26 for signal type designations for all package signals.
4. INT can be programmed as push-pull or open-drain. As a push-pull output, it drives V_{OL} and V_{OH} as defined here.
5. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or for more than one third of the clock cycle, whichever is less. Exceeding the clamp current I_{CL} listed in the Conditions column of the table can result in permanent damage to the chip.
6. Minimum output drive specified at ambient = 85 ºC and IOVCC = 1.7 V. Typical output drive specified at ambient = 25 ºC and IOVCC = 1.8 V. Maximum output drive specified at ambient = 0 ºC and IOVCC = 1.9 V.
7. Minimum output drive specified at ambient = 85 ºC and IOVCC = 3.0 V. Typical output drive specified at ambient = 25 ºC and IOVCC = 3.3 V. Maximum output drive specified at ambient = 0 ºC and IOVCC = 3.6 V.
8. Do not remove IOVCC from the SiI9022A/SiI9024A HDMI Transmitter unless the attached I^2C bus is completely idle.
9. Current leakage for input pins including audio and video pins will not exceed this range.

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Table 3.5. TMDS I/O Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units	Notes
V_{OD}	Differential outputs single-ended swing amplitude	TMDS	R_{LOAD} = 50 Ω	400	500	600	mV	1, 2
V_{DOH}	Differential HIGH level output voltage	TMDS	—	—	3.3	—	V	—
I_{DOS}	Differential output short circuit current	TMDS	V_{OUT} = 0 V	—	—	5	µA	—

Note:
1. Limits are defined by the HDMI Specification.
2. R_{EXT_SWING} condition as defined in the Differential Data Signals section.

3.3.2. DC Power Supply Specifications

Table 3.6 and Table 3.7 list the power consumption in both power-down and active modes using different IOVCC supplies. See Table 3.8 for an explanation of the power operating modes.

Table 3.6. Low Power Standby Mode Power Consumption

Symbol	Parameter	Mode	3.3 V IOVCC		1.8 V IOVCC		1.2 V AVCC		1.2 V CVCC		Units	Notes
			Typ[6]	Max	Ty[6]p	Max	Typ[6]	Max	Typ[6]	Max		
I_{PDQ}	Complete power-down current	D3 Cold	0.15	0.20	0.018	0.022	0.05	0.066	0.02	0.025	mA	1, 5
I_{PDQ}	Complete power-down current	D3 Hot	1.00	1.65	0.550	0.670	0.75	0.830	3.50	4.50	mA	1, 5
I_{PDQ}	Quiet power-down current	D2	1.10	1.90	0.580	0.700	0.82	1.15	4.20	5.20	mA	1, 5

Table 3.7. Operating Mode Power Consumption

Symbol	Parameter	Mode	Frequency	3.3 V IOVCC		1.8 V IOVCC		1.2 V AVCC		1.2 V CVCC		Units	Notes
				Typ[6]	Max	Typ[6]	Max	Typ[6]	Max	Typ[6]	Max		
I_{CCT}	Transmitter supply current	D0 Single-Edge Mode	74.25 MHz	4.0	5.4	1.0	2.4	7.5	11.8	18.0	26.7	mA	2, 3
			148.5 MHz	5.3	8.9	1.7	3.4	15.4	19.9	32.0	43.4	mA	2, 3
			162 MHz	5.0	8.7	1.5	3.2	16.5	20.9	33.0	45.6	mA	2, 3
		D0 Dual-Edge Mode	74.25 MHz	4.2	5.4	1.3	2.4	9.5	11.8	20.0	26.7	mA	2, 3
			148.5 MHz	7.3	10.0	2.0	3.9	18.0	20.9	34.0	44.0	mA	2, 3
			162 MHz	7.0	9.6	1.8	3.8	18.2	22.8	36.0	46.4	mA	2, 3

Notes:
1. These values reflect the static device current with no IDCK clock applied.
2. Power is related to input clock (IDCK) frequency.
3. Maximum power limits measured with all power supplies at maximum normal operating conditions, minimum normal operating ambient temperature, R_{EXT_SWING} as defined in the Differential Data Signals section on page 32, and a video pattern of single-pixel vertical lines.
4. Power consumption was measured across all power rails at +10% VCC: IOVCC = 1.98 V or 3.6 V, CVCC12 = 1.32 V, and AVCC12 = 1.32 V.
5. IOVCC, CVCC12, and AVCC12 should not be removed in the low-power modes because input states and leakage current cannot be guaranteed without all power supplies present.
6. Typical power consumption is shown for reference and may vary based on typical pattern usage of system.

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Table 3.8 describes the chip conditions for the various power consuming modes. Refer to the Programmer's Reference for details about setting different power operating modes.

Table 3.8. Power Operating Modes

Mode		Core Running	Outputs Powered	Oscillator Powered	Inputs Switching	Description	Comment
D3 Cold[1, 2]	Complete Power Down	No	No	No	No	Absolute Minimum power.	Can still wake up through HPD, but RSEN wake-up is disabled. Local I²C interface is disabled. Hardware reset is required to re-enable.
D3 Hot[1, 2]	Complete Power Down	Yes	No	No	No	Minimum power.	Can still wake up through HPD and RSEN. Local I²C interface is disabled. Hardware reset is required to re-enable.
D2	Quiet Power Down	Yes	No	Yes	No	Slave I²C bus available for register access.	Monitor events while minimizing transmitter power.
D0	Full Power	Yes	Yes	Yes	Yes	Full function.	Functional mode.

Notes:
1. A full hardware reset is required to wake the system up from D3 Hot or D3 Cold mode.
2. HPD must be low or Cable must not be connected prior to entering D3 Hot/Cold mode for wake-up to be valid.

3.4. AC Specifications

3.4.1. TMDS AC Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 3.9. TMDS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{DDF}	VSYNC and HSYNC delay from DE falling edge	—	1	—	—	T_{CIP}	Figure 4.4	1
T_{DDR}	VSYNC and HSYNC delay to DE rising edge	—	1	—	—	T_{CIP}	Figure 4.4	1
T_{HDE}	DE HIGH time	—	—	—	8191	T_{CIP}	Figure 4.5	1
T_{LDE}	DE LOW time		138	—	—	T_{CIP}	Figure 4.5	1, 3
S_{LHT}	Differential swing LOW-to-HIGH transition Time	R_{LOAD} = 50 Ω	75	—	—	ps	Figure 4.12	2, 4, 5
S_{HLT}	Differential swing HIGH-to-LOW transition Time		75	—	—	ps	Figure 4.12	2, 4, 5

Notes:
1. Guaranteed by design.
2. Guaranteed by characterization.
3. T_{LDE} (DE LOW time) minimum is defined for HDMI mode carrying 480p video with 192 kHz audio, which requires at least 138 pixel clocks of blanking to carry the audio packets. The minimum DE LOW time is 12 clocks for TMDS. For more details, see the Minimum Horizontal Blanking Specification section (page 25). Minimum vertical blanking time is three horizontal line times.
4. Limits are defined by the HDMI Specification.
5. With R_{EXT_SWING} condition as defined in the Differential Data Signals section on page 32.

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3.4.2. Audio AC Timing Specifications

See the notes below Table 3.11.

Table 3.10. I²S Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_I2S}	Sample rate	—	32	—	192	kHz	—
T_{SCKCYC}	I²S cycle time[1]	C_L = 10 pF	360	400	440	ns	Figure 4.8
$T_{SCKHIGH}$	I²S clock HIGH[1]	C_L = 10 pF	110	—	—	ns	—
T_{SCKLOW}	I²S Clock LOW[1]	C_L = 10 pF	110	—	—	ns	—
T_{I2SSU}	I²S setup time[1]	C_L = 10 pF	60	—	—	ns	Figure 4.8
T_{I2SHD}	I²S hold time[1]	C_L = 10 pF	0	—	—	ns	Figure 4.8
$T_{MCLKCYC}$	MCLK cycle time	C_L = 10 pF	13.3	—	—	ns	Figure 4.10
F_{MCLK}	MCLK frequency	C_L = 10 pF	—	—	75	MHz	—
$T_{MCLKDUTY}$	MCLK duty cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$	Figure 4.10

Table 3.11. S/PDIF Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_SPDIF}	Sample rate	—	32	—	192	kHz	—
T_{SPCYC}	S/PDIF cycle time[1]	C_L = 10 pF	—	—	1.0	UI	Figure 4.9
T_{SPDUTY}	S/PDIF duty cycle[1]	C_L = 10 pF	90%	—	110%	UI	Figure 4.9
T_{AUDDLY}	Audio pipeline delay[3]	—	—	30	70	µs	—

Notes:

1. Refer to the I²S or S/PDIF specifications based on 2.5 MHz for I²S receiver.
2. Setup and hold minimum times are based on 13.388 MHz sampling, from Figure 3 of Philips *I²S Specification*.
3. Audio pipeline delay is measured from transmitter input signals to TMDS output. The video path delay is insignificant.
4. I²S and S/PDIF input timing is guaranteed by design to meet the listed specifications at default settings.

3.4.3. Video Input AC Timing Specifications

Table 3.12 lists the video input AC timing specifications when IOVCC is 1.8 V, and covers both package types. Table 3.13 on the next page lists the timing when IOVCC is 3.3 V, and applies only to the 81-ball and 72-pin package. Data for both tables are given for normal operating conditions unless otherwise specified.

Table 3.12. Video Input AC Specifications: 1.8 V IOVCC

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{CIP}	IDCK period, one pixel per clock	—	6	—	40	ns	Figure 4.2	1
F_{CIP}	IDCK frequency, one pixel per clock	—	25	—	165	MHz	—	1
T_{CIP12}	IDCK period, dual-edge clock	—	12	—	40	ns	Figure 9	2
F_{CIP12}	IDCK frequency, dual-edge clock	—	25	—	82.5	MHz	—	2
T_{DUTY}	IDCK duty cycle: 24-bit single-edge clocking	—	30%	—	70%	T_{CIP}	Figure 4.1	—
	IDCK duty cycle: 12-bit dual-edge clocking	—	40%	—	60%			—
T_{IJIT}	Worst case IDCK clock jitter	—	—	—	2.0	ns	—	3, 4
T_{SIDF}	Setup time to IDCK falling edge	Single-edge clocking mode	0	—	—	ns	Figure 4.2	5, 6
T_{HIDF}	Hold time to IDCK falling edge		1.8	—	—	ns	Figure 4.2	6
T_{SIDR}	Setup time to IDCK rising edge		0	—	—	ns	Figure 4.2	5, 7
T_{HIDR}	Hold time to IDCK rising edge		2.0	—	—	ns	Figure 4.2	7
T_{SIDF}	Setup time to IDCK falling edge	12-bit dual-edge clocking mode	0	—	—	ns	Figure 9	8
T_{HIDF}	Hold time to IDCK falling edge		2.1	—	—	ns	Figure 9	8
T_{SIDR}	Setup time to IDCK rising edge		0	—	—	ns	Figure 9	8
T_{HIDR}	Hold time to IDCK rising edge		2.5	—	—	ns	Figure 9	8

Note: See notes for Table 3.13.

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Table 3.13. Video Input AC Specifications: 3.3 V IOVCC

3.3 V IOVCC ± 10% unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{CIP}	IDCK period, one pixel per clock	—	6	—	40	ns	Figure 4.2	1
F_{CIP}	IDCK frequency, one pixel per clock	—	25	—	165	MHz	—	1
T_{CIP12}	IDCK period, dual-edge clock	—	12	—	40	ns	Figure 9	2
F_{CIP12}	IDCK frequency, dual-edge clock	—	25	—	82.5	MHz	—	2
T_{CIP12A}	IDCK period, dual-edge clock	—	6	—	40	ns	Figure 9	2
F_{CIP12A}	IDCK frequency, dual-edge clock	—	25	—	165	MHz	—	2
T_{DUTY}	IDCK duty cycle: 24-bit single-edge clocking	—	30%	—	70%	T_{CIP}	Figure 4.1	—
	IDCK duty cycle: 12-bit dual-edge clocking	—	40%	—	60%			—
T_{CH}	Clock HIGH time, dual-edge clocking	F_{CIP} > 82.5 MHz	3.6	—	—	ns	Figure 4.1	—
T_{CL}	Clock LOW time, dual-edge clocking		2.4	—	—	ns		
T_{IJIT}	Worst case IDCK clock jitter	—	—	—	2.0	ns	—	3, 4
T_{SIDF}	Setup time to IDCK falling edge	Single-edge clocking mode	0	—	—	ns	Figure 4.2	5, 6
T_{HIDF}	Hold time to IDCK falling edge		1.8	—	—	ns	Figure 4.2	6
T_{SIDR}	Setup time to IDCK rising edge		0	—	—	ns	Figure 4.2	7
T_{HIDR}	Hold time to IDCK rising edge		2.0	—	—	ns	Figure 4.2	7
T_{SIDF}	Setup time to IDCK falling edge	12-bit dual-edge clocking mode	0	—	—	ns	Figure 9	8
T_{HIDF}	Hold time to IDCK falling edge		1.9	—	—	ns	Figure 9	8
T_{SIDR}	Setup time to IDCK rising edge		0	—	—	ns	Figure 9	8
T_{HIDR}	Hold time to IDCK rising edge		2.4	—	—	ns	Figure 9	8

Notes:

1. T_{CIP} and F_{CIP} apply in single-edge clocking modes. T_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
2. T_{CIP12}, T_{CIP12A}, F_{CIP12}, and F_{CIP12A} apply in dual-edge mode. T_{CIP12} and T_{CIP12A} are not controlling specifications.
3. Input clock jitter is estimated by triggering a digital scope at the rising edge of input clock, and measuring peak-to-peak time spread of the rising edge of the input clock 1 µs after the triggering.
4. Actual jitter tolerance can be higher depending on the frequency of the jitter.
5. Setup and hold time specifications apply to D[23:0] (81-ball and 72-pin package) or D[15:0] (49-ball package), DE, VSYNC, and HSYNC input signals, relative to IDCK input clock.
6. Edge Select bit = 0.
7. Edge Select bit = 1.
8. Setup and hold limits are not affected by the Edge Select bit setting for 12-bit dual-edge clocking mode. (See the Programmer's Reference for information about the Edge Select bit setting.)

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3.4.4. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 3.14. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{RESET}	RESET# signal LOW time required for reset	—	100	—	—	µs	Figure 4.6 Figure 4.7	1
T_{I2CDVD}	SDA data valid delay from SCL falling edge on READ command	C_L = 400 pF	—	—	700	ns	Figure 4.13	2, 4
T_{HDDAT}	I²C data hold time	40–400 kHz	2.0	—	—	ns	—	3, 4
T_{INT}	Response time for INT output signal from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	—	—	100	µs	Figure 4.14	5
F_{DSCL}	Frequency on master DDC SCL signal	—	40	70	100	kHz	—	6
F_{CSCL}	Frequency on CSCL signal	—	40	—	400	kHz	—	—

Notes:

1. Reset on RESET# signal can be LOW as CVCC12 and IOVCC become stable, or be pulled LOW for at least T_{RESET}.
2. All standard-mode (100 kHz) I²C timing requirements are guaranteed by design and comply with the I²C Specification. These timings apply to the slave I²C port (signals CSDA and CSCL) and to the master I²C port (signals DSDA and DSCL) with I²C stall disabled.
3. This minimum hold time is required by CSCL and CSDA signals as an I²C slave. The device does not include the 300 ns internal delay required by the I²C Specification (Version 2.1, Table 5, note 2).
4. Operation of I²C signals above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} described on page 14.
5. During RESET# = LOW, the INT output signal shows whether there is an attached and powered-on TMDS receiver. See the description of the INT signal in the Configuration and Control Signals section on page 31.
6. The Master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I²C Standard Mode, or 100 kHz. Use of the Master DDC block does not require an active IDCK.

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4. Timing Diagrams

Data signals D[23:0] shown are available on the 81-ball and 72-pin device. Substitute D[15:0] for the 49-ball device.

4.1. Input Timing Diagrams

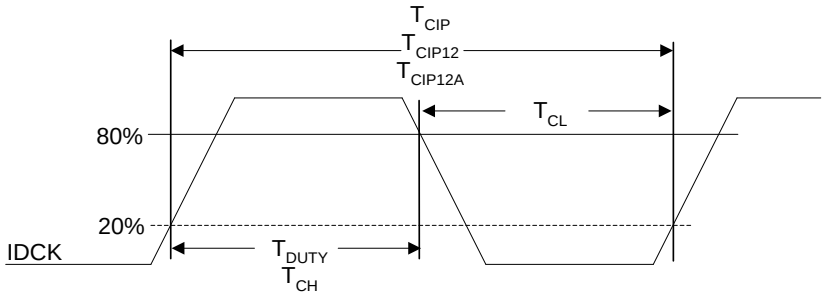
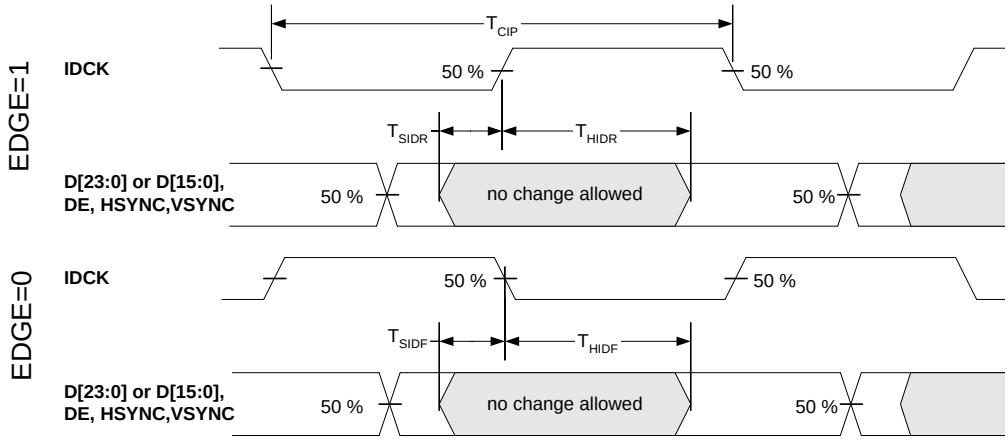


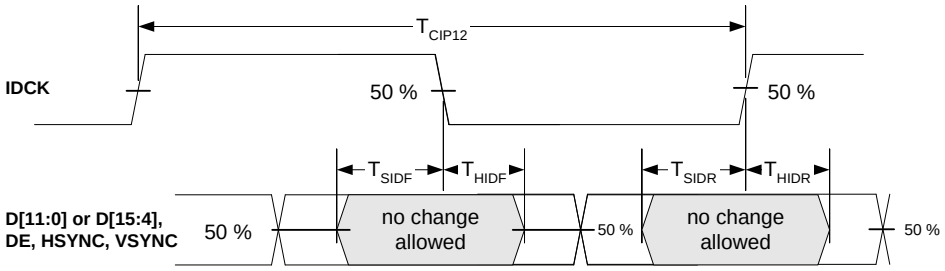
Figure 4.1. IDCK Clock Cycle/High/Low Times



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

D[23:0] are used in the 81-ball and 72-pin package; D[15:0] are used in the 49-ball package.

Figure 4.2. Control and Data Single-Edge Setup/Hold Times to IDCK



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

D[11:0] are used in the 81-ball and 72-pin package; D[15:4] are used in the 49-ball package.

Figure 4.3. Dual-Edge Setup/Hold Times to IDCK

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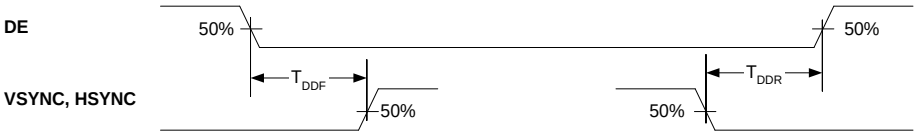

Figure 4.4. VSYNC and HSYNC Delay Times from/to DE

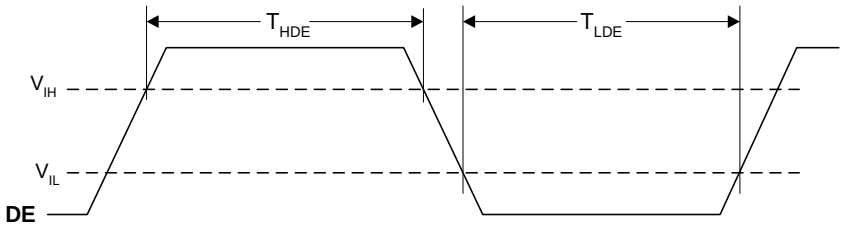

Figure 4.5. DE High/Low Times

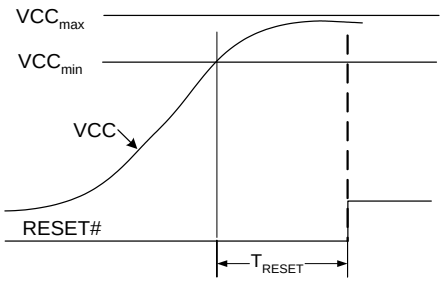

Figure 4.6. Conditions for Use of RESET#

Note: VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# goes HIGH.

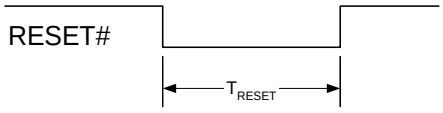

Figure 4.7. RESET# Minimum Timings

Note: RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (as shown in Figure 4.6), or by pulling RESET# LOW from a HIGH state (as shown in Figure 4.7) for at least T_{RESET}.

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4.2. Audio Timing Diagrams

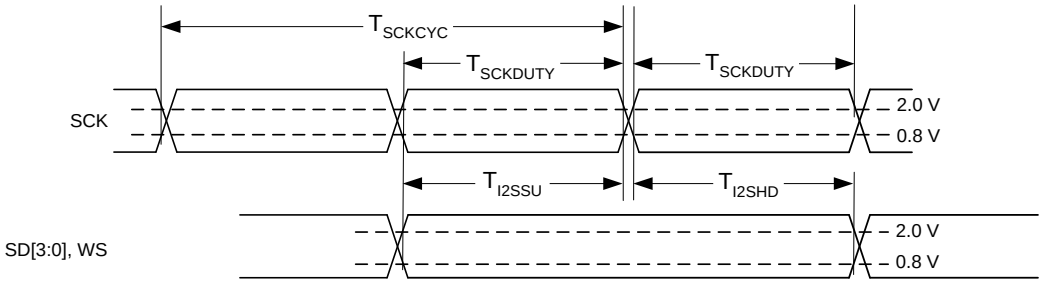

Figure 4.8. I²S Input Timings

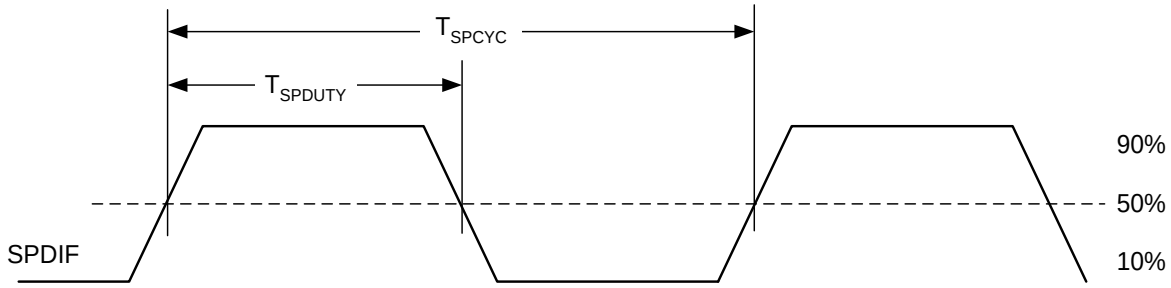

Figure 4.9. S/PDIF Input Timings

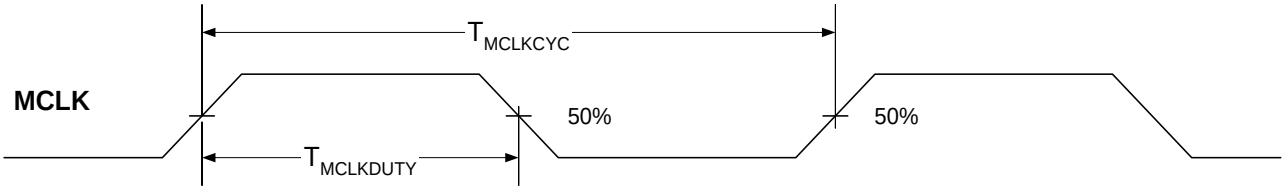

Figure 4.10. MCLK Timings

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4.3. Power Supply Sequencing

Power sequencing is not usually required. Lattice Semiconductor recommends that all individual power supplies reach their nominal levels within 5 ms in normal operation. Once powered on, the IOVCC, CVCC, and AVCC power supplies should not be removed during any power mode including D0, D2, D3 Hot and D3 Cold.

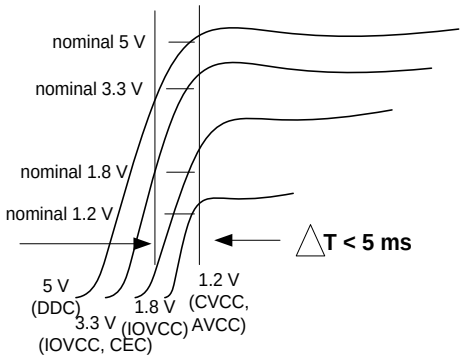

Figure 4.11. Power Supply Sequencing

4.3.1. Output Timing Diagrams

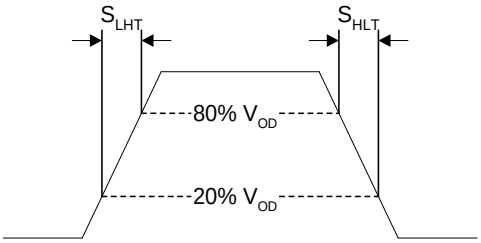

Figure 4.12. Differential Transition Times

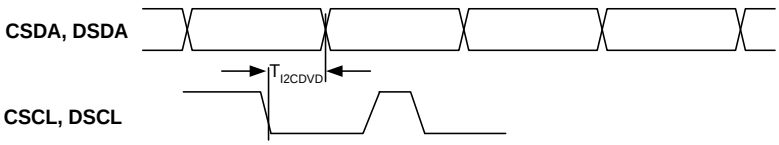

Figure 4.13. I²C Data Valid Delay (Driving Read Cycle Data)

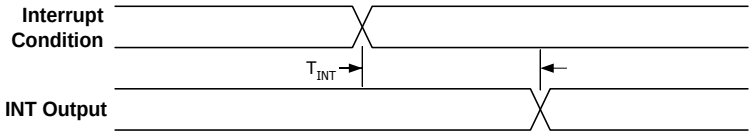

Figure 4.14. INT Output Signal Response to Interrupt Condition

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4.4. Minimum Horizontal Blanking Specification

Several cases define the minimum blanking time requirements. Vertical blanking times are normally multiples of the horizontal line times and do not place a constraint on performance. (HDMI requires at least two line times in each vertical blanking interval.) The minimum horizontal blanking time depends on the mode. An HSYNC or VSYNC edge can occur in any clock cycle except when active video data is being transmitted. When HDMI is active, this includes the two clocks of leading guard band for the active video data.

Table 4.1. Minimum Horizontal Blanking Calculations

Mode	Information Type	Clock Count
DVI Only Defined by transmitter data sheet.	Total minimum horizontal blanking time	12
HDMI with No Data Islands Defined by HDMI Spec (Section 5.2.3.2, page 46; and Figure 5-3).	Minimum control period	12
	Leading guard band	2
	Total minimum horizontal blanking time	14
HDMI with One Data Island HDMI allows a minimum of one data island, which can contain one data packet.	Minimum control period	12
	Leading guard band	2
	Packet	32
	Trailing guard band	2
	Minimum control period	12
	Leading guard band	2
	Total minimum horizontal blanking time	62

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5. Ball and Pin Diagrams and Descriptions

5.1. Ball and Pin Diagrams

5.1.1. 81-Ball VFBGA Package

Figure 5.1 shows the ball diagram for the SiI9022A/SiI9024A transmitter in the 81-ball package. See the Ball and Pin Descriptions beginning on page 29 for a description of the ball functions. Balls are shaded using the grouping shown in Figure 5.3 on page 28.

	1	2	3	4	5	6	7	8	9
A	CEC_A	RSVDHO	AGND	TX1+	TX0+	TXC+	TXC-	AGND	EXT_SWING
B	CI2CA	VDDQ	TX2+	TX2-	TX1-	TX0-	CEC_D	IO_SEL	RSVDL
C	CSDA	CSCL	RESET#	CVCC12	IOGND	AVCC12	AVCC12	DSDA	DSCL
D	CGND	CGND	CVCC12	IOGND	IOVCC	IOGND	CVCC12	HPD	INT
E	D23	D22	D21	D20	IOVCC	SD1	CVCC12	IOVCC	IOVCC
F	D19	D18	D17	D16	CVCC12	SD2	SCK	WS	SD0
G	D15	D14	D9	D7	CGND	CVCC12	SPDIF	MCLK	SD3
H	D12	D11	IDCK	D6	CGND	D3	D1	D0	VSYNC
J	D13	D10	D8	D5	CGND	D4	D2	DE	HSYNC

Figure 5.1. 81-Ball Package Ball Diagram (Top View)

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5.1.2. 49-Ball VFBGA Package

Figure 5.2 shows the ball diagram for the SiI9022A/SiI9024A transmitter in the 49-ball package. See the Ball and Pin Descriptions beginning on page 29 for a description of the ball functions. Balls are shaded using the grouping shown in Figure 5.3 on the next page.

	1	2	3	4	5	6	7
A	TX2+	TX1+	TX1-	TX0+	TX0-	TXC+	TXC-
B	CEC_A	TX2-	AGND	AVCC12	DSDA	RSVDL	EXT_SWING
C	CSDA	CSCL	VDDQ	CVCC12	RESET#	INT	DSCL
D	D15	D14	IOGND	CGND	HPD	WS	SD0
E	D13	D12	IOVCC	D6	SCK	D0	MCLK
F	D11	D10	IDCK	D5	D1	D2	VSYNC
G	D9	D8	D7	D4	D3	DE/SPDIF	HSYNC

Figure 5.2. 49-Ball Package Ball Diagram (Top View)

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5.1.3. 72-Pin QFN Package

Figure 5.3 shows the pin diagram for the SiI9022A/SiI9024A transmitter in the 72-pin package. See the Ball and Pin Descriptions beginning on page 29 for a description of the pin functions.

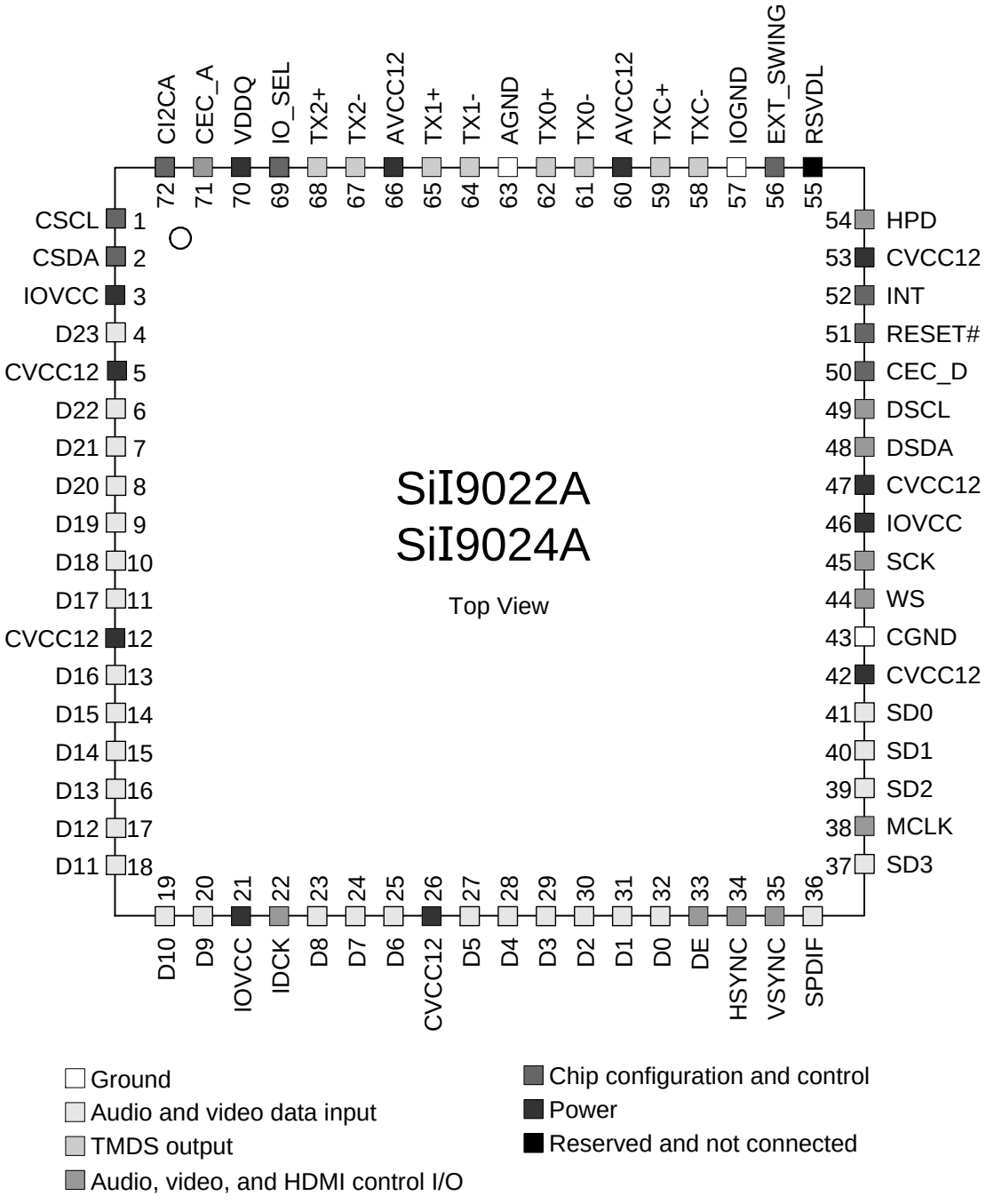

Figure 5.3. 72-Pin Package Pin Diagram (Top View)

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5.2. Ball and Pin Descriptions

5.2.1. Video Input

The digital video input signals all operate from the IOVCC power plane and are tolerant up to the voltage supplied to that plane (1.8 V or 3.3 V). These balls or pins have internal weak pull-down resistors, and are high-impedance in D3 power-down mode.

Name	VFBGA		QFN	Type	Dir	Description	
	49-Ball	81-Ball	72-Pin			81-Ball / 72-Pin	49-Ball
D0	E6	H8	32	Schmitt	Input	12-bit Input Pixel Data Bus. These pins or balls are used in 12-bit dual-edge mode and in 24-bit single-edge mode.	16-bit Input Pixel Data Bus.
D1	F5	H7	31				
D2	F6	J7	30				
D3	G5	H6	29				
D4	G4	J6	28				
D5	F4	J4	27				
D6	E4	H4	25				
D7	G3	G4	24				
D8	G2	J3	23				
D9	G1	G3	20				
D10	F2	J2	19				
D11	F1	H2	18				
D12	E2	H1	17	Schmitt	Input	12-bit Input Pixel Data Bus. These pins or balls are used only in 24-bit single-edge mode. In 12-bit dual-edge mode these signals should be left unconnected.	
D13	E1	J1	16				
D14	D2	G2	15				
D15	D1	G1	14				
D16	NA	F4	13				
D17	NA	F3	11				
D18	NA	F2	10				
D19	NA	F1	9				
D20	NA	E4	8				
D21	NA	E3	7				
D22	NA	E2	6				
D23	NA	E1	4				
IDCK	F3	H3	22	Schmitt	Input	Input Data Clock.	
DE	NA	J8	33	Schmitt	Input	Data Enable input control signal.	
DE/SPDIF	G6	NA	NA	Schmitt	Input	Input DE Control Signal or S/PDIF.	
HSYNC	G7	J9	34	Schmitt	Input	Horizontal sync input control signal.	
VSYNC	F7	H9	35	Schmitt	Input	Vertical sync input control signal.	

Note: Any unused video or control balls or pins listed in this section should be left not connected to conserve power.

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5.2.2. Audio Input

The digital audio input signals all operate from the IOVCC power plane, and are tolerant up to the voltage supplied to that plane (1.8 V or 3.3 V). These balls or pins have weak internal pull-up resistors, and are high-impedance in D3 power-down mode.

Name	VFBGA		QFN	Type	Dir	Description
	49-Ball	81-Ball	72-Pin			
SCK	E5	F7	45	Schmitt	Input	I²S Serial Clock.
WS	D6	F8	44	Schmitt	Input	I²S Word Select.
SD0	D7	F9	41	Schmitt	Input	I²S Serial Data 0.
SD1	NA	E6	40	Schmitt	Input	I²S Serial Data 1.
SD2	NA	F6	39	Schmitt	Input	I²S Serial Data 2.
SD3	NA	G9	37	Schmitt	Input	I²S Serial Data 3.
MCLK	E7	G8	38	Schmitt	Input	Audio Input Master Clock.
SPDIF	NA	G7	36	Schmitt	Input	S/PDIF Audio Input.
DE/SPDIF	G6	NA	NA	Schmitt	Input	S/PDIF audio or DE control input. (Applies to 49-ball package only.)

Note: Any unused audio balls or pins listed in this section should be left not connected to conserve power. All data, clock, and control inputs in this section have a weak internal pullup, which is switched off in D3 mode to reduce leakage current.

5.2.3. CEC

The CEC signals operate from an internally generated power plane, but are tolerant up to the 3.3 V power specified for CEC.

Name	VFBGA		QFN	Type	Dir	Description
	49-Ball	81-Ball	72-Pin			
CEC_A	B1	A1	71	CEC-compliant	Input/ Output	HDMI compliant CEC I/O to interface to CEC devices. CEC electrically compliant I/O. This ball or pin connects to the CEC signal of all HDMI connectors in the system. ***For IOVCC = 3.3 V:*** No external pullup resistor is required. ***For IOVCC = 1.8 V:*** A 51 kΩ pullup resistor in series with a Schottky diode to a 3.3 V source is required; see Figure 7.5 on page 70. As an input, the pad acts as a LVTTL Schmitt triggered input. As an output, the pad acts as an NMOS driver.
CEC_D	NA	B7	50	LVTTL	Input/ Output	CEC interface to local system. This is an LVTTL I/O with a weak pull-up resistor. This ball or pin typically connects to the local CPU. The CEC_D output can be disabled with programming to allow the internal CEC logic to handle the CEC_A signal.

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5.2.4. Configuration and Control

The configuration and control input and output signals all operate from the IOVCC 1.8 V or 3.3 V power plane, and are tolerant up to and drive to the voltage supplied to that plane.

The CSCL, CSDA, DSCL, and DSDA signals are not true open-drain buffers. When no VCC is applied to the chip, these signals can continue to draw a small current, and prevent the master IC from communicating with other devices on the I^2C bus. Therefore, do not remove VCC from the SiI9022A/SiI9024A HDMI Transmitter unless the attached I^2C bus is completely idle. Note that the level on the CI2CA signal is not latched internally and should not be changed during any active I^2C operations.

Name	VFBGA		QFN	Type	Dir	Description
	49-Ball	81-Ball	72-Pin			
HPD	D5	D8	54	Schmitt 5 V tolerant	Input	Hot Plug Detect Input. An external 10 kΩ pulldown resistor to GND on the board is required.
INT	C6	D9	52	LVTTL	Output	Interrupt Output. Configurable by a register setting to be either an active-HIGH (push-pull) output or an active-LOW (open-drain) output. In push-pull mode, the output drives to the corresponding level for the IOVCC power plane. In active-LOW (default) output, an external pull-up to 3.3 V is required.
CI2CA	NA	B1	72	LVTTL	Input	I^2C Device Address Select. ***For 49-ball package:*** Not available. Fixed LOW internally. ***For 81-ball and 72-pin package:*** A 4.7 kΩ external pull-down to GND or pull-up resistor to IO_SEL voltage level MUST be connected to this signal for proper operation. See the Control and Configuration section on page 11 for additional information
RESET#	C5	C3	51	Schmitt	Input	Reset signal (active LOW). When RESET# is LOW, all input and output pins are not functional.
CSCL	C2	C2	1	Schmitt Open-drain	Input/ Output	Local I^2C Bus Clock. This bus accesses the compatible mode registers, the TPI registers, and the CPI registers. An external 4.7 kΩ pullup resistor on the board is required.
CSDA	C1	C1	2	Schmitt Open-drain	Input/ Output	Local I^2C Bus Data. This accesses the compatible mode registers, the TPI registers, and the CPI registers.. An external 4.7 kΩ pullup resistor on the board is required.
IO_SEL	NA	B8	69	LVTTL	Input	I/O Select. This input sets the I/O thresholds to the proper level to match the I/O supply voltage. LOW – Selects 3.3 V I/O thresholds. HIGH – Selects 1.8 V I/O thresholds. Connect IO_SEL to 1.8 V to select 1.8 V I/O threshold and to ground to select 3.3 V I/O threshold.

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5.2.5. DDC Bus

The DDC signals operate from an internally generated power plane, but are tolerant up to the 5 V power specified for DDC.

Name	VFBGA		QFN	Type	Dir	Description
	49-Ball	81-Ball	72-Pin			
DSCL	C7	C9	49	Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C Bus Clock. This bus accesses the EDID and HDCP data on an attached sink device. The DSCL signal is bi-directional, since the transmitter monitors the state of DSCL so that it can accommodate I²C clock stretching by the slave device. An external pullup resistor between 1.8 kΩ and 2.2 kΩ on the board is required.
DSDA	B5	C8	48	Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C Bus Data. This bus accesses the EDID and HDCP data on an attached sink device. An external pullup resistor between 1.8 kΩ and 2.2 kΩ on the board is required.

5.2.6. Differential Data

Name	VFBGA		QFN	Type	Dir	Description
	49-Ball	81-Ball	72-Pin			
TX0+	A4	A5	62	TMDS	Output	TMDS output data pairs.
TX0-	A5	B6	61	TMDS	Output	
TX1+	A2	A4	65	TMDS	Output	
TX1-	A3	B5	64	TMDS	Output	
TX2+	A1	B3	68	TMDS	Output	
TX2-	B2	B4	67	TMDS	Output	
TXC+	A6	A6	59	TMDS	Output	TMDS output clock pair.
TXC-	A7	A7	58	TMDS	Output	
EXT_SWING	B7	A9	56	Analog	Input	Voltage Swing Adjust. A resistor (R_{EXT_SWING}) is connected from this ball or pin to GROUND. This resistor determines the amplitude of the voltage swing. The recommended value is 4.3 kΩ ±1% with internal source termination enabled and 5.1 kΩ ±1% without internal source termination. The value of this resistor can be adjusted to optimize the signal swing in the specific design.

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5.2.7. Power and Ground

Name	VFBGA		QFN	Type	Description
	49-Ball	81-Ball	72-Pin		
CVCC12	C4	C4, D3, D7, E7, F5, G6	5, 12, 26, 42, 47, 53	Power	Digital Core VCC. Connect to 1.2 V supply.
CGND	D4	D1, D2, G5, H5, J5	43	Ground	Digital Core GND.
IOVCC	E3	D5, E5, E8, E9	3, 21, 46	Power	I/O VCC. Connect to either the 1.8 V or 3.3 V supply. This ball must be connected to 1.8 V in the 49-ball package.
IOGND	D3	C5, D4, D6	57	Ground	I/O GND.
AVCC12	B4	C6, C7	60, 66	Power	Analog VCC. Connect to 1.2 V supply.
AGND	B3	A3, A8	63	Ground	Analog GND.
RSVDH0	NA	A2	NA	No connect	Reserved. This ball is not connected in the 81-ball package for downward compatibility with the SiI9022A/SiI9024A transmitter. It can be left open, or connected to ground or CVCC12 without adverse effect.
RSVDL	B6	B9	55	LVTTL Input	Reserved. Must be tied LOW.
VDDQ	C3	B2	70	LVTTL Input	Reserved. Must be tied LOW.

Note: The 72-pin QFN package has an e-Pad which ***must*** be connected to the ground plane of the board.

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6. Feature Information

6.1. RGB to YCbCr Color Space Converter

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. Table 6.1 lists the conversion formulas that are used. The HDMI AVI packet defines the color space of the incoming video.

Table 6.1. RGB to YCbCr Conversion Formulas

Video Format	Conversion	Formulas
		CE Mode 16-235 RGB
640 × 480	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
480i	ITU-R BT.601	
576i	ITU-R BT.601	
480p	ITU-R BT.601	
576p	ITU-R BT.601	
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	

6.2. YCbCr to RGB Color Space Converter

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to the detailed formulas in Table 6.2. Note the difference between RGB range for CE modes and PC modes.

Table 6.2. YCbCr-to-RGB Conversion Formulas

Format change	Conversion	YCbCr Input Color Range
YCbCr 16-235 Input to RGB 16-235 Output	**601***	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
	709[1]	R′ = Y + 1.540(Cr – 128) G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input to RGB 0-255 Output	**601**	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

***Note:** No clipping can be done.

6.3. 3D Video Formats

The SiI9022A/SiI9024A transmitter supports the 3D video modes described in the HDMI 1.4a Specification. All modes support RGB 4:4:4, YCbCr 4:2:2, and YCbCr 4:4:4 color formats and 8-bit color depth. External separate HSYNC, VSYNC, and DE signals can be supplied, or these signals can be supplied as embedded EAV/SAV sequences in the video stream. Table 6.3 lists only the maximum possible resolution with a given frame rate; for example, Side-by-Side mode is defined for 1080p60, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means

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that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz and its associated pixel frequency is supported.

6.3.1. Limitations

Frame Packing format: The Frame packing format requires Vact_space which must have constant video data. Dithering should be disabled when transmitting the frame packing format.

The 1080p 24 Hz video format has a total of 2250 lines. However, the VRES counter (TPI 0x6C, 0x6D) of the SiI9022A/SiI9024A device is only 11 bits, which provides for a maximum of 2047 lines. In this case, the VRES counter will overflow and show the value of 0. This does not affect the output of the transmitter.

The DE generator is supported for all formats except 1080p 24 Hz. DE_LIN (TPI 0x68, 0x69) is only 11 bits (maximum 2047) while this value for 1080p 24 Hz should be 2205 lines.

Side-by-Side format: L frame and R frame are concatenated without a border. Since 4:4:4 to 4:2:2 downsampling and 4:2:2 dithering and upsampling to 4:4:4 has a decimation filter and looks at some adjacent pixels, these three features should be avoided to prevent possible visible artifacts.

L + Depth format: No video processing should be used.

Top-and-Bottom format: There are no limitations.

Table 6.3. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	24	148.5
		720p	50 / 60	
	interlaced	1080i	50 / 60	
L + Depth	—	1080p	24	
		720p	50/60	
Side-by-Side	Full	1080i	50/60	
		720p	50/60	
	Half	1080p	50/60	
		1080p	24	74.25
		720p	50/60	
		1080i 50/60	60	
Top-and-Bottom	—	1080p	24	
		720p	50/60	

6.4. S/PDIF Audio Input

The S/PDIF stream carries 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic described in the Audio Data Capture Logic section packetizes the audio data according to the HDMI specification. The S/PDIF input supports audio sampling rates from 32 to 192 kHz. No clock input is required for S/PDIF since the chip logic extracts the clock from the incoming S/PDIF data stream. Optionally, an external MCLK source can be used.

6.5. I²S Audio Inputs

The 81-ball and 72-pin packages support four I²S inputs, SD0 through SD3, which allow transmission of DVD-Audio and decoded Dolby Digital/DTS bit stream to A/V receivers and high-end displays. This interface supports 2-channel to 8-channel audio with up to 192 kHz sampling rate. The input clock SCK is used to latch the incoming data; data must meet specified setup and hold time requirements with respect to SCK.

The 49-ball package has only one I²S input, SD0, which supports only 2-channel audio up to 192 kHz sampling rate.

A separate master clock signal that is coherent with the I²S inputs is required for HDMI time-stamping purposes. *Coherent* means that this clock signal and the I²S inputs must have been created from the same clock source. This clock

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can be generated internally, using a PLL. As an option, the original MCLK signal used to strobe the I²S signals out from the sourcing chip can be used. If the internal PLL is used, then an external MCLK input is not required.

6.6. Supported Audio Sampling Rates

The audio data can be down-sampled by one-half or one-fourth with register control. This feature allows the transmitter to share the audio bus with a high-sample-rate audio DAC, while down-sampling audio for an attached display that supports only lower rates. The transmitter supports conversions from 192 to 48 kHz, 176.4 to 44.1 kHz, 96 to 48 kHz, and 88.2 to 44.1 kHz.

The appropriate registers must be configured to describe the format of audio provided to the transmitter. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

Table 6.4 lists the supported MCLK frequencies and audio sample rates.

Table 6.4. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs						
	32 kHz[1, 2]	44.1 kHz[1, 2]	48 kHz[1, 2]	88.2 kHz[1, 2]	96 kHz[1, 2]	176.4 kHz[2]	192 kHz[2]
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.869 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	24.576 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz		
1024	32.768 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz	50.803 MHz	55.296 MHz				

Notes:

1. 2-channel S/PDIF supported rate.
2. 2-channel and 8-channel I²S supported rate.

Table 6.5. S/PDIF Audio Formats Supported for each Video Format

Video Format	32 kHz	44.1 kHz	48 kHz		96 kHz	96 kHz→48 kHz	192 kHz
	2-ch	2-ch	2-ch	5.1-ch	2-ch	2-ch	2-ch
VGA	√	√	√	√	√	√	√
480i	√	√	√	√	√	√	√
480p	√	√	√	√	√	√	√
576p	√	√	√	√	√	√	√
720p and above	√	√	√	√	√	√	√

Note: √ = Supported, — = Not Supported

Table 6.6. I²S Audio Formats Supported for each Video Format

Video Format	I²S Format												
	2-Channel Audio									8-Channel Audio (81-Ball and 72-Pin package only)			
	32	44.1	48	88.2	96	96→48	176.4	192	192→48	48	88.2	96	192
VGA	√	√	√	√	√	√	√	√	√	√	—	—	—
480i	√	√	√	√	√	√	√	√	√	√	—	—	—
480p	√	√	√	√	√	√	√	√	√	√	—	—	—
576p	√	√	√	√	√	√	√	√	√	√	—	—	—
480p 2x	√	√	√	√	√	√	√	√	√	√	√	√	—
720p and above	√	√	√	√	√	√	√	√	√	√	√	√	√

Note: √ = Supported, — = Not Supported

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6.7. I²C Register Information

I²C registers monitor and control all functions of the transmitter. For devices in the 81-ball and 72-pin package, the device I²C addresses can be altered setting the CI2CA signal LOW or HIGH as listed in Table 6.7. An external pull-up or pull-down resistor (depending on the desired set of I²C addresses) is used to set the level on the CI2CA signal. Note that the level on the CI2CA signal is not latched internally and should not be changed during any active I²C operations.

The CI2CA signal is not externally accessible on the 49-ball package and is internally connected to ground. As a result, the device I²C addresses for devices in the 49-ball package cannot be changed and are fixed to the same addresses as when the CI2CA signal is LOW.

Table 6.7. Control of I²C Address with CI2CA Signal

Internal Function	CI2CA = LOW	CI2CA = HIGH
	49-Ball / 81-Ball / 72-Pin	81-Ball / 72-Pin
Transmitter Programming Interface (TPI) device address	0x72	0x76
CEC Programming Interface (CPI) device address	0xC0	0xC4
SiI9020-compatible internal registers: first device address	0x72	0x76
SiI9020-compatible internal registers: second device address	0x7A	0x7E

Two separate sets of registers are available for the transmitter subsystem.

- SiI9020-compatible registers are nearly identical to those used by previous generations of Lattice Semiconductor parts. These registers can run under the direct control of existing code on a host processor and are used to perform audio/video format processing, CEA-861D InfoFrame packet formatting, and power-down control. Refer to the *SiI9020 HDMI PanelLink Transmitter Programmer's Reference* (listed in References section) for information about these registers.
- Transmitter Programming Interface (TPI) registers represent a higher-level interface. Lattice Semiconductor recommends using the TPI registers instead of the SiI9020-compatible registers, because they automate in hardware many functions such as audio N-value calculation, HDCP local link authentication and integrity checking, and HDCP repeater authentication. The HDCP feature, which was not available on the SiI9020 transmitter, can only be used through the TPI register interface of the SiI9024A device. Refer to the Programmer's Reference (listed in References section) for information on these registers.

For the CEC subsystem, a set of CEC Programming Interface registers fully automates CEC handling. Refer to the *CEC Programming Interface (CPI) Programmer's Reference* (listed in References section) for information on these registers.

6.8. DDC Support

The Master DDC block supports I²C transactions specified by VESA *Enhanced Display Data Channel Standard* (Section 3.1.2). The Master DDC block complies with the Standard Mode timing of the I²C specification, limited to 100 kHz by Section 8.4.1 of the HDMI specification, and supports slave clock stretching as required by E-DDC. Figure 6.1 below and Figure 7.6 on page 71 show the connection of the HDMI connector to the DDC ports of the transmitter. Figure 6.2 on the next page shows the supported I²C transactions.

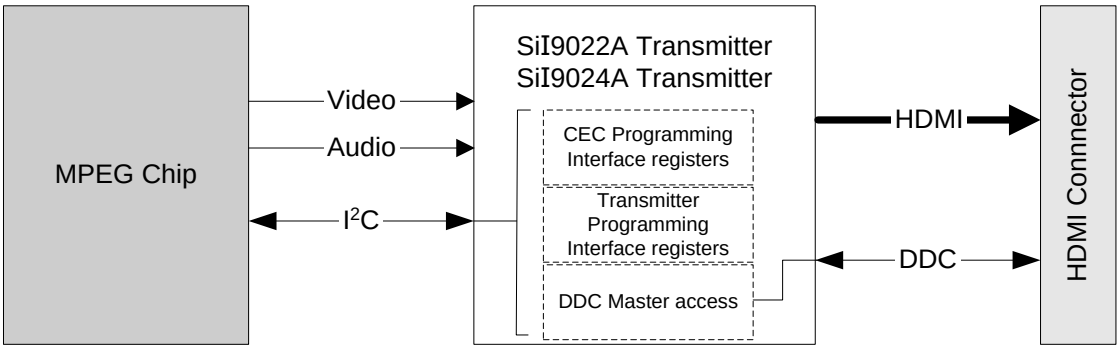

Figure 6.1. Simplified Host I²C Interface using Master DDC Port

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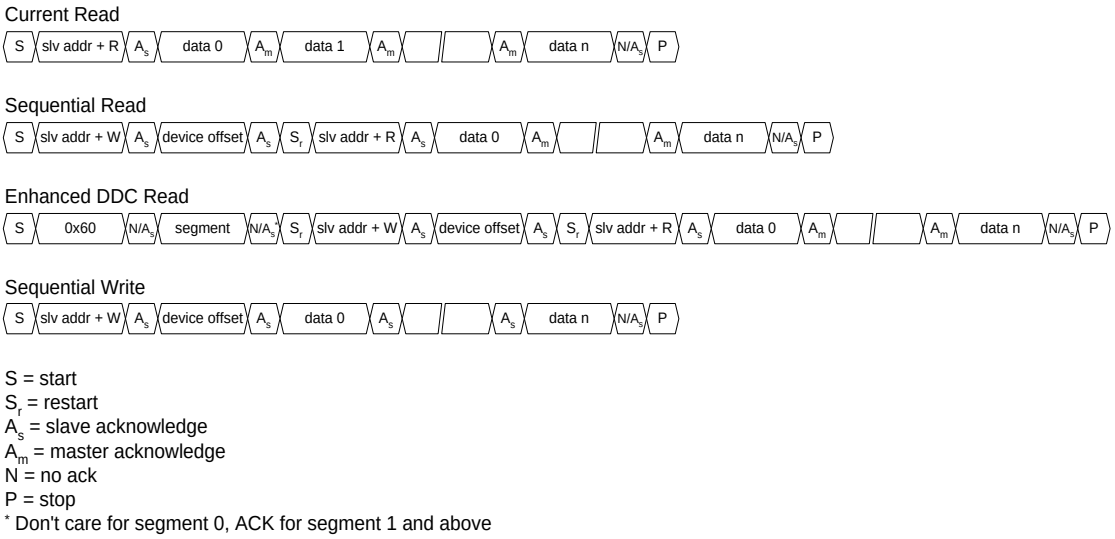

S = start
S_r = restart
A_s = slave acknowledge
A_m = master acknowledge
N = no ack
P = stop
* Don't care for segment 0, ACK for segment 1 and above

Figure 6.2. Master I²C Supported Transactions

6.8.1. DDC Stall Support

Stall feature is also supported on the SiI9022A/SiI9024A device. Stall can be enabled after ACK or on every cycle. This feature can also reduce an incoming 400 kHz Local I²C speed to 100 kHz DDC. Lattice Semiconductor does not recommend enabling this feature when the incoming local I²C speed and DDC speed is set to 100 kHz since additional I²C bus free time is required. Additionally, if a sink device supports I²C speeds higher than 100 kHz, this feature should be disabled.

6.9. Power Saving Modes and Wakeup Feature

In addition to D2 mode, the SiI9022A/SiI9024A device supports 2 additional power saving modes which include the D3 Hot and D3 Cold mode. D3 Hot mode provides better power savings compared to D2 mode. D3 Cold mode offers the best power savings compared to D2 and D3 Hot. Once in D3 Hot or Cold modes, the I²C registers are no longer accessible, and to regain full access to the internal registers, the transmitter must be hardware reset.

The wakeup feature is an additional function to alert the host and re-enable the SiI9022A/SiI9024A device from D3 Cold or D3 Hot mode. The wakeup feature works by sending an INT# signal to the host when an active display sink is connected to the transmitter. The INT# signal is generated when either an active Receiver Sense or a Hotplug signal is detected by the transmitter.

6.9.1. Wakeup Support in D3 Cold and D3 Hot Modes

To enable the wakeup feature in either D3 Hot or D3 Cold mode, adhere to the following sequences; refer to the Programmer's Reference for more details. Table 6.8 below summarizes the detection support of D3 Hot and Cold.

Table 6.8. D3 hot and D3 Cold Feature

Mode		RSEN Detect	Hotplug Detect	Minimum Requirements	Condition
D3 Cold	Complete Power Down	No	Yes	HPD low or Cable Disconnected	HPD only. Cable must be disconnected before entering D3 Cold.
D3 Hot	Complete Power Down	Yes	Yes	RSEN disconnected	Can be used with Display Sinks with multi input ports that disable input but keep HPD high.

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6.9.1.1. D3 Cold Wakeup

The D3 Cold Wakeup feature sends an INT signal when connecting a cable produces a Hotplug signal. Lattice Semiconductor recommends disconnecting the cable to theSiI9022A/SiI9024A transmitter before entering D3 Cold mode.

1. 1. Disconnect the cable.
2. 2. Clear any pending interrupts.
3. 3. Perform a hardware reset of the transmitter.
4. 4. Program register 0xC7 to 0x00 to enter TPI mode.
5. 5. Set INT# source to Hotplug using register 0x3C.
6. 6. Clear any pending interrupts.
7. 7. Enter D3 Cold mode using register 0x1E.

6.9.1.2. D3 Hot Wakeup

Unlike the D3 Cold mode, the D3 Hot mode also supports using RSEN for a wakeup event. This allows the D3 Hot mode to support a different usage model. In a situation where the sink may have additional input ports but may disable the inputs while keeping the Hotplug active or vice versa, a change in either the RSEN or Hotplug signal prompts an INT# signal from the transmitter. The INT# will trigger if there is any change in the HPD signal, such as a HIGH-to-LOW change. Since this is not the intended wakeup event required, the host can choose to re-enter the D3 Hot mode.

8. 1. Cable can be disconnected or left connected.
9. 2. Set INT# source to either RSEN or HPD.
10. 3. Clear any pending interrupts.
11. 4. Enable D3 Hot mode via register 0x1E.

6.10. Common Video Input Formats

Table 6.9 lists the bus interface formats available to support common video input resolutions. The format number in the left column of this table lists the input modes indicated in Table 6.10 on the next page that are required to support each format. Additional discrete CEA and VESA resolutions meeting the requirements listed in Table 3.14 on page 20 and Table 4.1 on page 25 may also be supported.

Table 6.9. Video Input Formats

Format	Input Pixel Clock (MHz)								Notes
	480i[1, 3]	480p[2]	XGA	720p	1080i	1080p24	1080p	UXGA	
1	27	27	65	74.25	74.25	74.25	148.5	162	—
2	27	27	65	74.25	74.25	74.25	—	—	—
3	27	27	—	74.25	74.25	74.25	148.5	162	—
4	27	54	—	148.5	148.5	148.5	—	—	—
5	—	54	—	—	—	—	—	—	4

Notes:

1. 480i support also encompasses 576i support.
2. 480p support also encompasses 576p support.
3. 480i must be input at 27 MHz using pixel replication to be transmitted across the HDMI link.
4. BTA-T1004 format is defined for a single-channel (8/10/12-bit) bus.

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6.11. Data Bus Mappings

The transmitter supports multiple input data mappings. Some have explicit control signals, and some have embedded control signals. The selection of data mapping mode should be consistent at the signals and in the corresponding register settings. Refer to the Programmer's Reference for more details. All versions of this transmitter support up to a maximum of 8-bit color depth in any mode.

Table 6.10. Input Video Formats

Input Mode	Input Format	Data Bus Width	Clock Mode[11]	Sync Signals	Page		Notes
					81-Ball/72-Pin	49-Ball	
RGB 4:4:4	1	24	1x	Separate	42	—	6, 10
YCbCr 4:4:4	2	24	1x	Separate	42	—	1, 6, 10
YC 4:2:2 Separate Syncs	3	16, 20[10], 24[10]	1x	Separate	43	58	2
YC 4:2:2 Embedded Syncs	1	16, 20[10], 24[10]	1x	Embedded	46	59	2, 4
YC MUX 4:2:2 Separate Syncs	3	8, 10[10], 12[10]	2x	Separate	49	60	2, 3, 4, 7
YC MUX 4:2:2 Embedded Syncs	4	8, 10[10], 12[10]	2x	Embedded	51	61	2, 3, 4, 5, 7
RGB 4:4:4	1	12	dual-edge	Separate	54	63	8
YCbCr 4:4:4	1	12	dual-edge	Separate	54	63	1, 8
YC 4:2:2 Separate Syncs	1	8, 10, 12	dual-edge	Separate	55	64	2, 4, 8
YC 4:2:2 Embedded Syncs	1	12	dual-edge	Embedded	53	62	2, 4, 8

Notes:

1. 4:4:4 data contains one Cr, one Cb, and one Y value for every pixel.
2. 4:2:2 data contains one Cr and one Cb value for every two pixels, and one Y value for every pixel.
3. In YC MUX mode, data is input on one or two 8-bit channels. A 2x pixel clock is required.
4. Y and CbCr data can be input on 12 bits (as part of a 24-bit mode or as a 12-bit mode), but the two least-significant bits will be zero since the internal data path is 10 bits wide.
5. Embedded sync decoding extracts the syncs. A 2x pixel clock is required. Note that the DE generator may be needed to convert extracted sync timings to CEA-861D-compliant timings.
6. A 2x pixel clock can also be sent with 4:4:4 data. This is necessary when the receiver is required to reformat such a stream into 4:2:2 data or into a multiplexed YC MUX output format.
7. When sending a 2x pixel clock, the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to the *HDMI Specification*, section 6.4.
8. Dual-edge clocking is allowed for these video mappings. Frequencies above 82.5 MHz dual-edge mode are only supported by the 72-pin QFN package and with IOVCC supplied at 3.3 V ± 10%.
9. The HDMI and the EIA/CEA-861D specifications require virtually every HDMI source to transmit an accurate AVI InfoFrame. Even in the rare cases where it is not absolutely required, Lattice Semiconductor strongly recommends that an AVI InfoFrame be transmitted during every vertical blanking interval.
10. Supported only in the 81-ball and 72-pin package.
11. Latching edge is programmable in single-edge clocking.

The transmitter can provide video across the HDMI link in various formats. Figure 6.3 on the next page shows an overview of the processing blocks needed for some of the available format transformations from video input to HDMI output. The TMDS encoding step is not shown in this figure. See also Figure 2.1 on page 9.

The mapping tables and timing diagrams beginning on page 42 are divided into two sections. The first is for the 81-ball and 72-pin package, and begins on page 42; the second is for the 49-ball package, and begins on page 58. In these tables, the term *Swap* indicates that the Y and the Cb/Cr pin assignments are reversed, meaning the Y signals of the Swap mapping appear on the Cb/Cr signals of the standard mapping. The term Non-broken (*NB*) indicates that the signal assignments of Y, Cb, and Cr signals are contiguous. For example, signals Y0 through Y9 appear on consecutive data pins D[2:11], whereas in the standard mapping they may be broken by NC or Cb/Cr signals.

In the timing diagrams which follow, data bits labeled *val* do not convey pixel information and will contain values defined by the relevant specification. In the diagrams showing embedded sync, the SAV and EAV sequence *FF*, *00*, *00*, *XY* is specified by ITU-R BT.656.

Unused inputs should be left unconnected.

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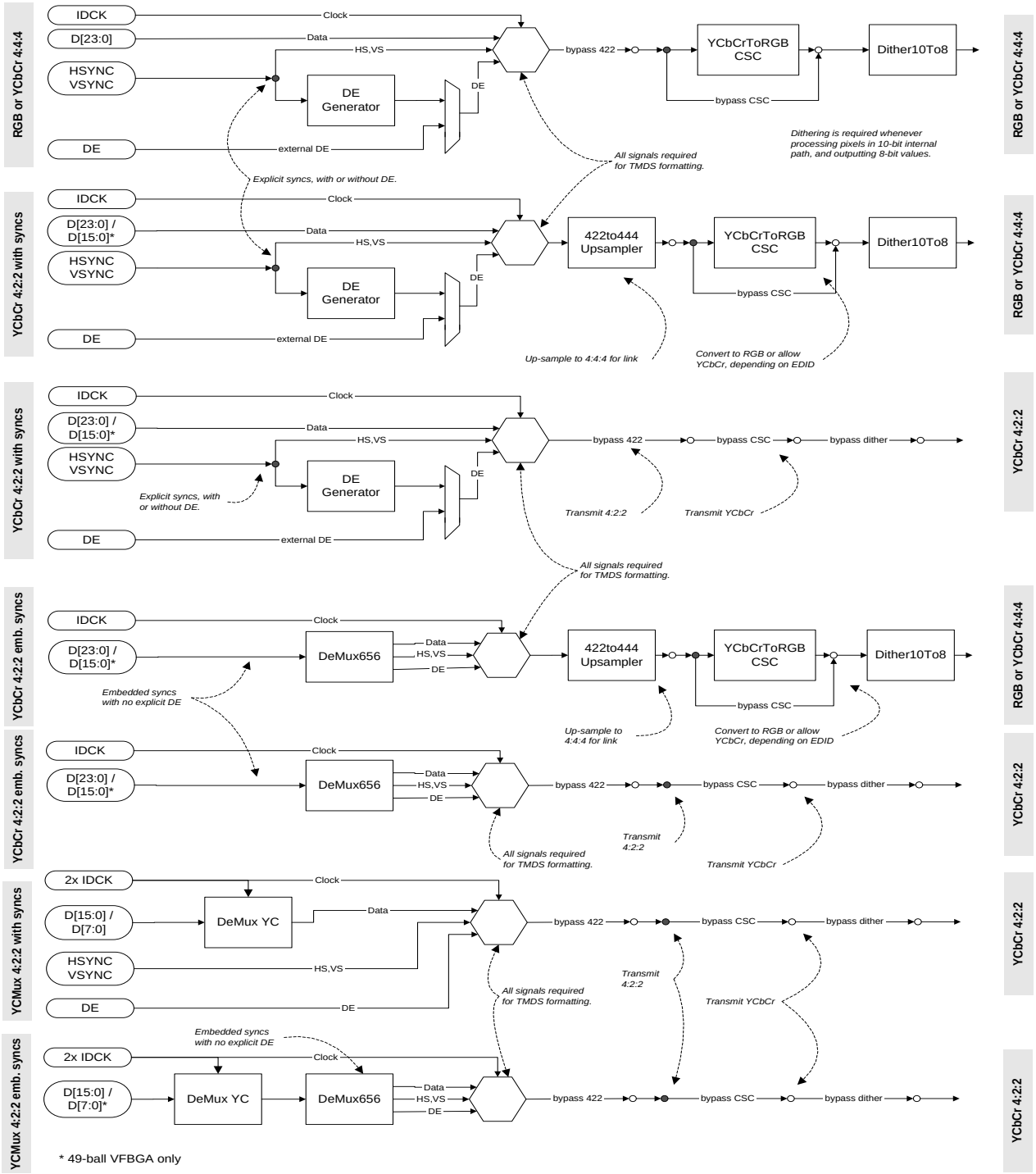

Figure 6.3. Parallel Input Video to HDMI Output Video Permutations

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6.11.1. Data Mappings for 81-ball and 72-pin Package

6.11.1.1. RGB and YCbCr 4:4:4 Separate Sync Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. Each column in Table 6.11 lists the first pixel of *n + 1* pixels in the line of video. The figure below the table shows RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}.

Table 6.11. RGB/YCbCr 4:4:4 Separate Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	24-bit Data Bus	
	RGB	YCbCr
D0	B0[0]	Cb0[0]
D1	B0[1]	Cb0[1]
D2	B0[2]	Cb0[2]
D3	B0[3]	Cb0[3]
D4	B0[4]	Cb0[4]
D5	B0[5]	Cb0[5]
D6	B0[6]	Cb0[6]
D7	B0[7]	Cb0[7]
D8	G0[0]	Y0[0]
D9	G0[1]	Y0[1]
D10	G0[2]	Y0[2]
D11	G0[3]	Y0[3]
D12	G0[4]	Y0[4]
D13	G0[5]	Y0[5]
D14	G0[6]	Y0[6]
D15	G0[7]	Y0[7]
D16	R0[0]	Cr0[0]
D17	R0[1]	Cr0[1]
D18	R0[2]	Cr0[2]
D19	R0[3]	Cr0[3]
D20	R0[4]	Cr0[4]
D21	R0[5]	Cr0[5]
D22	R0[6]	Cr0[6]
D23	R0[7]	Cr0[7]
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

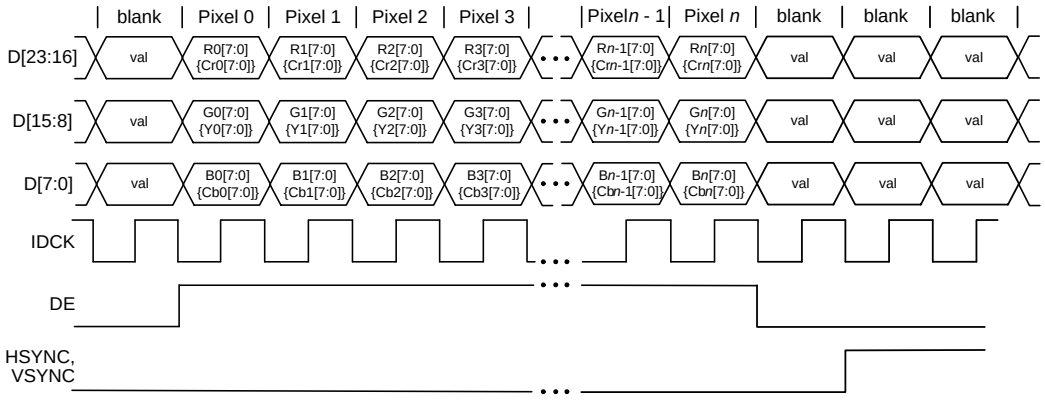

Figure 6.4. RGB/YCbCr 4:4:4 Separate Sync Timing (81-Ball and 72-Pin Package)

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6.11.1.2. YC 4:2:2 Separate Sync Formats

The YC 4:2:2 formats receive one pixel for every pixel clock period. A luma (Y) value is carried for every pixel, but the chroma values (Cb and Cr) change only every second pixel. The data bus can be 16-bit, 20-bit, or 24-bit. HSYNC and VSYNC are driven explicitly on their own pins. Each pair of columns in Table 6.12 and Table 6.13 list the first and second pixel of *n + 1* pixels in the line of video. In the figures of this section, values in braces {} show the Swap mode. The DE HIGH time must contain an even number of pixel clocks.

Table 6.12. 16-Bit and 20-Bit YC 4:2:2 Separate Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	16-bit Data Bus		16-bit Data Bus Swap		20-bit Data Bus		20-bit Data Bus NB		20-bit Data Bus Swap	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D[1:0]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D2	NC	NC	NC	NC	Y0[0]	Y1[0]	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
D3	NC	NC	NC	NC	Y0[1]	Y1[1]	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
D4	NC	NC	NC	NC	NC	NC	Y0[2]	Y1[2]	NC	NC
D5	NC	NC	NC	NC	NC	NC	Y0[3]	Y1[3]	NC	NC
D6	NC	NC	NC	NC	Cb0[0]	Cr0[0]	Y0[4]	Y1[4]	Y0[0]	Y1[0]
D7	NC	NC	NC	NC	Cb0[1]	Cr0[1]	Y0[5]	Y1[5]	Y0[1]	Y1[1]
D8	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[2]	Y1[2]	Y0[6]	Y1[6]	Cb0[2]	Cr0[2]
D9	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[3]	Y1[3]	Y0[7]	Y1[7]	Cb0[3]	Cr0[3]
D10	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[4]	Y1[4]	Y0[8]	Y1[8]	Cb0[4]	Cr0[4]
D11	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[5]	Y1[5]	Y0[9]	Y1[9]	Cb0[5]	Cr0[5]
D12	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[6]	Y1[6]	NC	NC	Cb0[6]	Cr0[6]
D13	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[7]	Y1[7]	NC	NC	Cb0[7]	Cr0[7]
D14	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[8]	Y1[8]	Cb0[0]	Cr0[0]	Cb0[8]	Cr0[8]
D15	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[9]	Y1[9]	Cb0[1]	Cr0[1]	Cb0[9]	Cr0[9]
D16	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Cb0[2]	Cr0[2]	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
D17	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Cb0[3]	Cr0[3]	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
D18	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[4]	Cr0[4]	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
D19	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[5]	Cr0[5]	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
D20	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[6]	Cr0[6]	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
D21	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[7]	Cr0[7]	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
D22	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[8]	Cr0[8]	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]
D23	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[9]	Cr0[9]	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

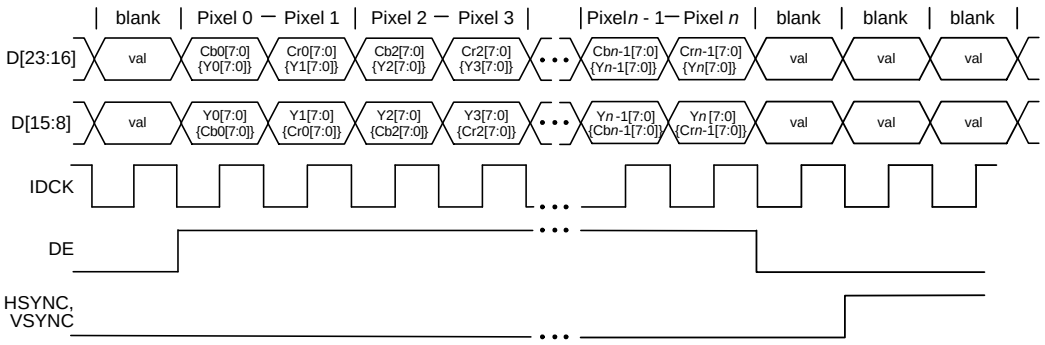

Figure 6.5. 16-Bit YC 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

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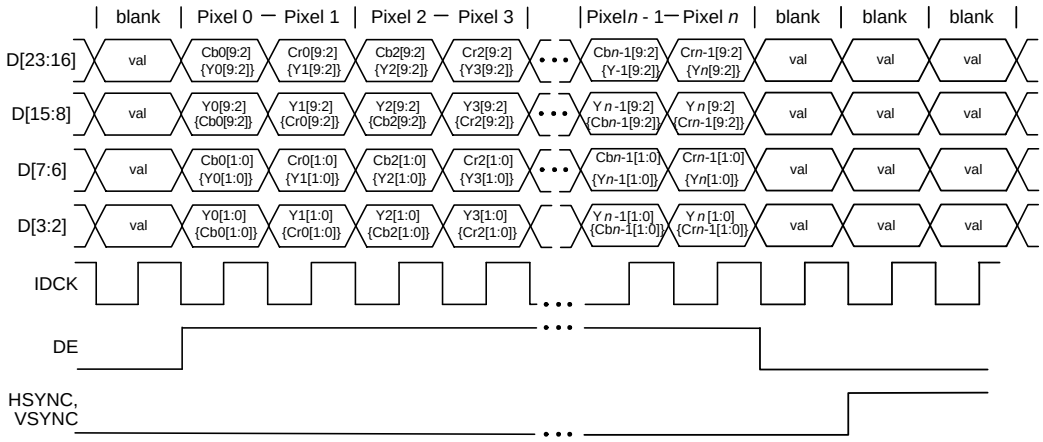

Figure 6.6. 20-Bit YC 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

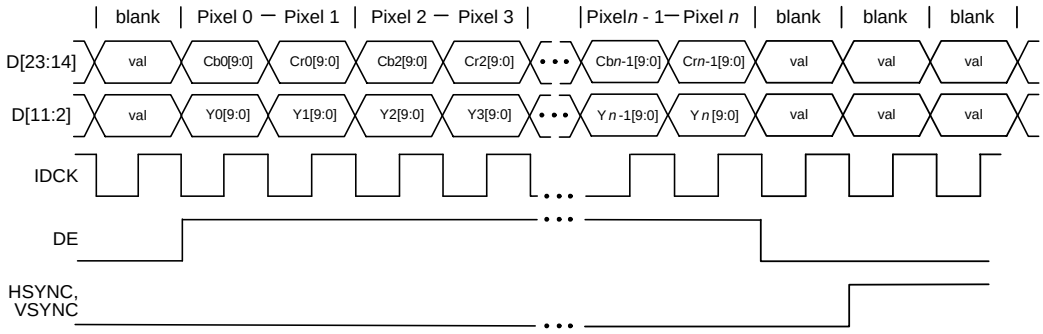

Figure 6.7. 20-Bit YC 4:2:2 Separate Sync NB Mode Timing (81-Ball and 72-Pin Package)

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Table 6.13. 24-Bit YC 4:2:2 Separate Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	24-bit Data Bus		24-bit Data Bus NB		24-bit Data Bus Swap	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D0	Y0[0]	Y1[0]	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
D1	Y0[1]	Y1[1]	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
D2	Y0[2]	Y1[2]	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
D3	Y0[3]	Y1[3]	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
D4	Cb0[0]	Cr0[0]	Y0[4]	Y1[4]	Y0[0]	Y1[0]
D5	Cb0[1]	Cr0[1]	Y0[5]	Y1[5]	Y0[1]	Y1[1]
D6	Cb0[2]	Cr0[2]	Y0[6]	Y1[6]	Y0[2]	Y1[2]
D7	Cb0[3]	Cr0[3]	Y0[7]	Y1[7]	Y0[3]	Y1[3]
D8	Y0[4]	Y1[4]	Y0[8]	Y1[8]	Cb0[4]	Cr0[4]
D9	Y0[5]	Y1[5]	Y0[9]	Y1[9]	Cb0[5]	Cr0[5]
D10	Y0[6]	Y1[6]	Y0[10]	Y1[10]	Cb0[6]	Cr0[6]
D11	Y0[7]	Y1[7]	Y0[11]	Y1[11]	Cb0[7]	Cr0[7]
D12	Y0[8]	Y1[8]	Cb0[0]	Cr0[0]	Cb0[8]	Cr0[8]
D13	Y0[9]	Y1[9]	Cb0[1]	Cr0[1]	Cb0[9]	Cr0[9]
D14	Y0[10]	Y1[10]	Cb0[2]	Cr0[2]	Cb0[10]	Cr0[10]
D15	Y0[11]	Y1[11]	Cb0[3]	Cr0[3]	Cb0[11]	Cr0[11]
D16	Cb0[4]	Cr0[4]	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
D17	Cb0[5]	Cr0[5]	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
D18	Cb0[6]	Cr0[6]	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
D19	Cb0[7]	Cr0[7]	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
D20	Cb0[8]	Cr0[8]	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]
D21	Cb0[9]	Cr0[9]	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]
D22	Cb0[10]	Cr0[10]	Cb0[10]	Cr0[10]	Y0[10]	Y1[10]
D23	Cb0[11]	Cr0[11]	Cb0[11]	Cr0[11]	Y0[11]	Y1[11]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

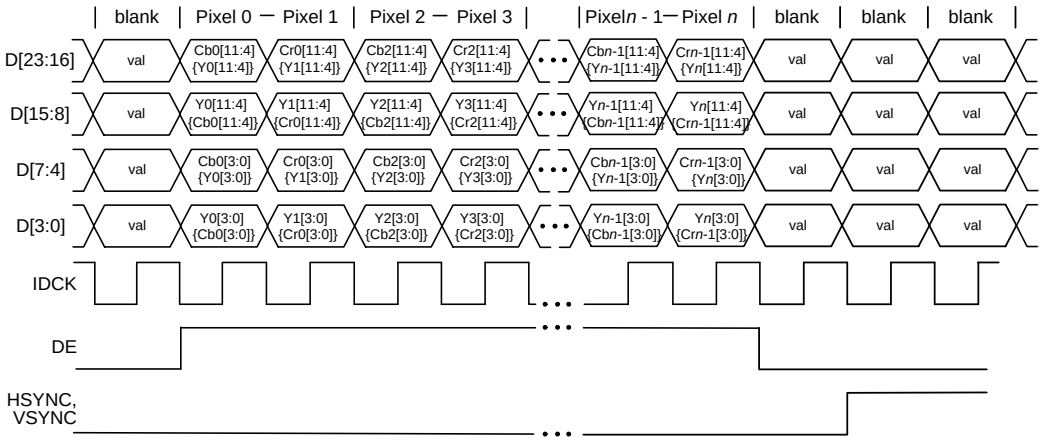

Figure 6.8. 24-Bit YC 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

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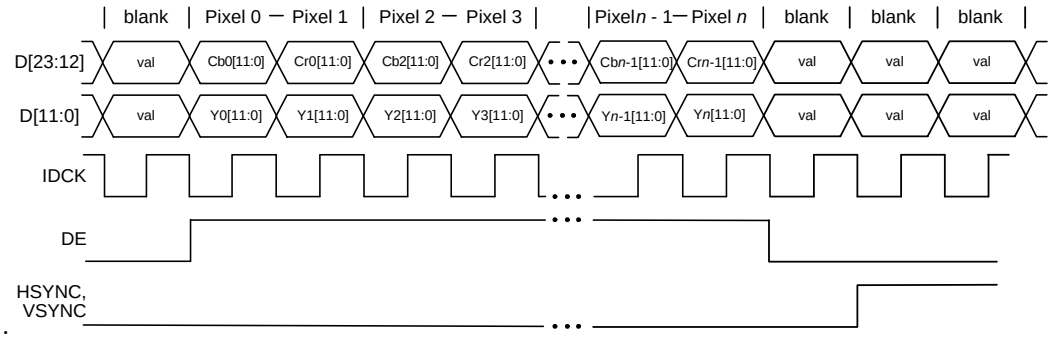

Figure 6.9. 24-Bit YC 4:2:2 Separate Sync NB Mode Timing (81-Ball and 72-Pin Package)

6.11.1.3. YC 4:2:2 Embedded Sync Formats

The Embedded Sync format is identical to the YC 4:2:2 Formats with Separate Syncs format, except that the syncs are embedded and not explicit. The data bus can be 16-bit, 20-bit, or 24-bit. Each pair of columns in Table 6.14 and Table 6.15 list the first and second pixel of *n + 1* pixels in the line of video. In the figures of this section, values in braces {} show the Swap mode.

Table 6.14. 16-Bit and 20-Bit YC 4:2:2 Embedded Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	16-bit Data Bus		16-bit Data Bus Swap		20-bit Data Bus		20-bit Data Bus Swap		20-bit Data Bus NB	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D[1:0]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D2	NC	NC	NC	NC	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
D3	NC	NC	NC	NC	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
D4	NC	NC	NC	NC	NC	NC	NC	NC	Y0[2]	Y1[2]
D5	NC	NC	NC	NC	NC	NC	NC	NC	Y0[3]	Y1[3]
D6	NC	NC	NC	NC	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Y0[4]	Y1[4]
D7	NC	NC	NC	NC	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Y0[5]	Y1[5]
D8	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[6]	Y1[6]
D9	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[7]	Y1[7]
D10	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[8]	Y1[8]
D11	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[9]	Y1[9]
D12	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	NC	NC
D13	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	NC	NC
D14	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]	Cb0[0]	Cr0[0]
D15	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]	Cb0[1]	Cr0[1]
D16	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
D17	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
D18	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
D19	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
D20	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
D21	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
D22	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]
D23	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]
HSYNC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
VSYNC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
DE	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

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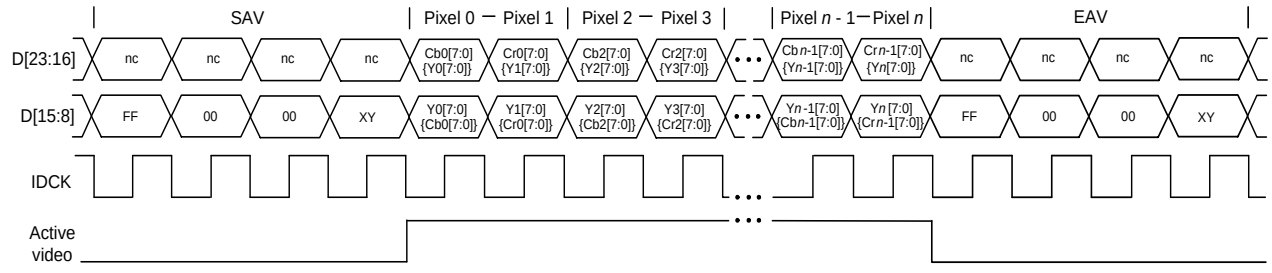

Figure 6.10. 16-Bit YC 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

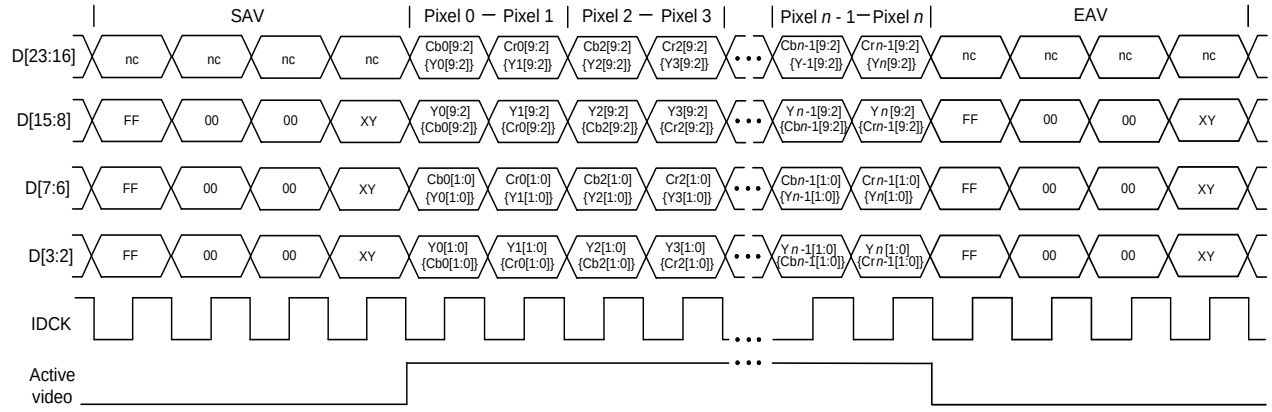

Figure 6.11. 20-Bit YC 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

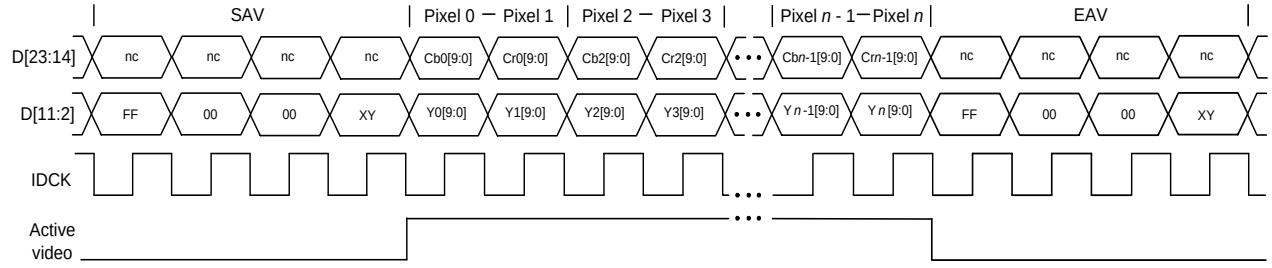

Figure 6.12. 20-Bit YC 4:2:2 Embedded Sync NB Mode Timing (81-Ball and 72-Pin Package)

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Table 6.15. 24-Bit YC 4:2:2 Embedded Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	24-bitData Bus		24-bitData Bus Swap		24-bitData Bus NB	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
D4	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Y0[4]	Y1[4]
D5	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Y0[5]	Y1[5]
D6	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Y0[6]	Y1[6]
D7	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Y0[7]	Y1[7]
D8	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[8]	Y1[8]
D9	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[9]	Y1[9]
D10	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[10]	Y1[10]
D11	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[11]	Y1[11]
D12	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]	Cb0[0]	Cr0[0]
D13	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]	Cb0[1]	Cr0[1]
D14	Y0[10]	Y1[10]	Cb0[10]	Cr0[10]	Cb0[2]	Cr0[2]
D15	Y0[11]	Y1[11]	Cb0[11]	Cr0[11]	Cb0[3]	Cr0[3]
D16	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
D17	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
D18	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
D19	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
D20	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]
D21	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]
D22	Cb0[10]	Cr0[10]	Y0[10]	Y1[10]	Cb0[10]	Cr0[10]
D23	Cb0[11]	Cr0[11]	Y0[11]	Y1[11]	Cb0[11]	Cr0[11]
HSYNC	NC	NC	NC	NC	NC	NC
VSYNC	NC	NC	NC	NC	NC	NC
DE	NC	NC	NC	NC	NC	NC

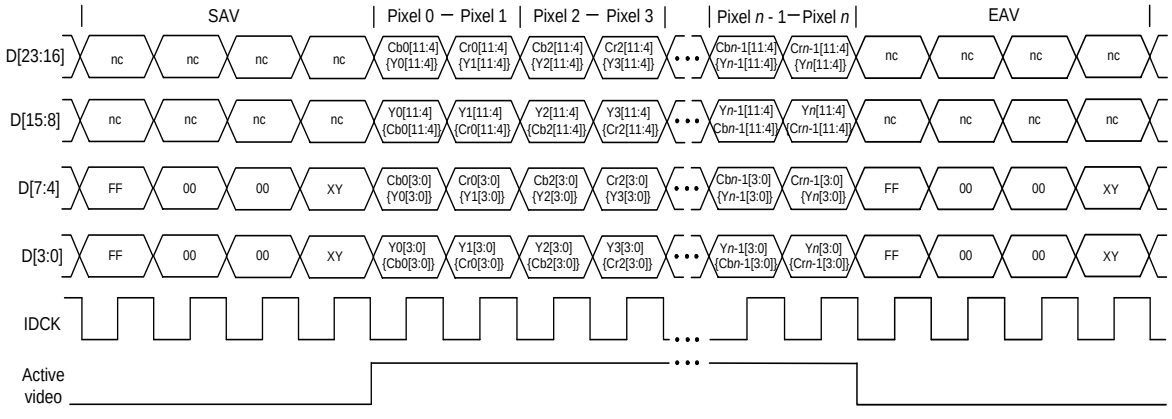

Figure 6.13. 24-Bit YC 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

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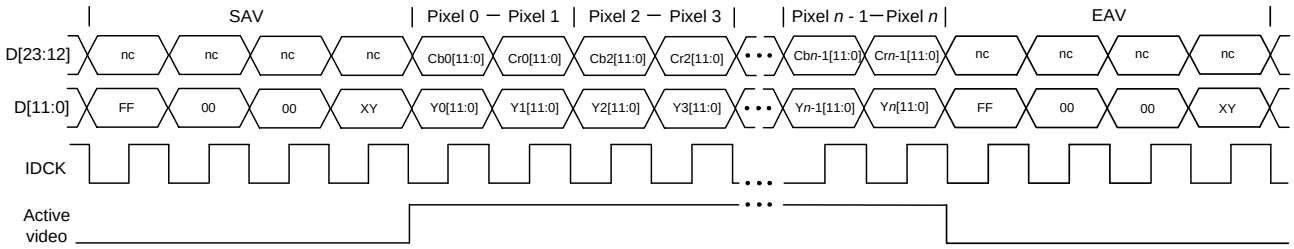

Figure 6.14. 24-Bit YC 4:2:2 Embedded Sync NB Mode Timing (81-Ball and 72-Pin Package)

6.11.1.4. YC Mux 4:2:2 Separate Sync Formats

The video data is multiplexed onto fewer pins than the mapping described in the YC 4:2:2 Separate Sync Formats on page 43. The clock rate is doubled so a chroma value is sent for each pixel, followed by a corresponding luma value for the same pixel. Thus, a luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. Each group of four columns in Table 6.16 lists the four clock cycles for the first two pixels of the line. Pixel values for Cr0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cb0 and Y1 values are sent with the second pixel (next two clock cycles). The figures below the table show how this pattern is extended for the rest of the pixels in a video line of *n + 1* pixels.

Table 6.16. 8-, 10-, and 12-Bit YC Mux 4:2:2 Separate Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	8-bit Data Bus				10-bit Data Bus				12-bit Data Bus			
	Clock cycle				Clock cycle				Clock cycle			
	First	Second	Third	Fourth	First	Second	Third	Fourth	First	Second	Third	Fourth
D0	NC				NC				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	NC				NC				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	NC				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	NC				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D[7:4]	NC				NC				NC			
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D14	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D[23:16]	NC				NC				NC			
HSYNC	HSYNC				HSYNC				HSYNC			
VSYNC	VSYNC				VSYNC				VSYNC			
DE	DE				DE				DE			

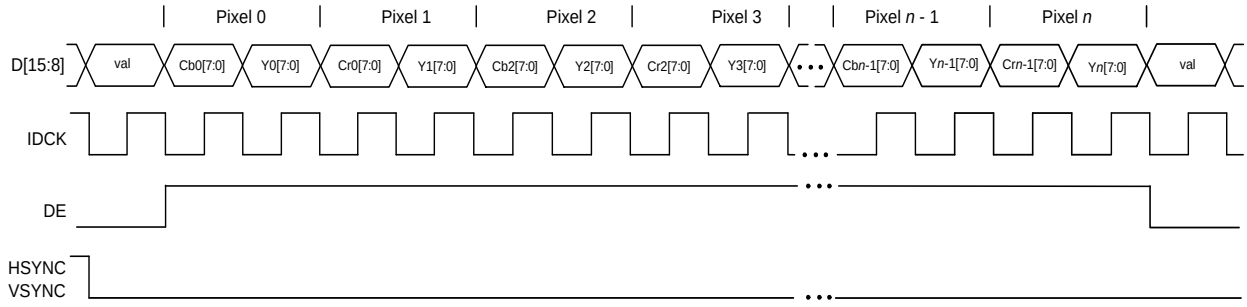

Figure 6.15. 8-Bit YC Mux 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

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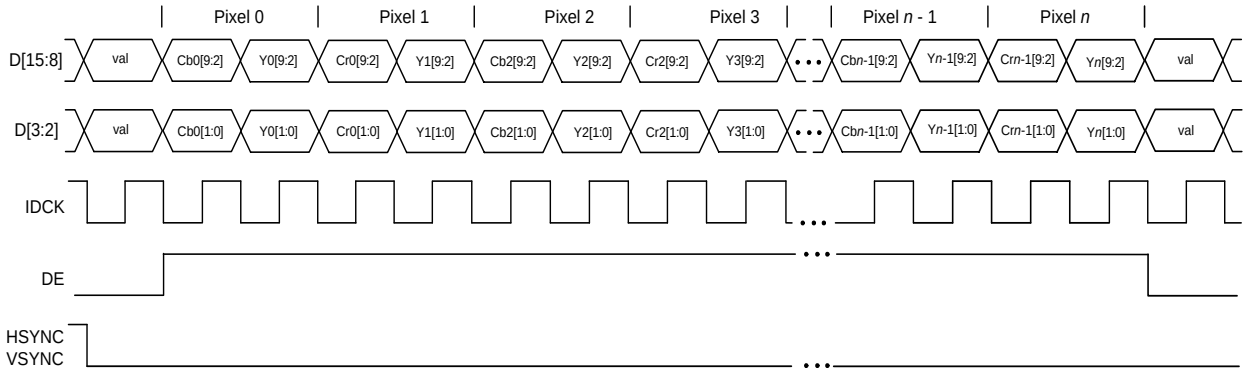

Figure 6.16. 10-Bit YC Mux 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

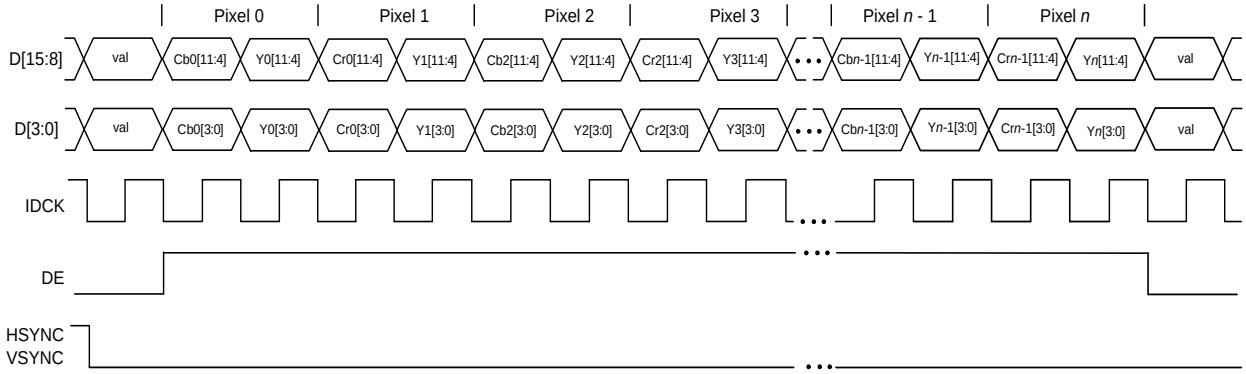

Figure 6.17. 12-Bit YC Mux 4:2:2 Separate Sync Timing (81-Ball and 72-Pin Package)

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6.11.1.5. YC Mux 4:2:2 Embedded Sync Formats

This format is similar to the one described in the YC Mux 4:2:2 Separate Sync Formats section on page 49, except the syncs are embedded. Normally this mode is used only for 480i, 480p, 576i and 576p modes. It is similar to SMTPE 293 in embedding the syncs. A luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. The input clock rate is twice the pixel clock rate. Each group of four columns in Table 6.17 lists the four clock cycles for the first two pixels of the line. Pixel values for Cr0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cb0 and Y1 values are sent with the second pixel (next two clock cycles). The figures following this table show only the first two pixels and last pixel of the line to make room to show the SAV and EAV sequences, but the remaining pixels are similar to those shown in the figures of the previous section. 480p, 54 MHz input can be achieved if the input clock is 54 MHz. The DE generator may be needed to convert extracted sync timings to CEA-861D timings. See the ITU-R BT.656 Specification.

Table 6.17. 8-, 10-, and 12-Bit YC Mux 4:2:2 Embedded Sync Data Mapping (81-Ball and 72-Pin Package)

Pin Name	8-bit Data Bus				10-bit Data Bus				12-bit Data Bus			
	Clock cycle				Clock cycle				Clock cycle			
	First	Second	Third	Fourth	First	Second	Third	Fourth	First	Second	Third	Fourth
D0	NC				NC				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	NC				NC				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	NC				Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	NC				Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D[7:4]	NC				NC				NC			
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D14	Cb0[6]	Y0[6]	Cr0[6]]	Y1[6]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D[23:16]	NC				NC				NC			
HSYNC	NC				NC				NC			
VSYNC	NC				NC				NC			
DE	NC				NC				NC			

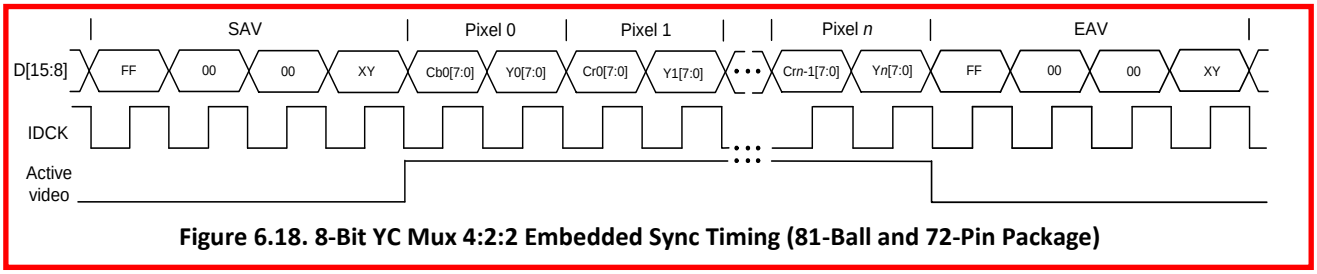

Figure 6.18. 8-Bit YC Mux 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

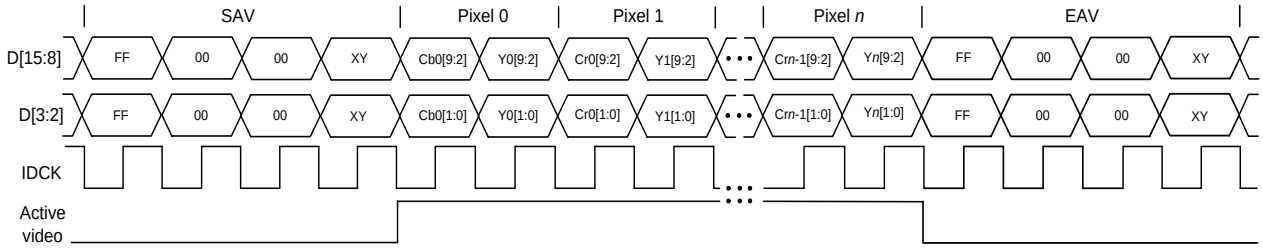

Figure 6.19. 10-Bit YC Mux 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

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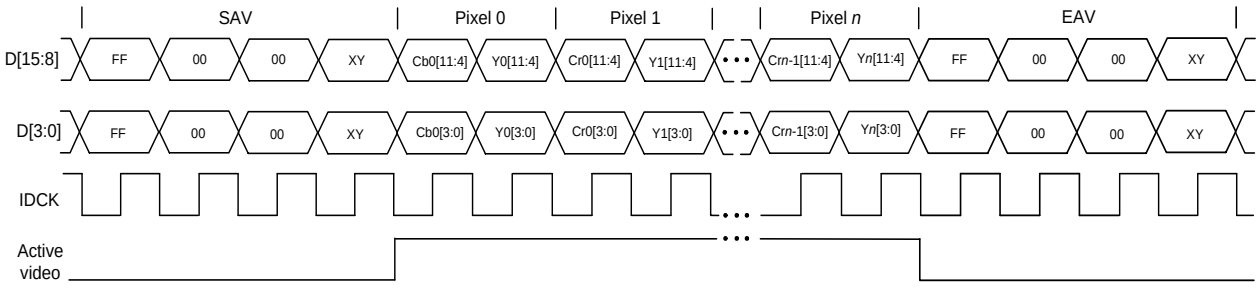

Figure 6.20. 12-Bit YC Mux 4:2:2 Embedded Sync Timing (81-Ball and 72-Pin Package)

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6.11.1.6. YC 4:2:2 Embedded Sync Dual Edge Format

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock. One clock edge latches in half the pixel data on 12 pins. The opposite clock edge latches in the remaining half of the pixel data on the same 12 pins. Data signals (D*x*]) must change state to meet the setup and hold times, specified for the 12-bit dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit. See Table 3.12 on page 18 or Table 3.13 on page 19. The syncs are embedded and not explicit. Figure 6.21 lists IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge).

Table 6.18. 12-Bit YC 4:2:2 Embedded Sync Dual Edge Data Mapping (81-Ball and 72-Pin Package)

Pin Name	12-bit Data Bus			
	Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge
D0	Y0[0]	Y0[8]	Y1[0]	Y1[8]
D1	Y0[1]	Y0[9]	Y1[1]	Y1[9]
D2	Y0[2]	Y0[10]	Y1[2]	Y1[10]
D3	Y0[3]	Y0[11]	Y13]	Y1[11]
D4	Cb0[0]	Cb0[4]	Cr0[0]	Cr0[4]
D5	Cb0[1]	Cb0[5]	Cr0[1]	Cr0[5]
D6	Cb0[2]	Cb0[6]	Cr0[2]	Cr0[6]
D7	Cb0[3]	Cb0[7]	Cr0[3]	Cr0[7]
D8	Y0[4]	Cb0[8]	Y1[4]	Cr0[8]
D9	Y0[5]	Cb0[9]	Y1[5]	Cr0[9]
D10	Y0[6]	Cb0[10]	Y1[6]	Cr0[10]
D11	Y0[7]	Cb0[11]	Y1[7]	Cr0[11]
D[23:12]	NC	NC	NC	NC
HSYNC	NC	—	NC	—
VSYNC	NC	—	NC	—
DE	NC	—	NC	—

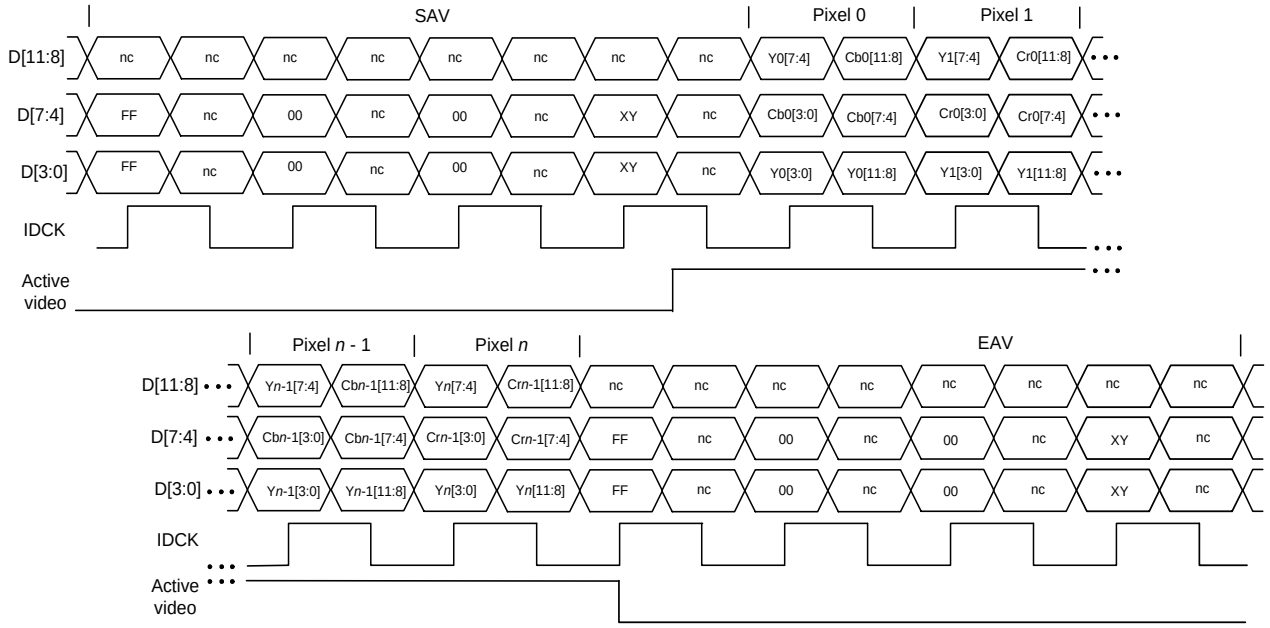

Figure 6.21. 12-Bit YC 4:2:2 Embedded Sync Dual Edge Timing (81-Ball and 72-Pin Package)

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6.11.1.7. RGB and YCbCr 4:4:4 Dual Edge Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. The same timing format is used for RGB and YCbCr 4:4:4. Each pair of columns in Table 6.19 lists the first pixel of *n + 1* pixels in the line of video. The figures below the table show RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit (see the Programmer's Reference). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge). See Table 3.12 on page 18 or Table 3.13 on page 19 for the required timing relationships.

Table 6.19. 12-Bit RGB/YCbCr 4:4:4 Separate Sync Dual Edge Data Mapping (81-Ball and 72-Pin Package)

Pin Name	12-bit Data Bus			
	RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge
D0	B0[0]	G0[4]	Cb0[0]	Y0[4]
D1	B0[1]	G0[5]	Cb0[1]	Y0[5]
D2	B0[2]	G0[6]	Cb0[2]	Y0[6]
D3	B0[3]	G0[7]	Cb0[3]	Y0[7]
D4	B0[4]	R0[0]	Cb0[4]	Cr0[0]
D5	B0[5]	R0[1]	Cb0[5]	Cr0[1]
D6	B0[6]	R0[2]	Cb0[6]	Cr0[2]
D7	B0[7]	R0[3]	Cb0[7]	Cr0[3]
D8	G0[0]	R0[4]	Y0[0]	Cr0[4]
D9	G0[1]	R0[5]	Y0[1]	Cr0[5]
D10	G0[2]	R0[6]	Y0[2]	Cr0[6]
D11	G0[3]	R0[7]	Y0[3]	Cr0[7]
D[23:12]	NC	NC	NC	NC
HSYNC	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—
DE	DE	—	DE	—

Note: Unused inputs should be left not connected.

Figure 6.22 shows IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge).

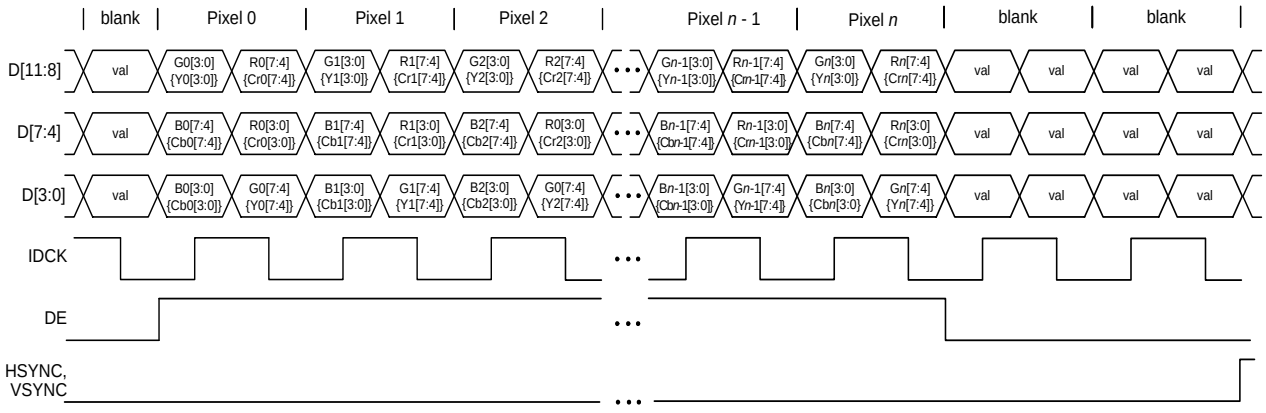

Figure 6.22. 12-Bit RGB 4:4:4 Separate Sync Dual Edge Timing (81-Ball and 72-Pin Package)

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6.11.1.8. YC 4:2:2 Separate Sync Dual Edge Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. Each group of 4 columns in the tables of this section lists the first two pixels of *n + 1* pixels in the line of video. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit (see the Programmer's Reference). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge). See Table 3.12 on page 18 or Table 3.13 on page 19 for the required timing relationships. Pixel values within braces {} in the figures show the values in Swap mode.

Table 6.20. 8-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (81-Ball and 72-Pin Package)

Pin Name	8-bit Data Bus				8-bit Data Bus Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D[3:0]	NC	NC	NC	NC	NC	NC	NC	NC
D4	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D7	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D8	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D11	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D[23:12]	NC	NC	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—

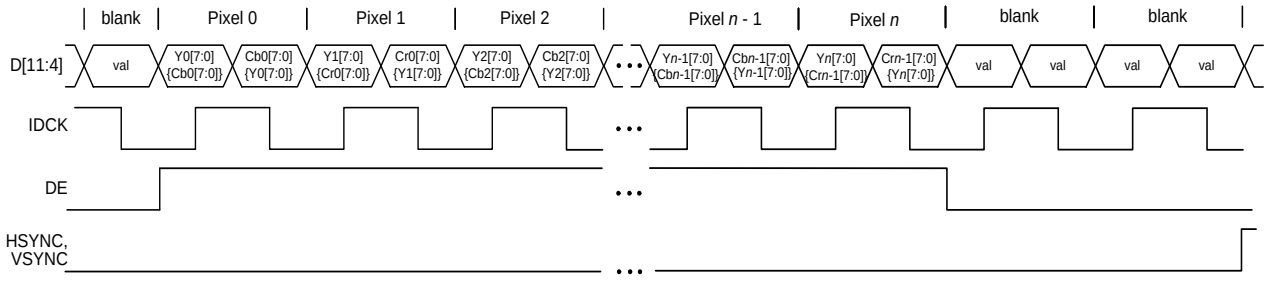

Figure 6.23. 8-Bit YC 4:2:2 Separate Sync Dual Edge Timing (81-b all and 72-p in Package)

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Table 6.21. 10-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (81-Ball and 72-Pin Package)

Pin Name	10-bit Data Bus				10-bit Data Bus Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D[1:0]	NC	NC	NC	NC	NC	NC	NC	NC
D2	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D3	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D4	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D5	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D6	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D7	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D8	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D9	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D10	Y0[8]	Cb0[8]	Y1[8]	Cr0[8]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D11	Y0[9]	Cb0[9]	Y1[9]	Cr0[9]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D[23:12]	NC	NC	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—

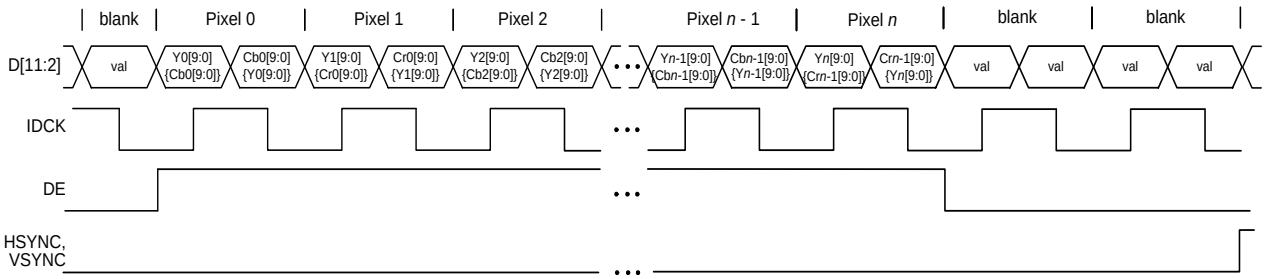

Figure 6.24. 10-Bit YC 4:2:2 Separate Sync Dual Edge Timing (81-Ball and 72-Pin Package)

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Table 6.22. 12-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (81-Ball and 72-Pin Package)

Pin Name	12-bit Data Bus				12-bit Data Bus NB				12-bit Data Bus NB Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D0	Y0[0]	Y0[8]	Y1[0]	Y1[8]	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	Y0[1]	Y0[9]	Y1[1]	Y1[9]	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	Y0[2]	Y0[10]	Y1[2]	Y1[10]	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	Y0[3]	Y0[11]	Y1[3]	Y1[11]	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	Cb0[0]	Cb0[4]	Cr0[0]	Cr0[4]	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	Cb0[1]	Cb0[5]	Cr0[1]	Cr0[5]	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	Cb0[2]	Cb0[6]	Cr0[2]	Cr0[6]	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	Cb0[3]	Cb0[7]	Cr0[3]	Cr0[7]	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D8	Y0[4]	Cb0[8]	Y1[4]	Cr0[8]	Y0[8]	Cb0[8]	Y1[8]	Cr0[8]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D9	Y0[5]	Cb0[9]	Y1[5]	Cr0[9]	Y0[9]	Cb0[9]	Y1[9]	Cr0[9]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D10	Y0[6]	Cb0[10]	Y1[6]	Cr0[10]	Y0[10]	Cb0[10]	Y1[10]	Cr0[10]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D11	Y0[7]	Cb0[11]	Y1[7]	Cr0[11]	Y0[11]	Cb0[11]	Y1[11]	Cr0[11]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D[23:12]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—	DE	—	DE	—

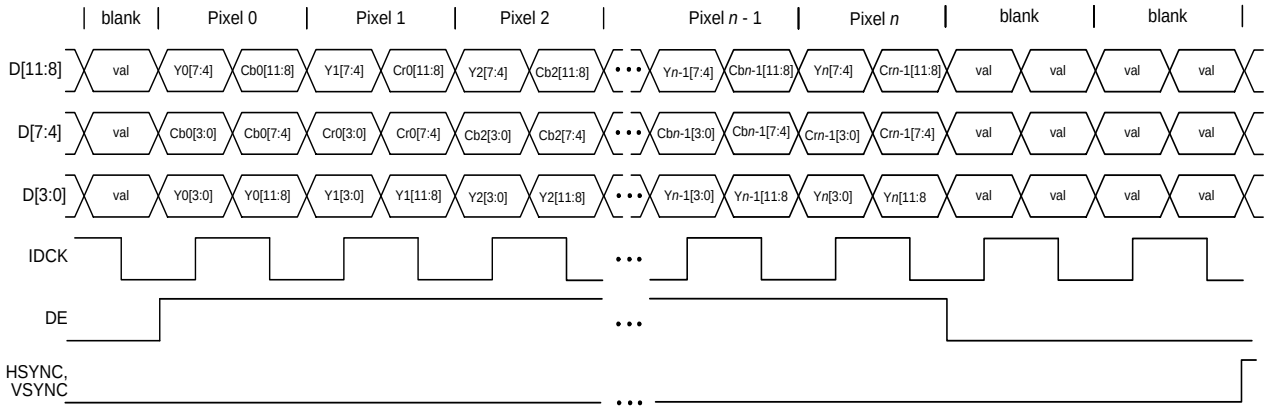

Figure 6.25. 12-Bit YC 4:2:2 Separate Sync Dual Edge Timing (81-Ball and 72-Pin Package)

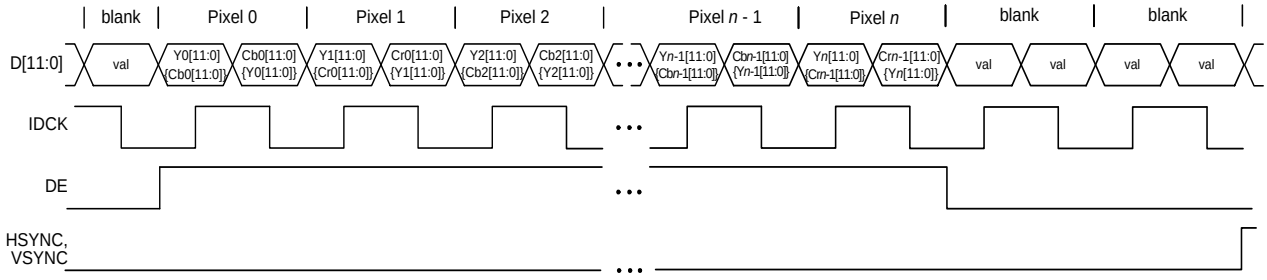

Figure 6.26. 12-Bit YC 4:2:2 Separate Sync NB Mode Dual Edge Timing (81-Ball and 72-Pin Package)

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6.11.2. Data Mappings for 49-Ball Package

6.11.2.1. YC 4:2:2 Separate Sync Formats

The YC 4:2:2 format receives one pixel for every pixel clock period. A luma (Y) value is carried for every pixel, but the chroma values (Cb and Cr) change only every second pixel. The data bus can only be 16-bits. HSYNC and VSYNC are driven explicitly on their own pins. Each pair of columns in Table 6.23 lists the first and second pixel of *n + 1* pixels in the line of video. Pixel values within braces {} in the figures show the values in Swap mode. The DE HIGH time must contain an even number of pixel clocks.

Table 6.23. 16-Bit YC 4:2:2 Separate Sync Data Mapping (49-Ball Package)

Pin Name	16-bit Data Bus		16-bit Data Bus Swap	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE

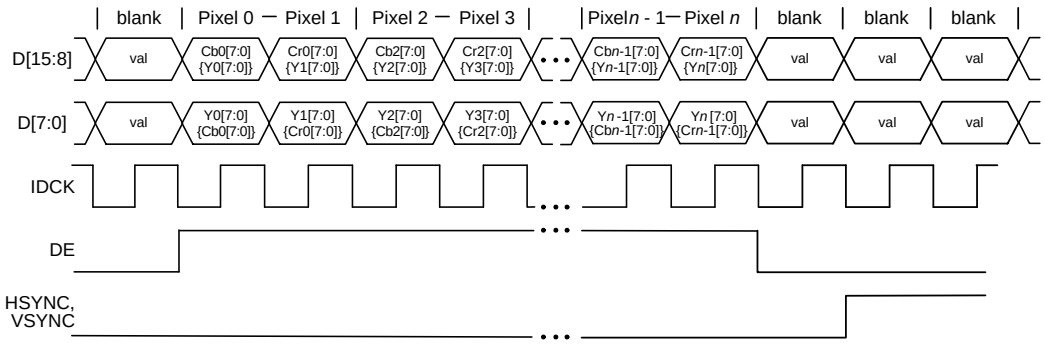

Figure 6.27. 16-bit YC 4:2:2 Separate Sync Timing (49-Ball Package)

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6.11.2.2. YC 4:2:2 Embedded Sync Format

The Embedded Sync format is identical to the YC 4:2:2 Format with Separate Syncs, except that the syncs are embedded and not explicit. The data bus can be 16-bit, 20-bit, or 24-bit. Each pair of columns in Table 6.24 lists the first and second pixel of *n + 1* pixels in the line of video.

Table 6.24. 16-Bit YC 4:2:2 Embedded Sync Data Mapping (49-Ball Package)

Pin Name	16-bit Data Bus	
	Pixel #0	Pixel #1
D0	Y0[0]	Y1[0]
D1	Y0[1]	Y1[1]
D2	Y0[2]	Y1[2]
D3	Y0[3]	Y1[3]
D4	Y0[4]	Y1[4]
D5	Y0[5]	Y1[5]
D6	Y0[6]	Y1[6]
D7	Y0[7]	Y1[7]
D8	Cb0[0]	Cr0[0]
D9	Cb0[1]	Cr0[1]
D10	Cb0[2]	Cr0[2]
D11	Cb0[3]	Cr0[3]
D12	Cb0[4]	Cr0[4]
D13	Cb0[5]	Cr0[5]
D14	Cb0[6]	Cr0[6]
D15	Cb0[7]	Cr0[7]
HSYNC	NC	NC
VSYNC	NC	NC
DE	NC	NC

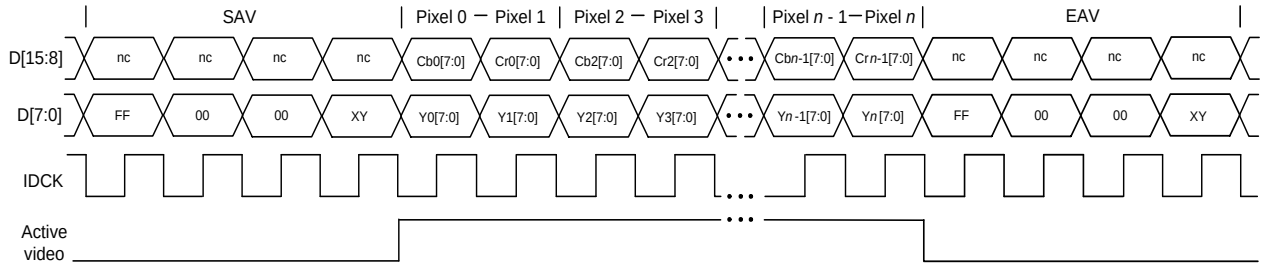

Figure 6.28. 16-Bit YC 4:2:2 Embedded Sync Timing (49-Ball Package)

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6.11.2.3. YC Mux 4:2:2 Separate Sync Format

The video data is multiplexed onto fewer pins than the mapping described in the YC 4:2:2 Separate Sync Formats on page 58. The clock rate is doubled so a chroma value is sent for each pixel, followed by a corresponding luma value for the same pixel. Thus, a luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. Each group of four columns in Table 6.25 lists the four clock cycles for the first two pixels of the line. Pixel values for Cr0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cb0 and Y1 values are sent with the second pixel (next two clock cycles). The figure below the table shows how this pattern is extended for the rest of the pixels in a video line of *n + 1* pixels.

Table 6.25. 8-Bit YC Mux 4:2:2 Separate Sync Data Mapping (49-Ball Package)

Pin Name	8-bit Data Bus			
	Clock cycle			
	First	Second	Third	Fourth
D0	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D[15:8]	NC			
HSYNC	HSYNC			
VSYNC	VSYNC			
DE	DE			

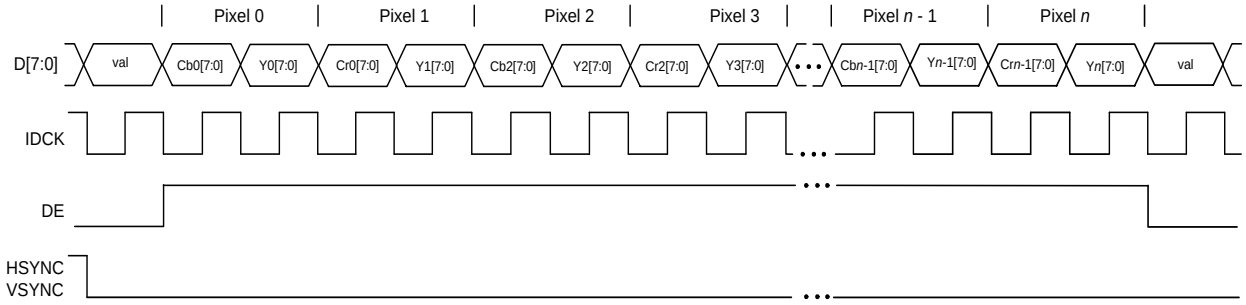

Figure 6.29. 8-Bit YC Mux 4:2:2 Separate Sync Timing (49-Ball Package)

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6.11.2.4. YC Mux 4:2:2 Embedded Sync Format

This format is similar to the one described in the YC Mux 4:2:2 Separate Sync Format section on page 60, except the syncs are embedded. Normally this mode is used only for 480i, 480p, 576i and 576p modes. It is similar to SMTPE 293 in embedding the syncs. A luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. The input clock rate is twice the pixel clock rate. Each group of four columns in Table 6.17 lists the four clock cycles for the first two pixels of the line. Pixel values for Cr0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cb0 and Y1 values are sent with the second pixel (next two clock cycles). The figure following this table shows only the first two pixels and last pixel of the line to make room to show the SAV and EAV sequences, but the remaining pixels are similar to those shown in the figure of the previous section. 480p, 54 MHz input can be achieved if the input clock is 54 MHz. The DE generator may be needed to convert extracted sync timings to CEA-861D timings. See the ITU-R BT.656 Specification.

Table 6.26. 8-Bit YC Mux 4:2:2 Embedded Sync Data Mapping (49-Ball Package)

Pin Name	8-bit Data Bus			
	Clock cycle			
	First	Second	Third	Fourth
D0	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D[15:8]	NC			
HSYNC	NC			
VSYNC	NC			
DE	NC			

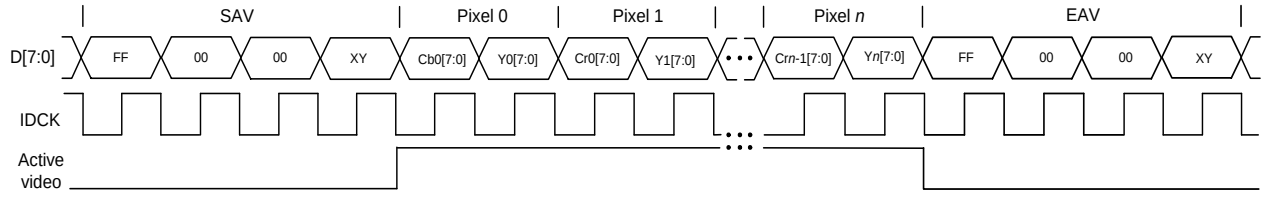

Figure 6.30. 8-Bit YC Mux 4:2:2 Embedded Sync Timing (49-Ball Package)

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6.11.2.5. YC 4:2:2 Embedded Sync Dual Edge Format

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock. One clock edge latches in half the pixel data on 12 pins. The opposite clock edge latches in the remaining half of the pixel data on the same 12 pins. Data signals (D*x*) must change state to meet the setup and hold times, specified for the 12-bit dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit. See Table 3.12 on page 18. The syncs are embedded and not explicit. Figure 6.31 shows IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge).

Table 6.27. 12-Bit YC 4:2:2 Embedded Sync Dual Edge Data Mapping (49-Ball Package)

Pin Name	12-bit Data Bus			
	Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge
D[3:0]	NC	NC	NC	NC
D4	Y0[0]	Y0[8]	Y1[0]	Y1[8]
D5	Y0[1]	Y0[9]	Y1[1]	Y1[9]
D6	Y0[2]	Y0[10]	Y1[2]	Y1[10]
D7	Y0[3]	Y0[11]	Y1[3]	Y1[11]
D8	Cb0[0]	Cb0[4]	Cr0[0]	Cr0[4]
D9	Cb0[1]	Cb0[5]	Cr0[1]	Cr0[5]
D10	Cb0[2]	Cb0[6]	Cr0[2]	Cr0[6]
D11	Cb0[3]	Cb0[7]	Cr0[3]	Cr0[7]
D12	Y0[4]	Cb0[8]	Y1[4]	Cr0[8]
D13	Y0[5]	Cb0[9]	Y1[5]	Cr0[9]
D14	Y0[6]	Cb0[10]	Y1[6]	Cr0[10]
D15	Y0[7]	Cb0[11]	Y1[7]	Cr0[11]
HSYNC	NC	—	NC	—
VSYNC	NC	—	NC	—
DE	NC	—	NC	—

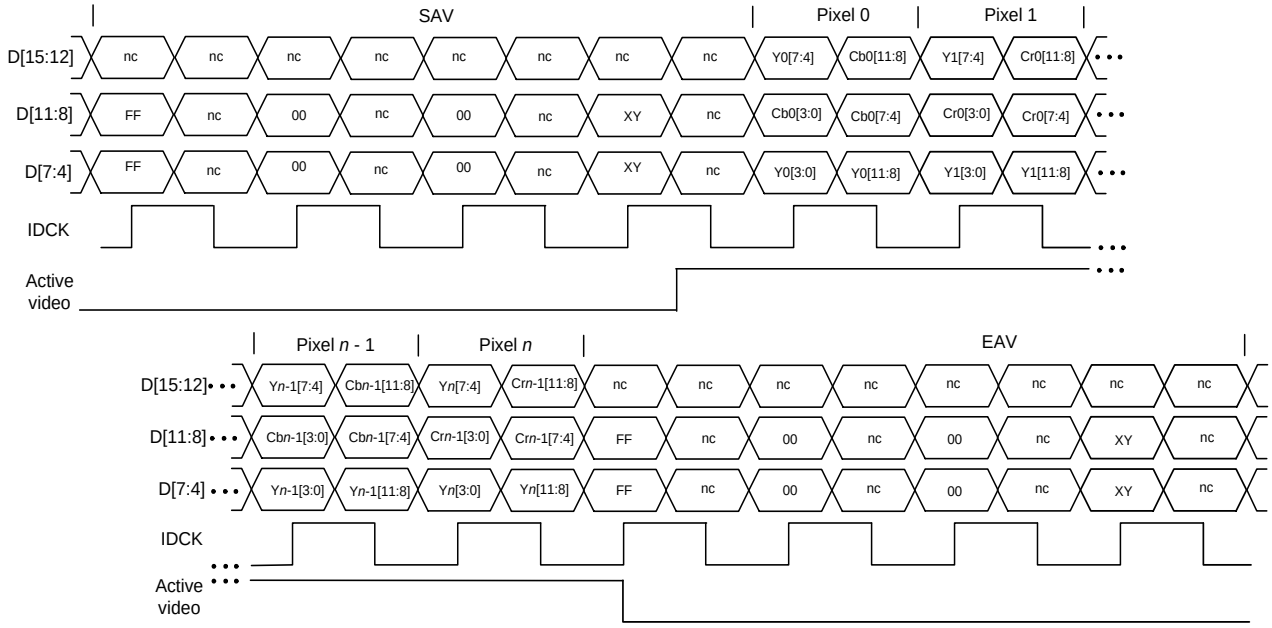

Figure 6.31. 12-Bit YC 4:2:2 Embedded Sync Timing (49-Ball Package)

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6.11.2.6. RGB and YCbCr 4:4:4 Dual Edge Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. The same timing format is used for RGB and YCbCr 4:4:4. Each pair of columns in Table 6.28 lists the first pixel of *n + 1* pixels in the line of video. The figures below the table show RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit (see the Programmer's Reference). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge). See Table 3.12 on page 18 for the required timing relationships.

Table 6.28. 12-Bit RGB/YCbCr 4:4:4 Separate Sync Dual Edge Data Mapping (49-Ball Package)

Pin Name	12-bit Data Bus			
	RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge
D[3-0]	NC	NC	NC	NC
D4	B0[0]	G0[4]	Cb0[0]	Y0[4]
D5	B0[1]	G0[5]	Cb0[1]	Y0[5]
D6	B0[2]	G0[6]	Cb0[2]	Y0[6]
D7	B0[3]	G0[7]	Cb0[3]	Y0[7]
D8	B0[4]	R0[0]	Cb0[4]	Cr0[0]
D9	B0[5]	R0[1]	Cb0[5]	Cr0[1]
D10	B0[6]	R0[2]	Cb0[6]	Cr0[2]
D11	B0[7]	R0[3]	Cb0[7]	Cr0[3]
D12	G0[0]	R0[4]	Y0[0]	Cr0[4]
D13	G0[1]	R0[5]	Y0[1]	Cr0[5]
D14	G0[2]	R0[6]	Y0[2]	Cr0[6]
D15	G0[3]	R0[7]	Y0[3]	Cr0[7]
HSYNC	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—
DE	DE	—	DE	—

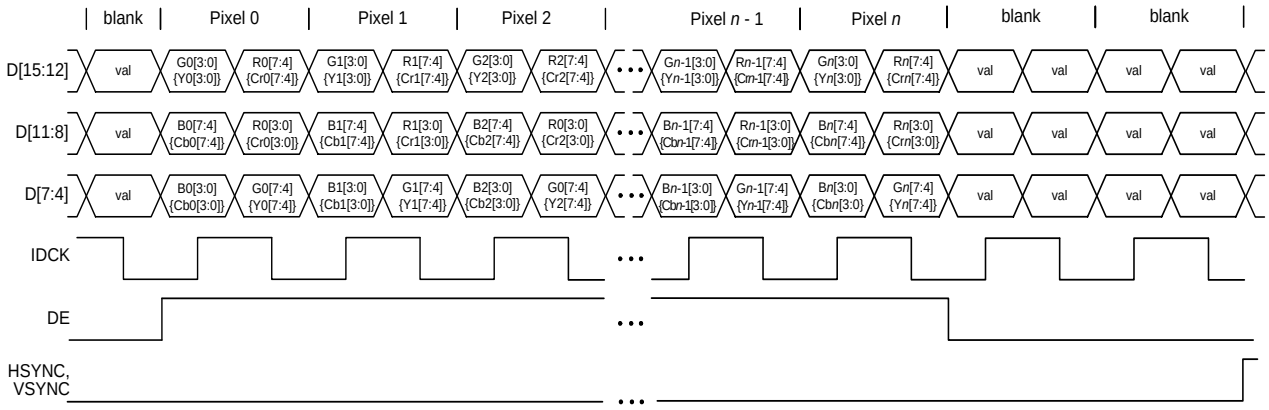

Figure 6.32. 12-Bit RGB/YCbCr 4:4:4 Separate Sync Timing (49-Ball Package)

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6.11.2.7. YC 4:2:2 Separate Sync Dual Edge Formats

The pixel clock runs at the pixel rate and a complete definition of each pixel is received on each clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. Each group of 4 columns in the tables of this section lists the first two pixels of *n + 1* pixels in the line of video. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit (see the Programmer's Reference). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge). See Table 3.12 on page 18 for the required timing relationships. Pixel values within braces {} in the figures show the values in Swap mode.

Table 6.29. 8-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (49-Ball Package)

Pin Name	8-bit Data Bus				8-bit Data Bus Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D[7:0]	NC	NC	NC	NC	NC	NC	NC	NC
D8	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D9	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D10	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D11	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D12	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D13	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D14	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D15	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—

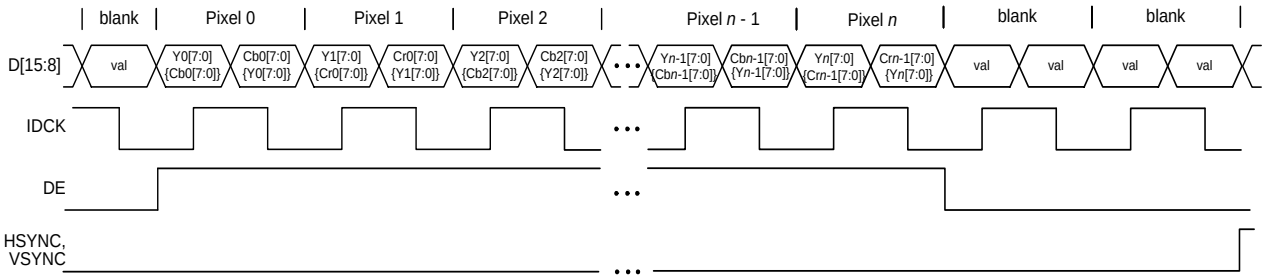

Figure 6.33. 8-Bit YC 4:2:2 Separate Sync Dual Edge Timing (49-Ball Package)

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Table 6.30. 10-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (49-Ball Package)

Pin Name	10-bit Data Bus				10-bit Data Bus Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D[5:0]	NC	NC	NC	NC	NC	NC	NC	NC
D6	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D7	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D8	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D9	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D10	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D11	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D12	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D13	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D14	Y0[8]	Cb0[8]	Y1[8]	Cr0[8]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D15	Y0[9]	Cb0[9]	Y1[9]	Cr0[9]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—

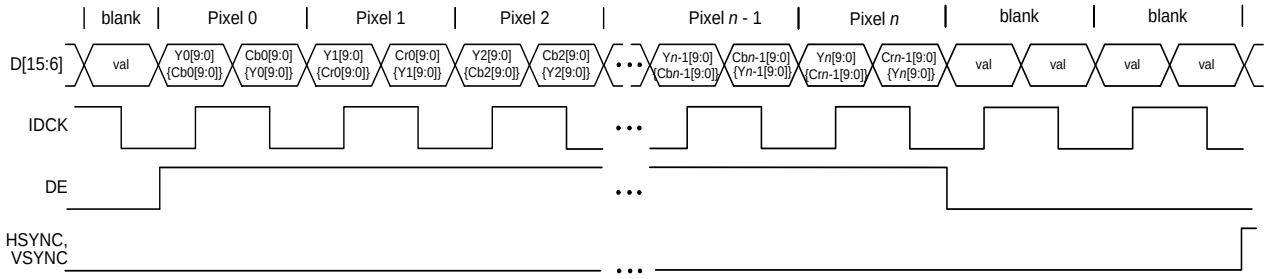

Figure 6.34. 10-Bit YC 4:2:2 Separate Sync Dual Edge Timing (49-Ball Package)

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Table 6.31. 12-Bit YC 4:2:2 Separate Sync Dual Edge Data Mapping (49-Ball Package)

Pin Name	12-bit Data Bus				12-bit Data Bus NB				12-bit Data Bus NB Swap			
	Pixel #0		Pixel #1		Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D[3:0]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D4	Y0[0]	Y0[8]	Y1[0]	Y1[8]	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	Y0[1]	Y0[9]	Y1[1]	Y1[9]	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	Y0[2]	Y0[10]	Y1[2]	Y1[10]	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D7	Y0[3]	Y0[11]	Y1[3]	Y1[11]	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D8	Cb0[0]	Cb0[4]	Cr0[0]	Cr0[4]	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	Cb0[1]	Cb0[5]	Cr0[1]	Cr0[5]	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	Cb0[2]	Cb0[6]	Cr0[2]	Cr0[6]	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D11	Cb0[3]	Cb0[7]	Cr0[3]	Cr0[7]	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D12	Y0[4]	Cb0[8]	Y1[4]	Cr0[8]	Y0[8]	Cb0[8]	Y1[8]	Cr0[8]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D13	Y0[5]	Cb0[9]	Y1[5]	Cr0[9]	Y0[9]	Cb0[9]	Y1[9]	Cr0[9]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D14	Y0[6]	Cb0[10]	Y1[6]	Cr0[10]	Y0[10]	Cb0[10]	Y1[10]	Cr0[10]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D15	Y0[7]	Cb0[11]	Y1[7]	Cr0[11]	Y0[11]	Cb0[11]	Y1[11]	Cr0[11]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
HSYNC	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—	HSYNC	—
VSYNC	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—	VSYNC	—
DE	DE	—	DE	—	DE	—	DE	—	DE	—	DE	—

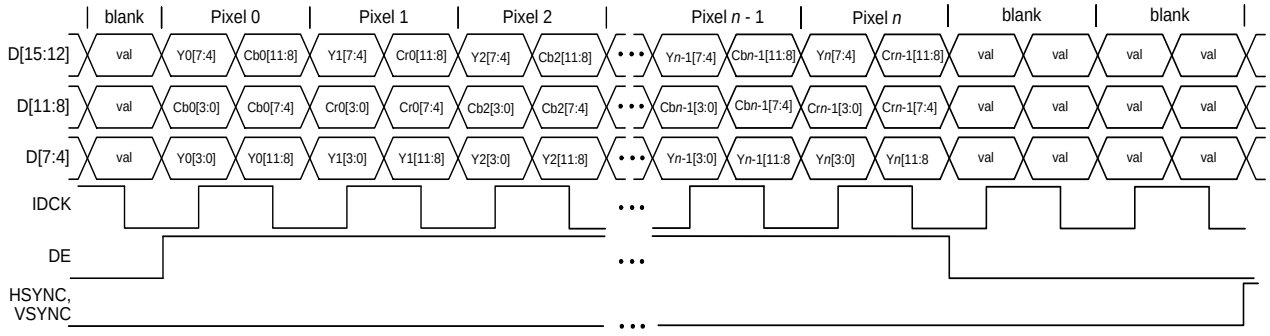

Figure 6.35. 12-Bit YC 4:2:2 Separate Sync Dual Edge Timing (49-Ball Package)

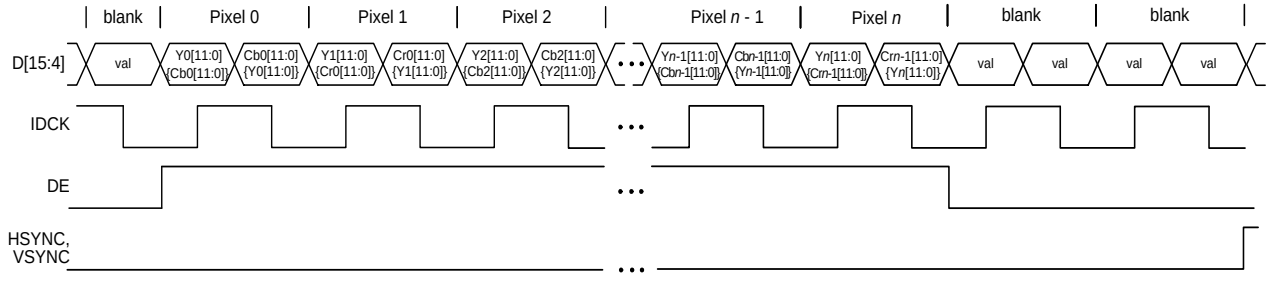

Figure 6.36. 12-Bit YC 4:2:2 Separate Sync NB Mode Dual Edge Timing (49-Ball Package)

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7. Design Recommendations

7.1. Power Supplies Decoupling

Designers should include adequate decoupling capacitors and a ferrite for each power supply, and an additional capacitor at each power ball or pin in the layout. These are shown schematically in Figure 7.1. Place these components as close as possible to the transmitter device balls or pins, and avoid routing through vias if possible, as shown in Figure 7.2, which represents a typical power connection on the transmitter. Connections in one group (such as AVCC12) can share C2, the ferrite, and C3, with each ball or pin having a separate C1 placed as close to the package as possible. Figure 7.2 shows one of the VFBGA packages; the same information applies to the 72-pin package.

Because of the low noise requirements of AVCC12, particular care ***must*** be taken to ensure the noise at the pin is less than 50 mV.

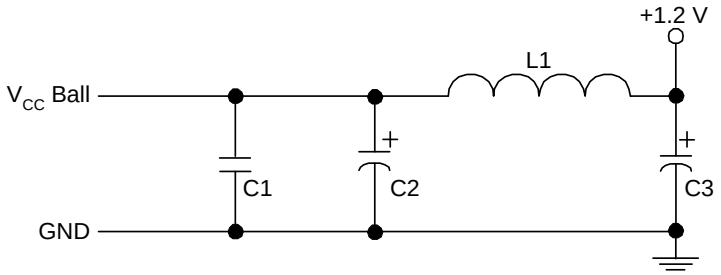

Figure 7.1. Decoupling and Bypass Schematic

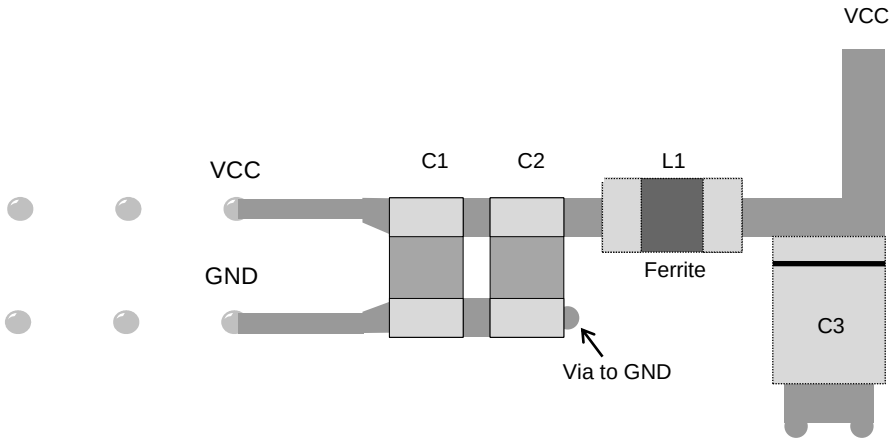

Figure 7.2. Decoupling and Bypass Capacitor Placement

7.2. High-Speed TMDS Signals

7.2.1. Source Termination

Source termination suppresses signal reflection and overshoot, and at the same time allows the transmitter to provide strong drive to support longer cables. The SiI9022A/SiI9024A transmitter supports internal source termination, which is disabled by default and can be enabled by programming. Lattice Semiconductor strongly recommends the use of internal source termination for applications running over 100 MHz.

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7.2.2. ESD Protection

The transmitter chip is designed to withstand electrostatic discharge during manufacturing handling. In applications where higher protection levels are required in the finished product, ESD-limiting components should be placed on all of the device pins connecting to an external interface. Special care should be taken on the TMDS signals to use low-capacitance ESD devices to minimize signal degradation. In no case should the capacitance value exceed 3 pF.

7.2.3. Transmitter Layout Guidelines

Place the transmitter chip as closely as possible to the output connector that carries the TMDS signals, and place the ESD diodes as close as possible to the HDMI connector. Route the differential signal lines together and as directly as possible from transmitter to connector. Lattice Semiconductor TMDS devices are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Avoid passing the TMDS lines through vias unless absolutely necessary when using the HDMI Type-D micro connector. The distance separating the two traces of the differential pair should be designed for 100-Ω differential impedance. An example of routing for the 49-ball package is shown in Figure 7.3. For additional ball grid array layout guidelines, refer to *Designing with BGA Packages* (listed in References section).

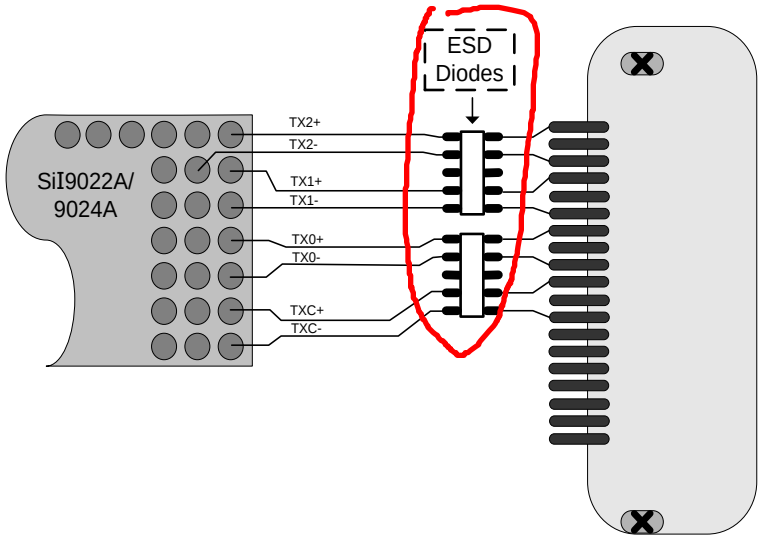

Figure 7.3. Transmitter to HDMI Connector Routing – Top View

7.3. Hot Plug Signal Conditioning

The HDMI interface provides a hot plug signal back to the host side from the display. This signal is generated by routing a 5 V source, in the host, through the cable to the display and back. The specification defines the minimum HIGH level for the hot plug as 2.0 V at the connector pin. The HPD signal is 5 V tolerant and can be connected to the HPD signal directly. However, an external pull down resistor of 10 kΩ is required, as shown in the circuit in Figure 7.5 on page 70, to guarantee that this CMOS input is not floating.

7.4. EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and additional factors. To control emissions, it is important not to place any passive components on the differential signal lines, except for the essential ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI, as long as the routing recommendations noted in the Transmitter Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground signals of the chip using a common ground.

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7.5. Typical Circuits

Representative circuits for using the transmitter chip are shown in Figure 7.4 through Figure 7.7. For a detailed review of your intended circuit implementation, contact your Lattice Semiconductor representative.

7.5.1. Power Supply Decoupling

Excessive noise on AVCC12 can cause improper PLL operation as the PLL tries to stay locked to the incoming video clock. Keep AVCC12 noise below the maximum allowable value V_{CCN} as specified in Table 3.2. If the ripple is higher than allowed for in the specifications, Lattice Semiconductor recommends using a separate power source to supply the AVCC12 inputs. The other power planes are relatively insensitive to ripple. Lattice Semiconductor recommends using low ESR capacitors. The 72-pin QFN package has an e-Pad which ***must*** be connected to the ground plane of the board.

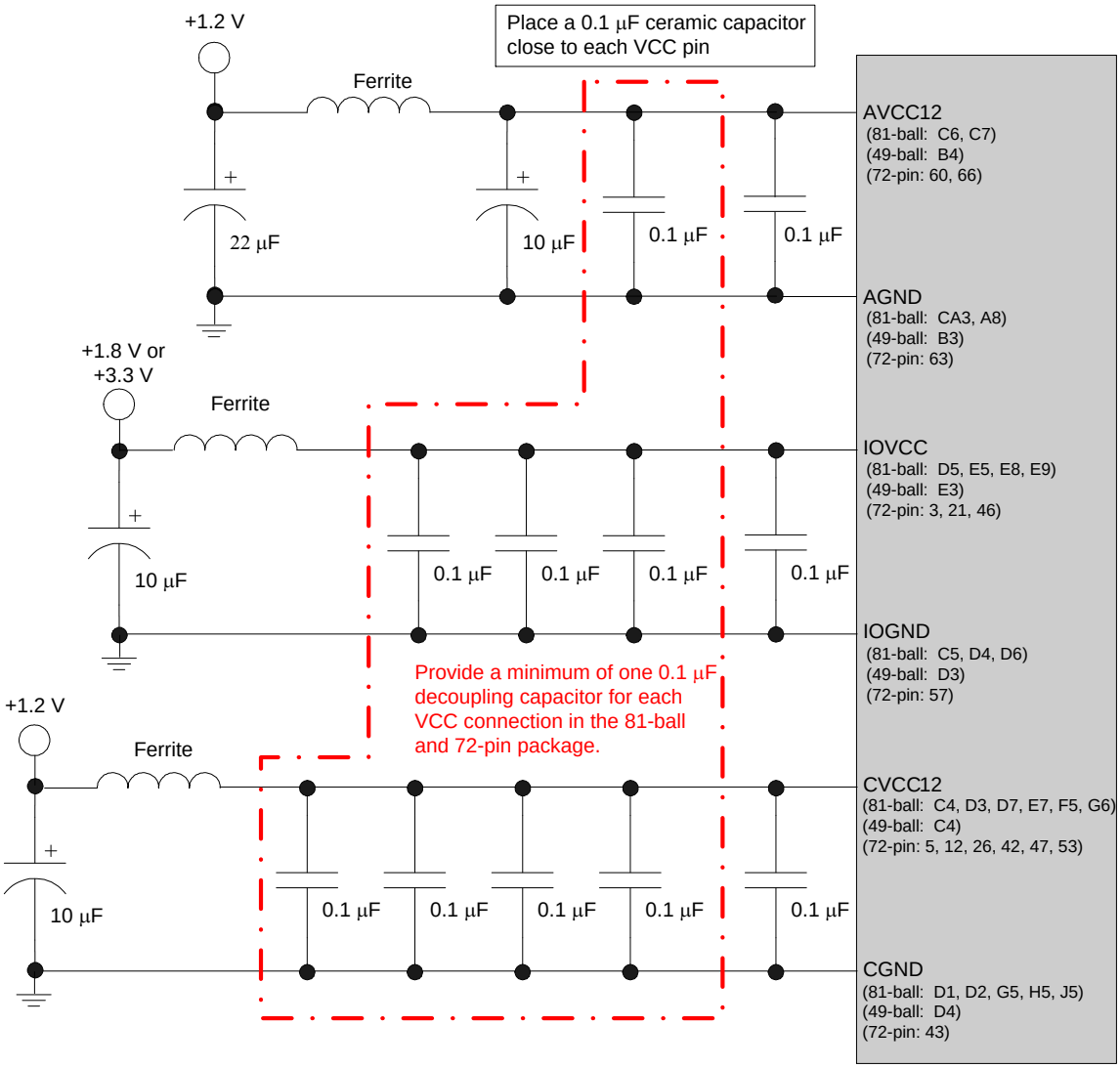

Figure 7.4. Power Supply Decoupling

Note: The 72-pin QFN package has an e-Pad which ***must*** be connected to the ground plane of the board.

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7.5.2. HDMI Port Connections

The suggested value for R_{EXT_SWING} is specified in the Differential Data Signals section on page 32. The Hot Plug Detect signal (HPD) is 5 V tolerant, so it is connected directly to the HDMI connector with a 10 kΩ pull-down resistor. No level-shifting circuit is needed for HPD.

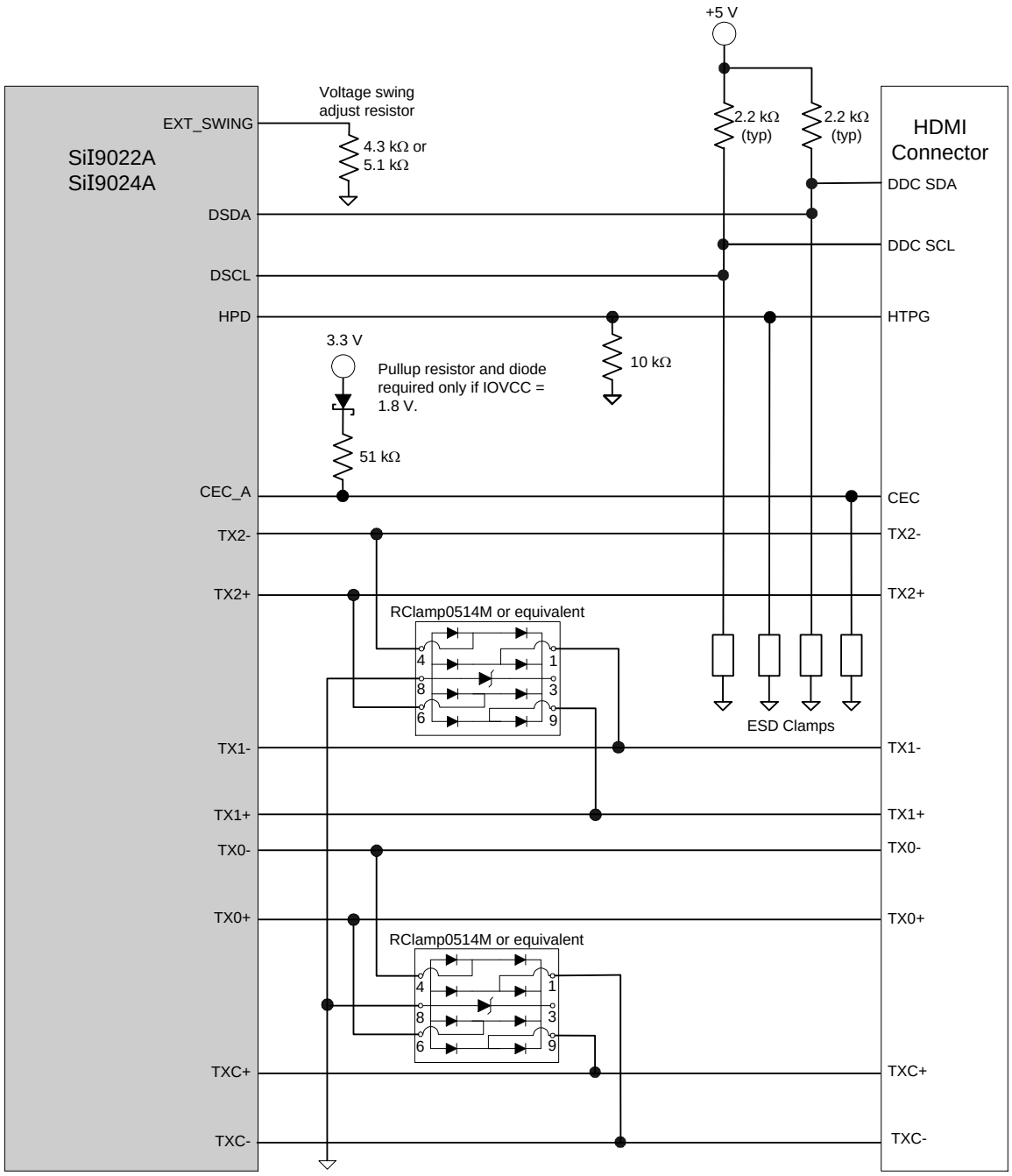

Figure 7.5. HDMI Port Connection Schematic

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7.5.3. Control Signal Connections

The general bus interconnection between the host processor and the transmitter is shown in Figure 7.6. The INT output can be connected as an interrupt to the processor, or the processor can poll a register to determine if any of the enabled interrupts have occurred.

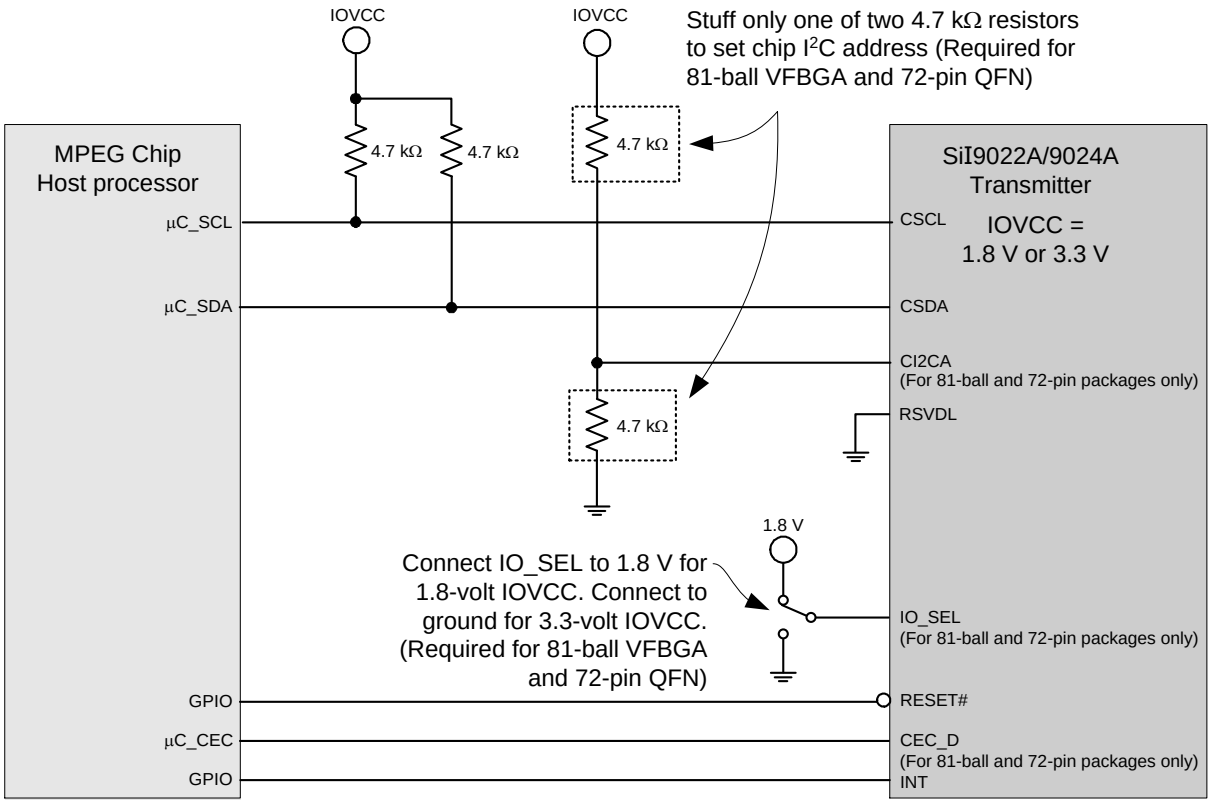

Figure 7.6. Controller Connections Schematic

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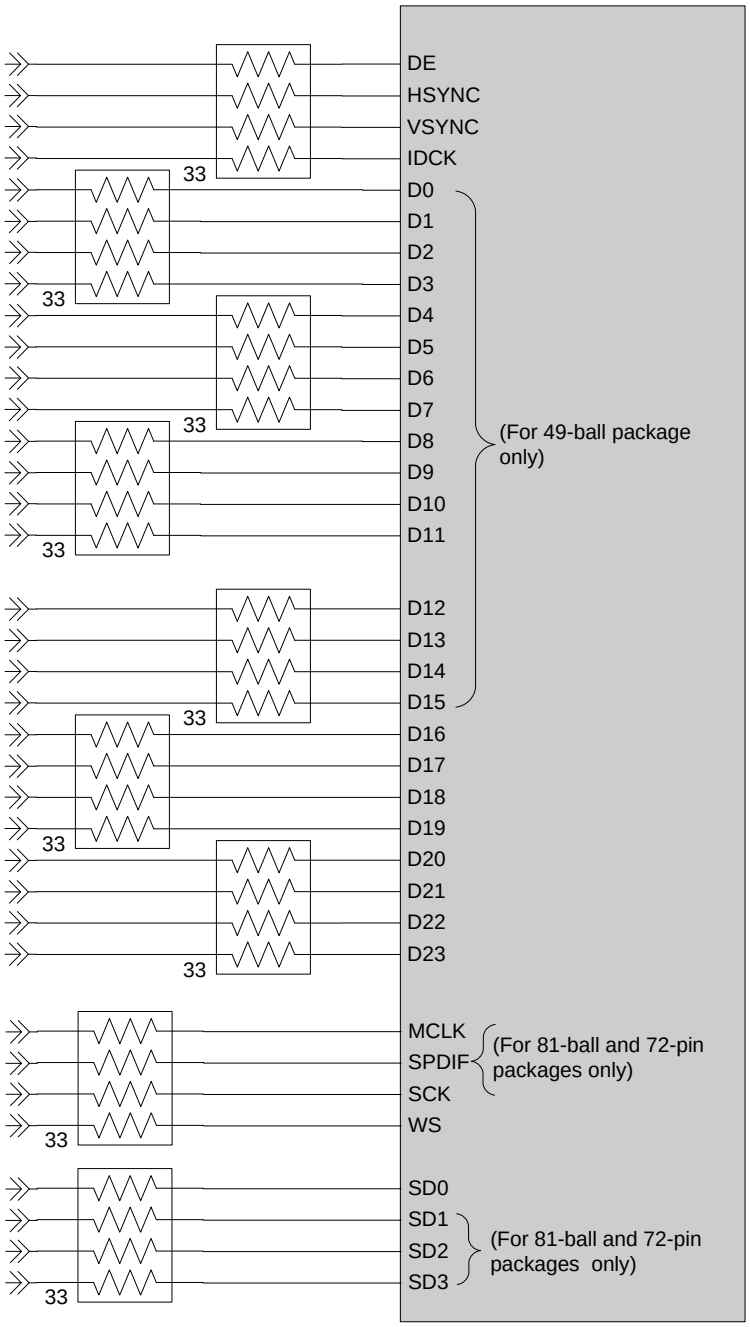
7.5.4. Digital Video Input Connections



Note: Some system designs may require series resistors to reduce reflections on the parallel input bus.

Figure 7.7. Digital Input Schematic

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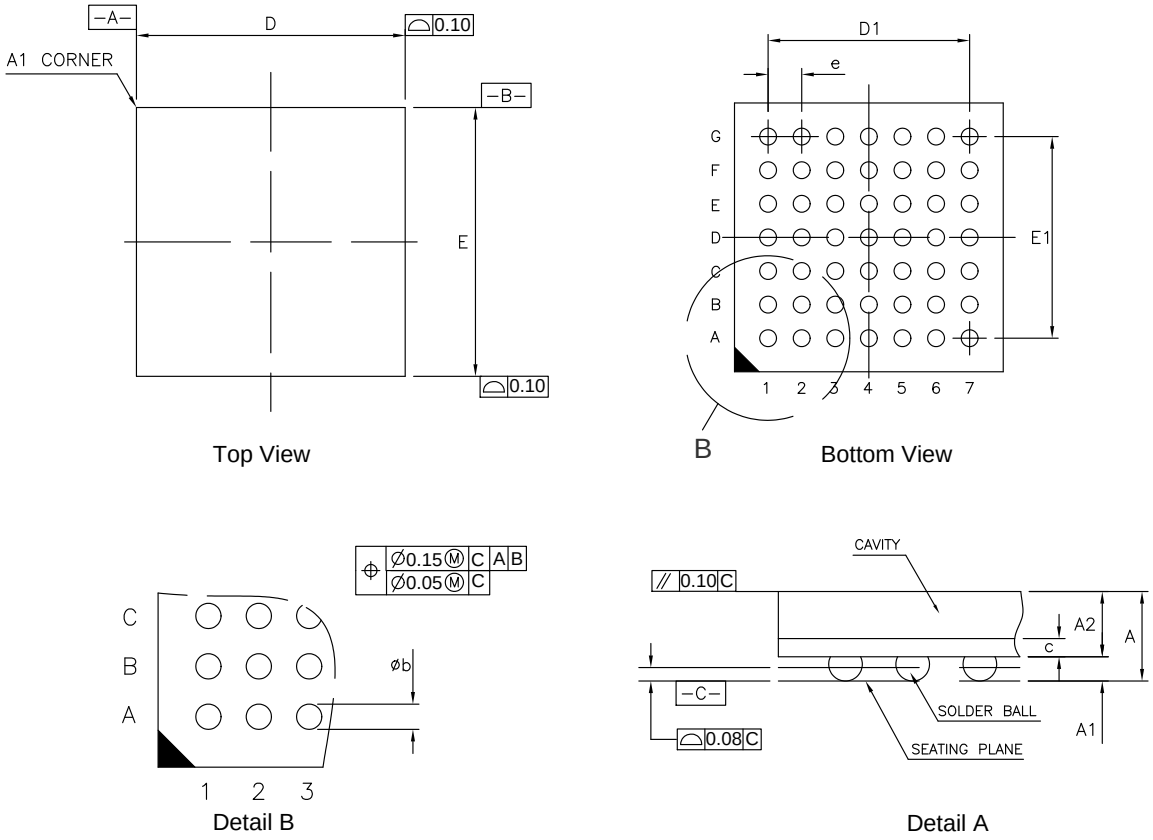
8. Packaging

8.1. 49-Ball Package Dimensions

These drawings are not to scale.



JEDEC Package Code MO-225

Item	Description	Min	Typ	Max
A	Thickness	—	—	0.80
A1	Stand-off	0.13	0.18	0.23
A2	Substrate thickness + Mold thickness	0.446	0.508	0.560
D	Body size	3.90	4.00	4.10
E	Body size	3.90	4.00	4.10
D1	Footprint	—	3.00	—
E1	Footprint	—	3.00	—
b	Ball width	0.20	0.25	0.30
e	Ball pitch	—	0.50	—

All dimensions are in millimeters.

Figure 8.1. 49-Ball VFBGA Package Diagram (SiI902*n*AYBT)

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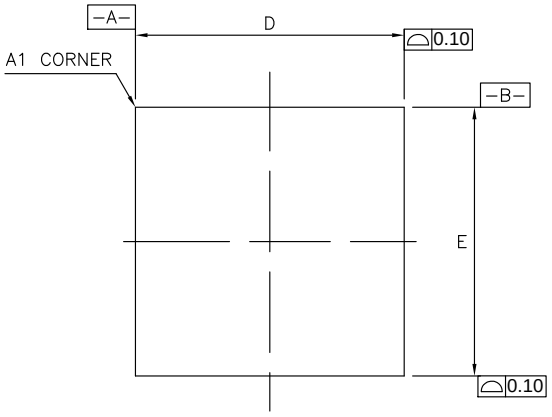
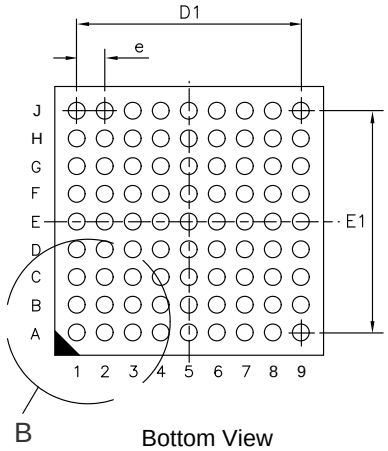
8.2. 81-Ball Package Dimensions

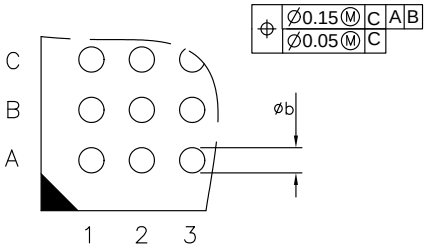
These drawings are not to scale.



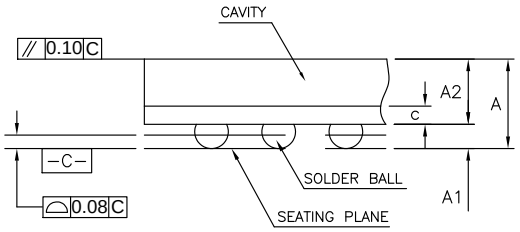
Top View



Bottom View



Detail B



Detail A

JEDEC Package Code MO-225

Item	Description	Min	Typ	Max
A	Thickness	—	—	0.80
A1	Stand-off	0.13	0.18	0.23
A2	Substrate thickness + Mold thickness	0.446	0.508	0.560
D	Body size	3.90	4.00	4.10
E	Body size	3.90	4.00	4.10
D1	Footprint	—	3.20	—
E1	Footprint	—	3.20	—
b	Ball width	0.20	0.25	0.30
e	Ball pitch	—	0.40	—

All dimensions are in millimeters.

Figure 8.2. 81-Ball VFBGA Package Diagram (SiI902*n*ARBT)

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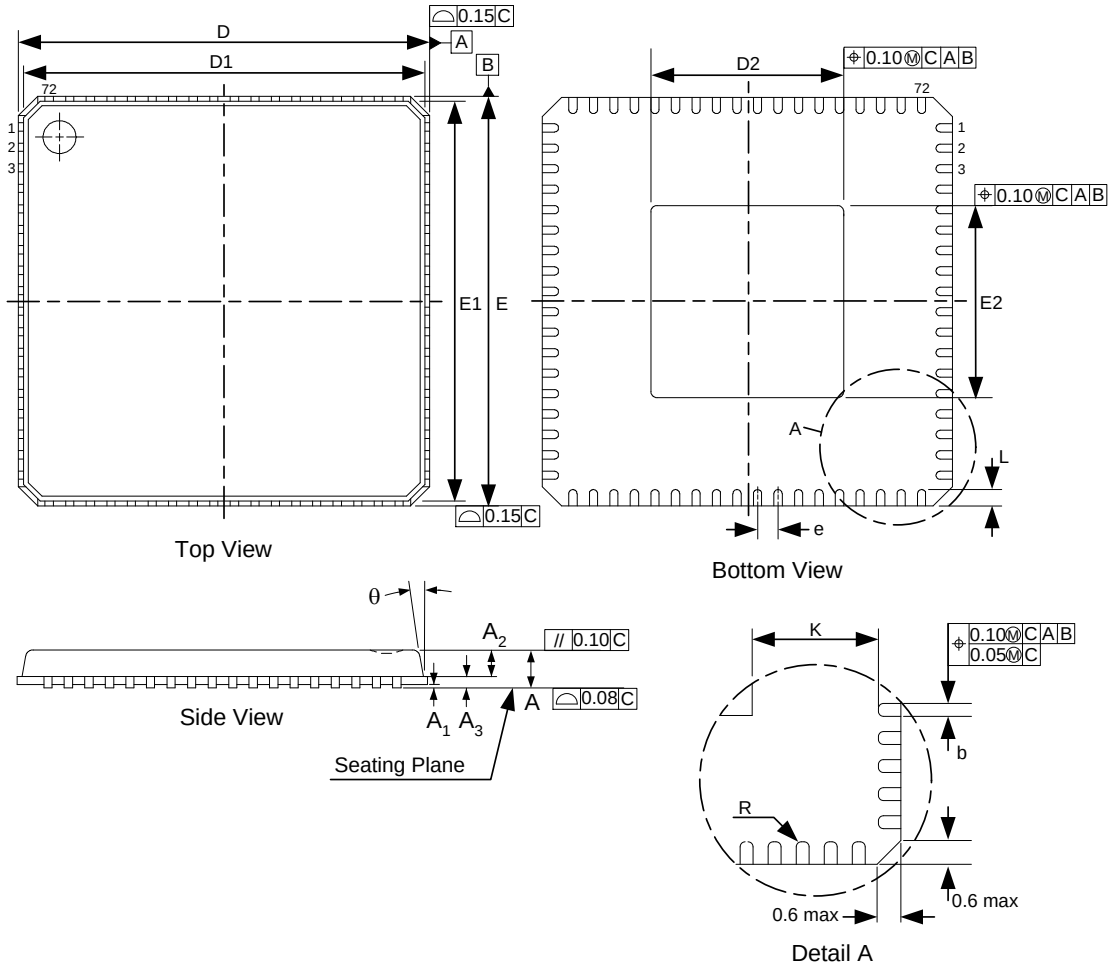
8.3. 72-Pin Package Dimensions

These drawings are not to scale.



JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A_1	Stand-off	0.00	0.02	0.05
A_2	Body thickness	0.60	0.65	0.70
A3		0.20 REF		
D	Footprint	10.00 BSC		
E	Footprint	10.00 BSC		
D_1	Body size	9.75 BSC		
E_1	Body size	9.75 BSC		

Item	Description	Min	Typ	Max
D2	ePad size	4.55	4.70	4.85
E2	ePad size	4.55	4.70	4.85
b	Plated lead width	0.18	0.23	0.28
e	Lead pitch	0.50 BSC		
K	ePad-to-pin clearance	0.20	—	—
L	Lead foot length	0.30	0.40	0.50
R	Lead radius	0.09	—	—
θ	Lead foot angle	0°	—	14°

All dimensions are in millimeters.

Figure 8.3. 72-Pin QFN Package Diagram (SiI902*n*ACNU)

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8.4. Marking Specification

Marking drawings are not to scale.

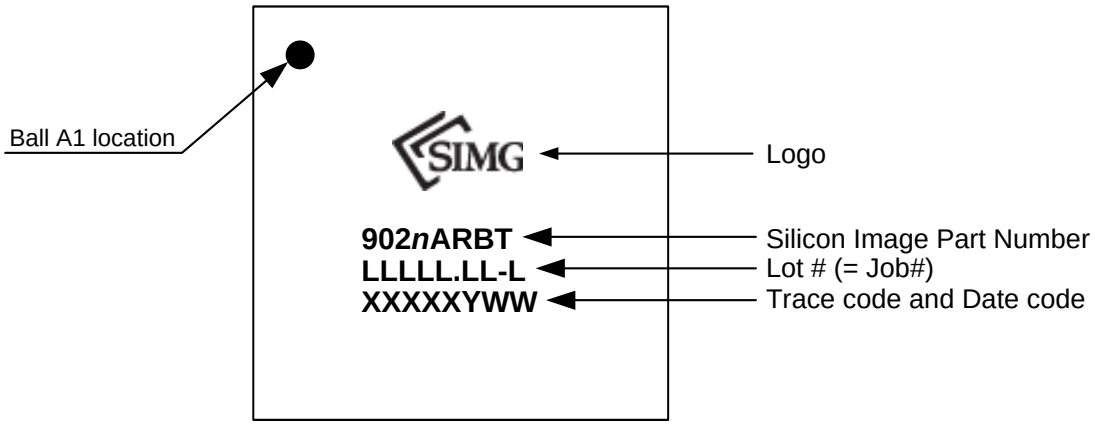

Figure 8.4. Marking Diagram (SiI902*n*ARBT)

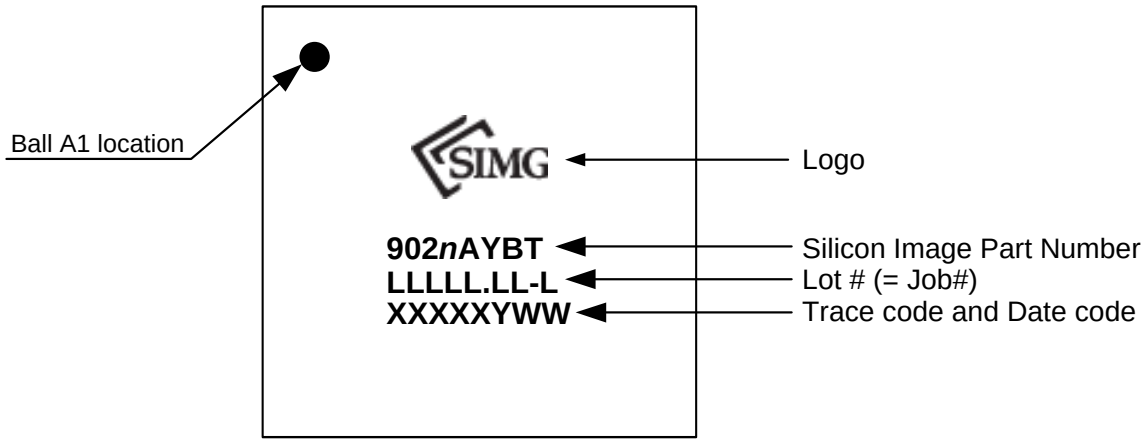

Figure 8.5. Marking Diagram (SiI902*n*AYBT)

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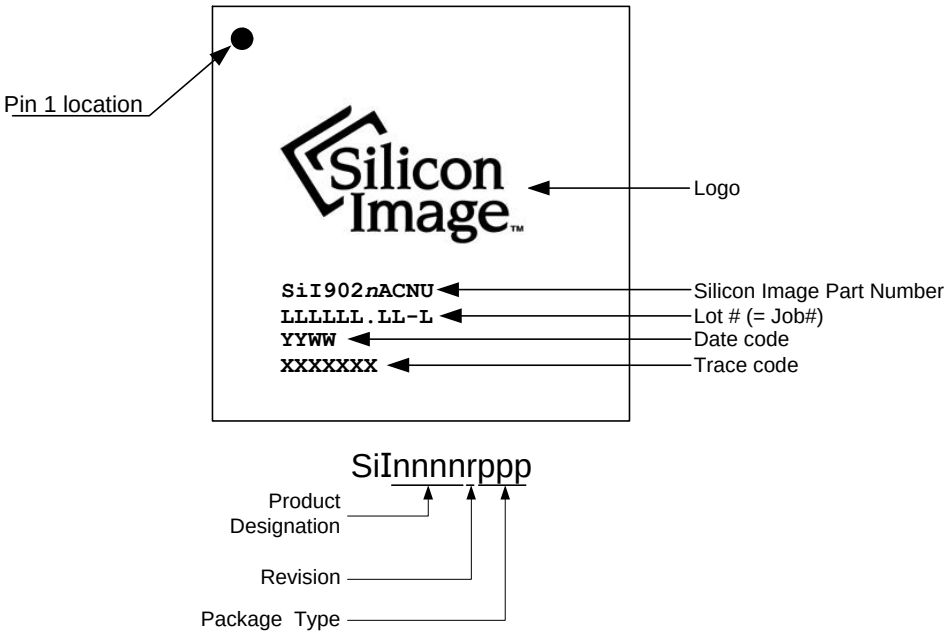

Figure 8.6. Marking Diagram (SiI902*n*ACNU)

8.5. Ordering Information

Part Numbers	Package Type	Pixel Clock Range	Security	Temperature Grade
SiI9022ARBT	81-ball 4 × 4 mm VFBGA	25 MHz –165 MHz	—	Extended (–20 °C to +85 °C)
SiI9022AYBT	49-ball 4 × 4 mm VFBGA	25 MHz –165 MHz	—	Extended (–20 °C to +85 °C)
SiI9022ACNU	72-pin 10 × 10 mm QFN	25 MHz –165 MHz	—	Extended (–20 °C to +85 °C)
SiI9024ARBT	81-ball 4 × 4 mm VFBGA	25 MHz –165 MHz	HDCP	Extended (–20 °C to +85 °C)
SiI9024AYBT	49-ball 4 × 4 mm VFBGA	25 MHz –165 MHz	HDCP	Extended (–20 °C to +85 °C)
SiI9024ACNU	72-pin 10 × 10 mm QFN	25 MHz –165 MHz	HDCP	Extended (–20 °C to +85 °C)

The universal package can be used in both lead-free and ordinary process lines.

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References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface,* Revision 1.4a, HDMI Consortium; March 2010
HCTS	*HDMI Compliance Test Specification,* Revision 1.4a, HDMI Consortium; March 2010
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital Content Protection, LLC; December 2006
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-EDID IG	*VESA EDID Implementation Guide*, Version 1.0, VESA; June 2001
CEA-861-E	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; March 2008
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative.

The Programmer's Reference requires an NDA with Lattice Semiconductor.

Document	Title
SiI-PR-1032	*Transmitter Programming Interface (TPI) Programmer's Reference*
SiI-PR-0020	*SiI9020 HDMI PanelLink Transmitter Programmer's Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*
SiI-AN-1016	*Designing with BGA Packages*
SiI-AN-1029	*Layout Guidelines and Results for Using HDMI Type-D Micro-Connector with SiI902nA Devices*
SiI-UG-1043	*CP9022AR/CP9024AR/CP9022AY/CP9024AY HDMI Transmitter Starter Kit User Guide*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

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Revision History

Revision E.01, August 2016

Formatted to latest template. No content has been changed.

Revision E, October 2015

Updated description of CSCL item in the Configuration and Control Signals section. Updated copyright information and legal disclaimers.

Revision D.01, January 2011

Updated Table 3.3. DC Digital I/O Specifications: IOVCC = 1.8 V, Table 3.4. DC Digital I/O Specifications: IOVCC = 3.3 V, Table 3.10. I2S Input Port Timings; corrected 1080p 24 Hz 3D lines.

Revision C.01, September 2010

Removed Patent information from DB, rolled the revision for DS.

Revision C, July 2010

Added information about L + D, and Top-and-Bottom modes; added Limitations section.

Revision B.01, April 2010

Update with new features; minor corrections and changes.

Revision B, December 2009

Updated to add 81-ball and 72-pin information; added Pixel Number to Data Mapping tables.

Revision A.01, November 2009

Update specification tables; minor corrections throughout.

Revision A, November 2009

First production release.

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