

# 74ALVT16260

12-bit to 24-bit multiplexed D-type latches; 3-state

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Product data sheet

## 1. General description

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The 74ALVT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1 to A12, 1B1 to 1B12 and 2B1 to 2B12) are available for address or data transfer. The output enable inputs ( $\overline{OE1B}$ ,  $\overline{OE2B}$ , and  $\overline{OE A}$ ) control the bus transceiver functions.  $\overline{OE1B}$  and  $\overline{OE2B}$  also allow bank control in the A to B direction.

Address or data information can be stored using the internal storage latches. The latch enable inputs (LE1B, LE2B, LEA1B and LEA2B) are used to control data storage. When the latch enable input is HIGH, the latch is transparent. When the latch enable input goes LOW, the data present at the inputs is latched and remains latched until the latch enable input is returned HIGH.

To ensure the high-impedance state during power-up or power-down, all output enable inputs should be tied to  $V_{CC}$  through a pull-up resistor. The minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ALVT16260 is available in a SSOP56 and a TSSOP56 package.

## 2. Features

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- 5 V I/O compatible
- Bus hold inputs eliminate the need for external pull-up resistors
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Output capability: +64 mA and -32 mA
- Distributed  $V_{CC}$  and GND pin configuration minimizes high-speed switching noise
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883C, method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

**PHILIPS**

### 3. Quick reference data

**Table 1. Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 2.5\text{ V}</math></b>						
$I_{CC}$	quiescent supply current	$V_{CC} = 2.7\text{ V}$ ; $V_I = GND$ or $V_{CC}$ ; $I_O = 0\text{ A}$ ; outputs disabled	[1]	-	40	- $\mu\text{A}$
$t_{PLH}$	LOW-to-HIGH propagation delay An to xBn; xBn to An	$C_L = 50\text{ pF}$	-	2.8	-	ns
$t_{PHL}$	HIGH-to-LOW propagation delay An to xBn; xBn to An	$C_L = 50\text{ pF}$	-	2.7	-	ns
$C_i$	input capacitance (control pins)	$V_I = 0\text{ V}$ or $V_{CC}$		4	-	pF
$C_{io}$	input/output capacitance (I/O pins)	$V_{I/O} = 0\text{ V}$ or $5.0\text{ V}$		9	-	pF
<b><math>V_{CC} = 3.3\text{ V}</math></b>						
$I_{CC}$	quiescent supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = GND$ or $V_{CC}$ ; $I_O = 0\text{ A}$ ; outputs disabled	[1]	-	60	- $\mu\text{A}$
$t_{PLH}$	LOW-to-HIGH propagation delay An to xBn; xBn to An	$C_L = 50\text{ pF}$	-	2.2	-	ns
$t_{PHL}$	HIGH-to-LOW propagation delay An to xBn; xBn to An	$C_L = 50\text{ pF}$	-	2.0	-	ns
$C_i$	input capacitance (control pins)	$V_I = 0\text{ V}$ or $V_{CC}$		4	-	pF
$C_{io}$	input/output capacitance (I/O pins)	$V_{I/O} = 0\text{ V}$ or $5.0\text{ V}$		9	-	pF

[1]  $I_{CC}$  is measured with outputs pulled up to  $V_{CC}$  or pulled down to ground.

### 4. Ordering information

**Table 2. Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
74ALVT16260DL	-40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ALVT16260DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram

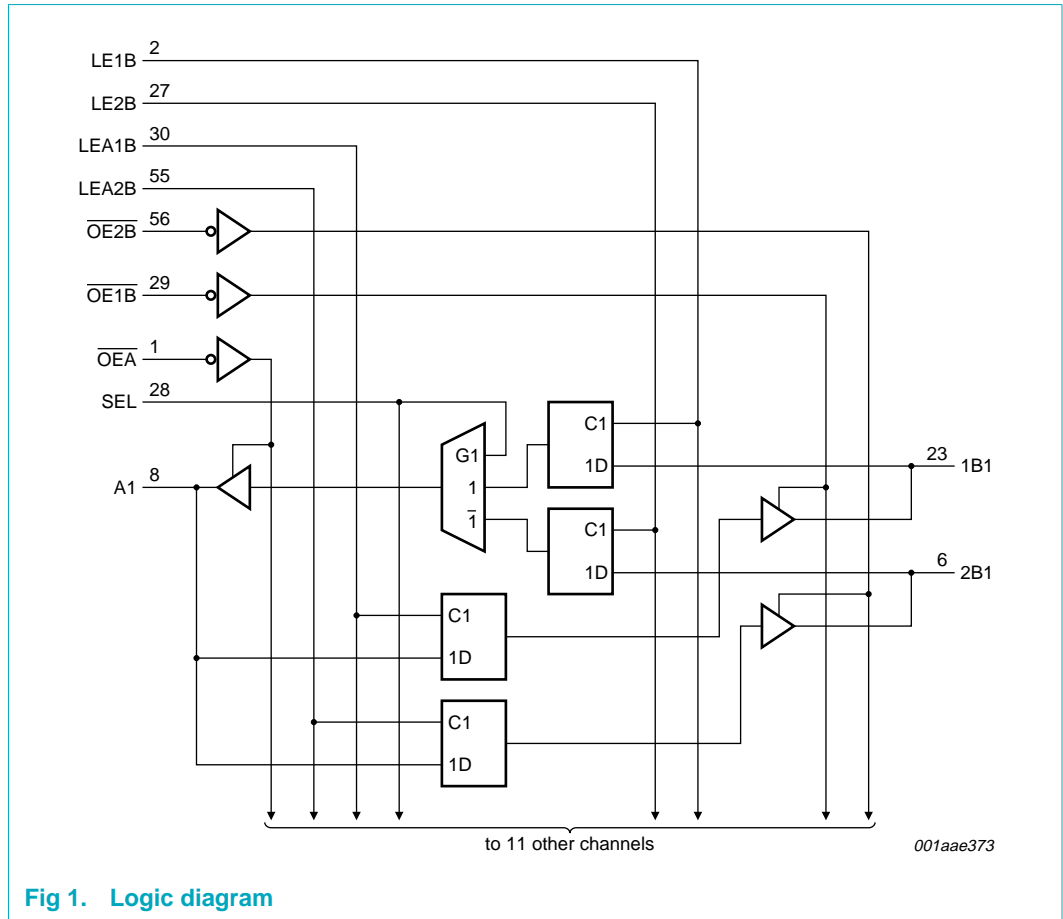
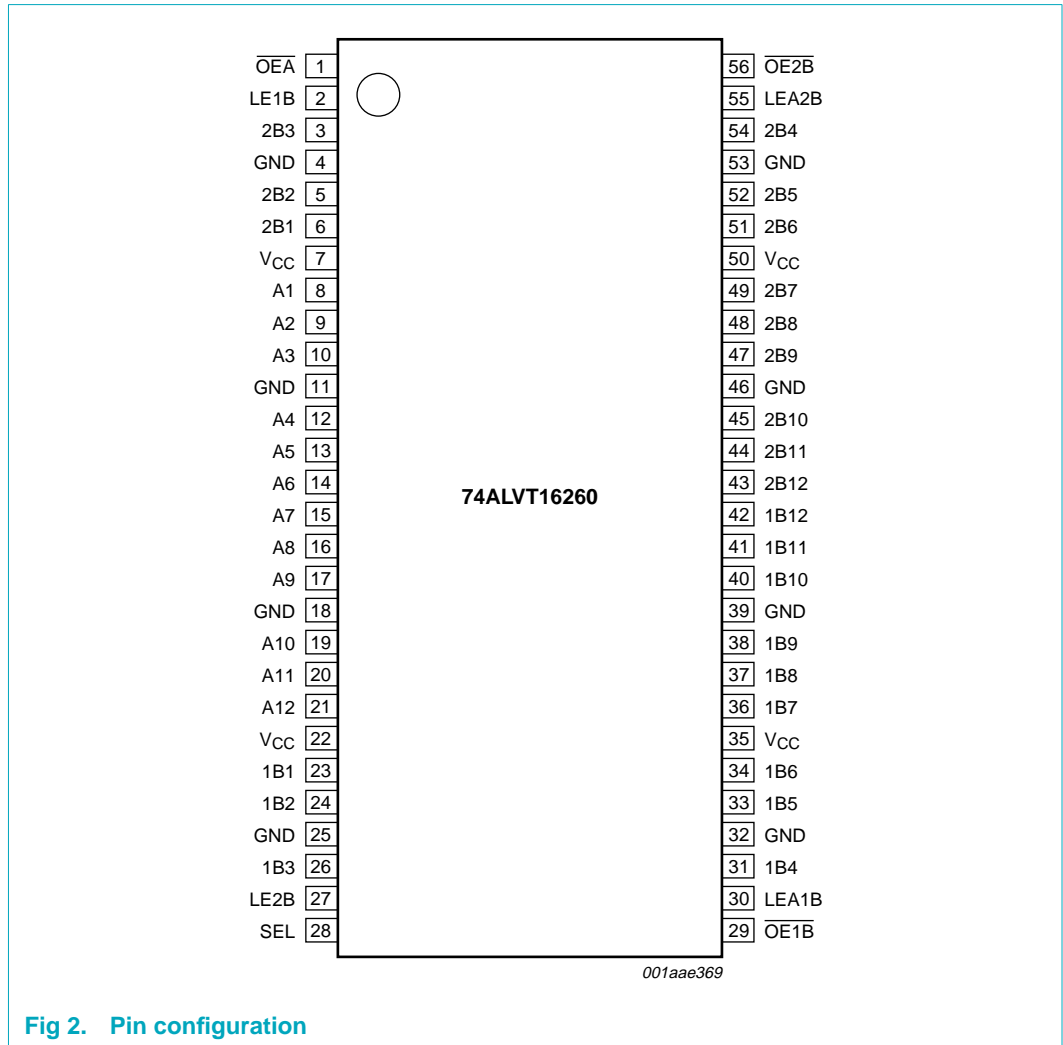


Fig 1. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin	Description
$\overline{OE}A$	1	output A enable input (active LOW)
LE1B	2	latch 1B to A enable input
2B3	3	2 data input/output B3
GND	4	ground (0 V)
2B2	5	2 data input/output B2
2B1	6	2 data input/output B1
V <sub>CC</sub>	7	supply voltage
A1	8	data input/output A1

Table 3. Pin description ...continued

Symbol	Pin	Description
A2	9	data input/output A2
A3	10	data input/output A3
GND	11	ground (0 V)
A4	12	data input/output A4
A5	13	data input/output A5
A6	14	data input/output A6
A7	15	data input/output A7
A8	16	data input/output A8
A9	17	data input/output A9
GND	18	ground (0 V)
A10	19	data input/output A10
A11	20	data input/output A11
A12	21	data input/output A12
V <sub>CC</sub>	22	supply voltage
1B1	23	1 data input/output B1
1B2	24	1 data input/output B2
GND	25	ground (0 V)
1B3	26	1 data input/output B3
LE2B	27	latch 2B to A enable input
SEL	28	select B1 or B2 input
$\overline{OE1B}$	29	output 1B enable input (active LOW)
LEA1B	30	latch A to 1B enable input
1B4	31	data input/output B4
GND	32	ground (0 V)
1B5	33	1 data input/output B5
1B6	34	1 data input/output B6
V <sub>CC</sub>	35	supply voltage
1B7	36	1 data input/output B7
1B8	37	1 data input/output B8
1B9	38	1 data input/output B9
GND	39	ground (0 V)
1B10	40	1 data input/output B10
1B11	41	1 data input/output B11
1B12	42	1 data input/output B12
2B12	43	2 data input/output B12
2B11	44	2 data input/output B11
2B10	45	2 data input/output B10
GND	46	ground (0 V)
2B9	47	2 data input/output B9
2B8	48	2 data input/output B8
2B7	49	2 data input/output B7

**Table 3. Pin description ...continued**

Symbol	Pin	Description
V <sub>CC</sub>	50	supply voltage
2B6	51	2 data input/output B6
2B5	52	2 data input/output B5
GND	53	ground (0 V)
2B4	54	2 data input/output B4
LEA2B	55	latch A to 2B enable input
$\overline{OE2B}$	56	output 2B enable input (active LOW)

## 7. Functional description

### 7.1 Function table

**Table 4. Function table of input B to output A;  $\overline{OE1B} = H$  and  $\overline{OE2B} = H$  [1]**

Control				Input		Output
$\overline{OE A}$	SEL	LE1B	LE2B	1Bn	2Bn	An
L	H	H	X	H	X	H
				L	X	L
		L	X	X	X	An
	L	X	H	X	H	H
				X	L	L
		X	L	X	X	An
H	X	X	X	X	X	Z

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 An = HIGH or LOW voltage level one setup time prior to the HIGH-to-LOW LExB transition.

**Table 5. Function table of input A to output B;  $\overline{OE A} = H$  [1]**

Control				Input	Output	
$\overline{OE1B}$	$\overline{OE2B}$	LEA1B	LEA2B	An	1Bn	2Bn
L	L	H	H	H	H	H
		H	H	L	L	L
		H	L	L	L	2Bn
		H	L	H	H	2Bn
		L	H	H	1Bn	H
		L	H	L	1Bn	L
		L	L	X	1Bn	2Bn
L	L	X	X	X	active	active
	H	X	X	X	active	Z
H	L	X	X	X	Z	active
	H	X	X	X	Z	Z

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 1Bn = HIGH or LOW voltage level one setup time prior to the HIGH-to-LOW LEA2B transition;  
 2Bn = HIGH or LOW voltage level one setup time prior to the HIGH-to-LOW LEA1B transition;  
 active = HIGH or LOW voltage level.

## 8. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		[2] -	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Recommended operating conditions

**Table 7. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 2.5</math> V</b>						
$V_{CC}$	supply voltage		2.3	-	2.7	V
$V_I$	input voltage		0	-	5.5	V
$V_{IH}$	HIGH-state input voltage		1.7	-	-	V
$V_{IL}$	LOW-state input voltage		-	-	0.7	V
$I_{OH}$	HIGH-state output current		-	-	-8	mA
$I_{OL}$	LOW-state output current	none	-	-	8	mA
		current duty cycle $\leq 50$ %; $f \geq 1$ kHz	-	-	24	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
$T_{amb}$	ambient temperature		-40	-	+85	°C
<b><math>V_{CC} = 3.3</math> V</b>						
$V_{CC}$	supply voltage		3.0	-	3.6	V

Table 7. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_I$	input voltage		0	-	5.5	V
$V_{IH}$	HIGH-state input voltage		2.0	-	-	V
$V_{IL}$	LOW-state input voltage		-	-	0.8	V
$I_{OH}$	HIGH-state output current		-	-	-32	mA
$I_{OL}$	LOW-state output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$ ; $f \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}\text{C}$

## 10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math> [1]</b>							
$V_{IK}$	input clamping voltage	$V_{CC} = 2.3\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V	
$V_{OH}$	HIGH-state output voltage	$V_{CC} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC}$	-	V	
		$V_{CC} = 2.3\text{ V}$ ; $I_{OH} = -8\text{ mA}$	1.8	2.1	-	V	
$V_{OL}$	LOW-state output voltage	$V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V	
		$V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V	
$V_{RST}$	power-up LOW-state output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = V_{CC}$ or GND	[2]	-	0.55	V	
$I_{LI}$	input leakage current	control pins	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1$	$\mu\text{A}$
			$V_{CC} = 0\text{ V}$ or $2.7\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
	I/O data pins	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$	[3]	-	0.1	1	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V}$ ; $V_I = 0\text{ V}$	[3]	-	+0.1	-5	$\mu\text{A}$
		$V_{CC} = 0\text{ V}$ or $2.7\text{ V}$ ; $V_I = 5.5\text{ V}$	-	-	0.1	20	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$	-	0.1	$\pm 100$	$\mu\text{A}$	
$I_{HOLD}$	bus hold current data input	$V_{CC} = 2.3\text{ V}$ ; $V_I = 0.7\text{ V}$	[4]	-	90	-	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V}$ ; $V_I = 1.7\text{ V}$	[4]	-	-10	-	$\mu\text{A}$
$I_{EX}$	external current into output	output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 2.3\text{ V}$	-	10	125	$\mu\text{A}$	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{OE}x = \text{don't care}$	[5]	-	1	100	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_{CC} = 2.7\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$					
		outputs HIGH-state	-	0.04	0.1	mA	
		outputs LOW-state	-	2.7	4.5	mA	
		outputs disabled	[6]	-	0.04	0.1	mA

**Table 8. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

 $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$\Delta I_{CC}$	additional quiescent supply current	per input pin; $V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND	[7] -	0.04	0.4	mA	
$C_i$	input capacitance (control pins)	$V_I = 0\text{ V}$ or $V_{CC}$	-	4	-	pF	
$C_{io}$	input/output capacitance (I/O pins)	$V_{I/O} = 0\text{ V}$ or $5.0\text{ V}$	-	9	-	pF	
<b><math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math>[8]</b>							
$V_{IK}$	input clamping voltage	$V_{CC} = 3.0\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V	
$V_{OH}$	HIGH-state output voltage	$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC}$	-	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.3	-	V	
$V_{OL}$	LOW-state output voltage	$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$	[3] -	0.07	0.2	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$	[3] -	0.25	0.4	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$	[3] -	0.3	0.5	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 64\text{ mA}$	[3] -	0.4	0.55	V	
$V_{RST}$	power-up LOW-state output voltage	$V_{CC} = 3.6\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = V_{CC}$ or GND	[2] -	-	0.55	V	
$I_{LI}$	input leakage current	control pins	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1$	$\mu\text{A}$
			$V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
	I/O data pins	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$	[3] -	0.1	1	$\mu\text{A}$	
		$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$	[3] -	+0.1	-5	$\mu\text{A}$	
		$V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	20	$\mu\text{A}$	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$	-	0.1	$\pm 100$	$\mu\text{A}$	
$I_{HOLD}$	bus hold current data input	$V_{CC} = 3\text{ V}$ ; $V_I = 0.8\text{ V}$	[4] 75	130	-	$\mu\text{A}$	
		$V_{CC} = 3\text{ V}$ ; $V_I = 2.0\text{ V}$	[4] -75	-140	-	$\mu\text{A}$	
		$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$	[4] $\pm 500$	-	-	$\mu\text{A}$	
$I_{EX}$	external current into output	output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.0\text{ V}$	-	10	125	$\mu\text{A}$	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{\text{OEx}} = \text{don't care}$	[9] -	1	$\pm 100$	$\mu\text{A}$	
$I_{CC}$	quiescent supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$					
		outputs HIGH-state	-	0.04	0.1	mA	
		outputs LOW-state	-	3.7	6	mA	
$\Delta I_{CC}$	additional quiescent supply current	per input pin; $V_{CC} = 3\text{ V}$ to $3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND	[7] -	0.04	0.4	mA	
$C_i$	input capacitance (control pins)	$V_I = 0\text{ V}$ or $V_{CC}$	-	4	-	pF	
$C_{io}$	input/output capacitance (I/O pins)	$V_{I/O} = 0\text{ V}$ or $5.0\text{ V}$	-	9	-	pF	

[1] Typical values are measured at  $V_{CC} = 2.5\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

- [3] Unused pins at  $V_{CC}$  or GND.
- [4] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [5] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2$  V to  $V_{CC} = 2.5$  V  $\pm$  0.2 V a transition time of 100  $\mu$ s is permitted. This parameter is valid for  $T_{amb} = 25$  °C only.
- [6]  $I_{CC}$  is measured with outputs pulled up to  $V_{CC}$  or pulled down to ground.
- [7] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.
- [8] All typical values are measured at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.
- [9] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2$  V to  $V_{CC} = 3.3$  V  $\pm$  0.3 V a transition time of 100  $\mu$ s is permitted. This parameter is valid for  $T_{amb} = 25$  °C only.

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#);  
 $T_{amb} = -40$  °C to  $+85$  °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 2.5</math> V <math>\pm</math> 0.2 V</b>						
$t_{PLH}$	LOW-to-HIGH propagation delay	see <a href="#">Figure 3</a>				
	An to xBn; xBn to An		0.8	2.8	5.2	ns
	LExB to An; LEAxB to xBn		1.1	3.1	5.6	ns
	SEL(1Bn) to An		1.2	2.9	4.8	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	see <a href="#">Figure 3</a>				
	An to xBn; xBn to An		1.1	2.7	4.9	ns
	LExB to An; LEAxB to xBn		0.9	2.8	5.3	ns
	SEL(1Bn) to An		1.1	2.4	4.5	ns
$t_{PZH}$	output enable time to HIGH-state	see <a href="#">Figure 4</a>				
	$\overline{OEA}$ to An; $\overline{OE1B}$ to 1Bn; $\overline{OE2B}$ to 2Bn		1.8	3.5	5.5	ns
$t_{PZL}$	output enable time to LOW-state	see <a href="#">Figure 4</a>				
	$\overline{OEA}$ to An; $\overline{OE1B}$ to 1Bn; $\overline{OE2B}$ to 2Bn		1.3	2.8	4.6	ns
$t_{PHZ}$	output disable time from HIGH-state	see <a href="#">Figure 4</a>				
	$\overline{OEA}$ to An; $\overline{OE1B}$ to 1Bn; $\overline{OE2B}$ to 2Bn		1.8	2.8	4.6	ns
$t_{PLZ}$	output disable time from LOW-state	see <a href="#">Figure 4</a>				
	$\overline{OEA}$ to An; $\overline{OE1B}$ to 1Bn; $\overline{OE2B}$ to 2Bn		1.0	2.2	3.4	ns
$t_{su}$	setup time	see <a href="#">Figure 5</a>				
	An to LEAxB; xBn to LExB		1.0	-	-	ns
$t_h$	hold time	see <a href="#">Figure 5</a>				
	LEAxB to An; LExB to xBn		1.0	-	-	ns
$t_w$	pulse width	see <a href="#">Figure 5</a>				
	LExB HIGH; LEAxB HIGH		3.3	-	-	ns

**Table 9. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#);

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>						
t <sub>PLH</sub>	LOW-to-HIGH propagation delay	see <a href="#">Figure 3</a>				
	An to xBn; xBn to An		0.7	2.2	3.6	ns
	LExB to An; LEAxB to xBn		1.0	2.4	4.1	ns
	SEL(1Bn) to An		1.0	2.2	3.4	ns
t <sub>PHL</sub>	HIGH-to-LOW propagation delay	see <a href="#">Figure 3</a>				
	An to xBn; xBn to An		0.7	2.0	3.4	ns
	LExB to An; LEAxB to xBn		1.1	2.3	3.9	ns
	SEL(1Bn) to An		1.0	2.0	3.3	ns
t <sub>PZH</sub>	output enable time to HIGH-state	see <a href="#">Figure 4</a>				
	$\overline{OE}A$ to An; $\overline{OE}1B$ to 1Bn; $\overline{OE}2B$ to 2Bn		1.1	2.7	4.1	ns
t <sub>PZL</sub>	output enable time to LOW-state	see <a href="#">Figure 4</a>				
	$\overline{OE}A$ to An; $\overline{OE}1B$ to 1Bn; $\overline{OE}2B$ to 2Bn		1.1	2.1	3.2	ns
t <sub>PHZ</sub>	output disable time from HIGH-state	see <a href="#">Figure 4</a>				
	$\overline{OE}A$ to An; $\overline{OE}1B$ to 1Bn; $\overline{OE}2B$ to 2Bn		2.4	3.4	4.8	ns
t <sub>PLZ</sub>	output disable time from LOW-state	see <a href="#">Figure 4</a>				
	$\overline{OE}A$ to An; $\overline{OE}1B$ to 1Bn; $\overline{OE}2B$ to 2Bn		2.0	3.0	4.0	ns
t <sub>su</sub>	setup time	see <a href="#">Figure 5</a>				
	An to LEAxB; xBn to LExB		1	-	-	ns
t <sub>h</sub>	hold time	see <a href="#">Figure 5</a>				
	LEAxB to An; LExB to xBn		1	-	-	ns
t <sub>w</sub>	pulse width	see <a href="#">Figure 5</a>				
	LExB HIGH; LEAxB HIGH		3.3	-	-	ns

12. Waveforms

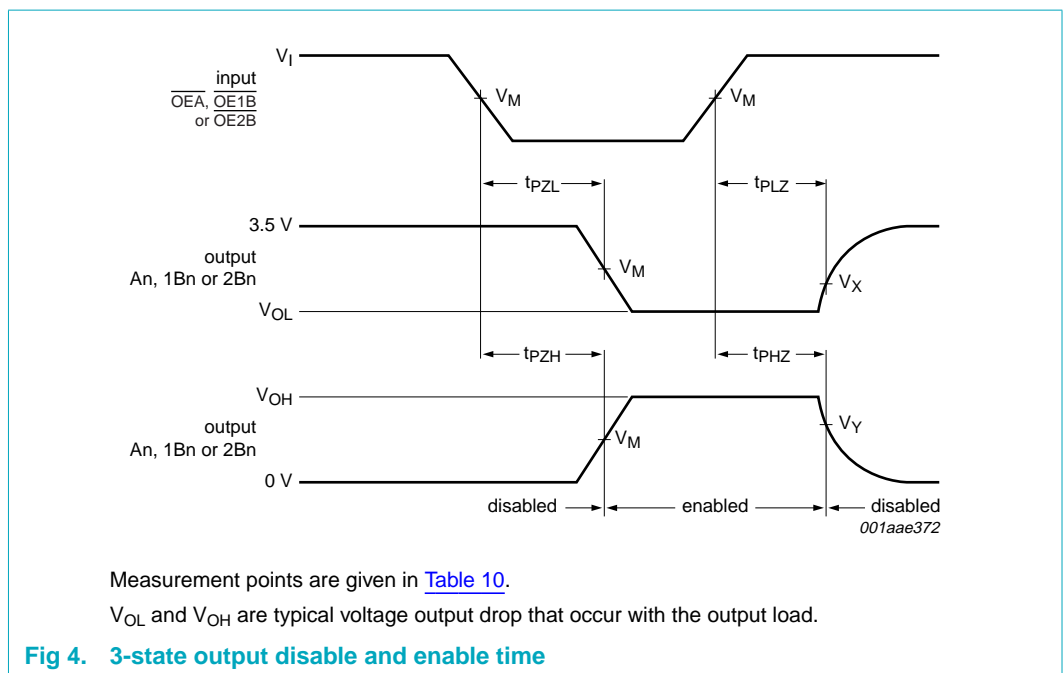
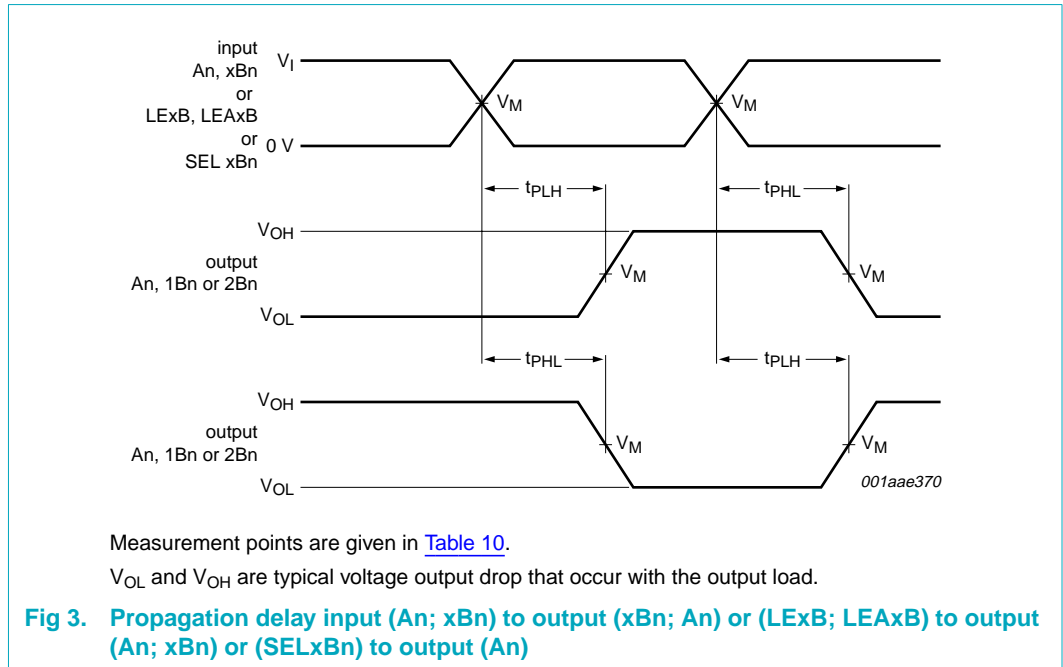
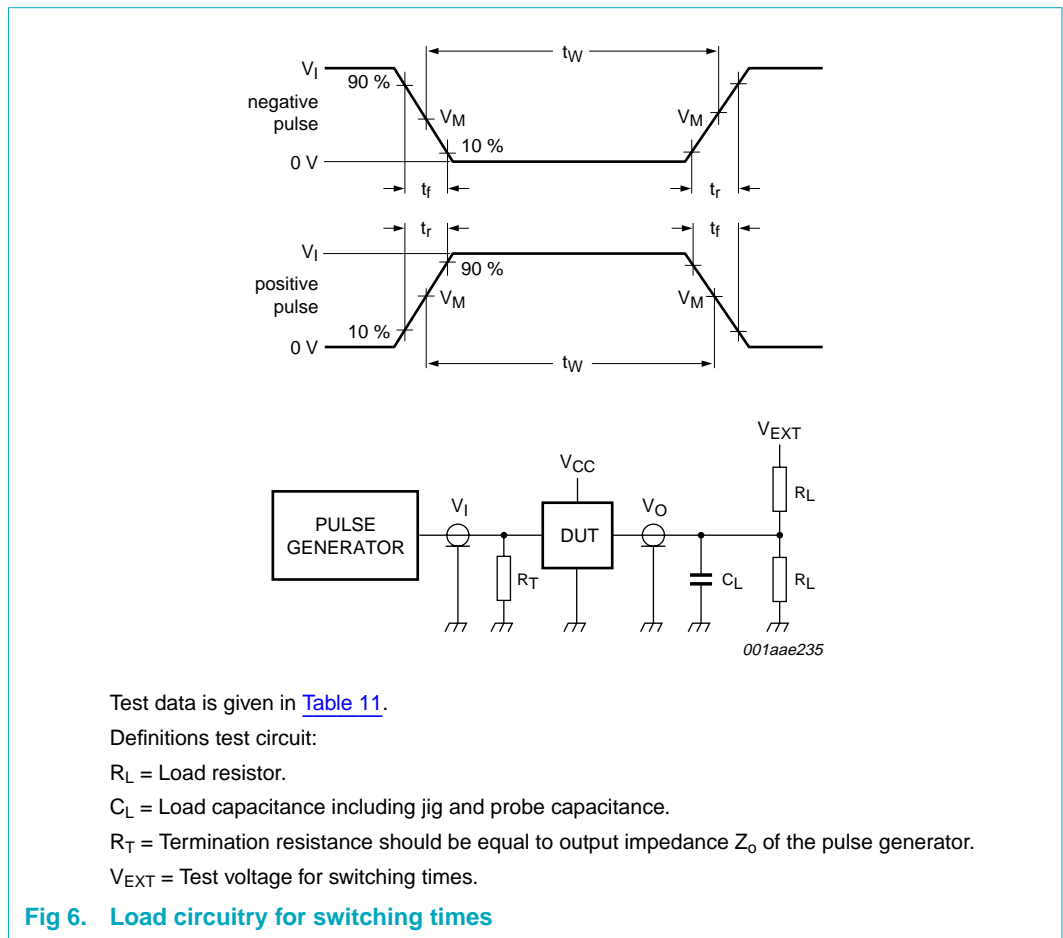
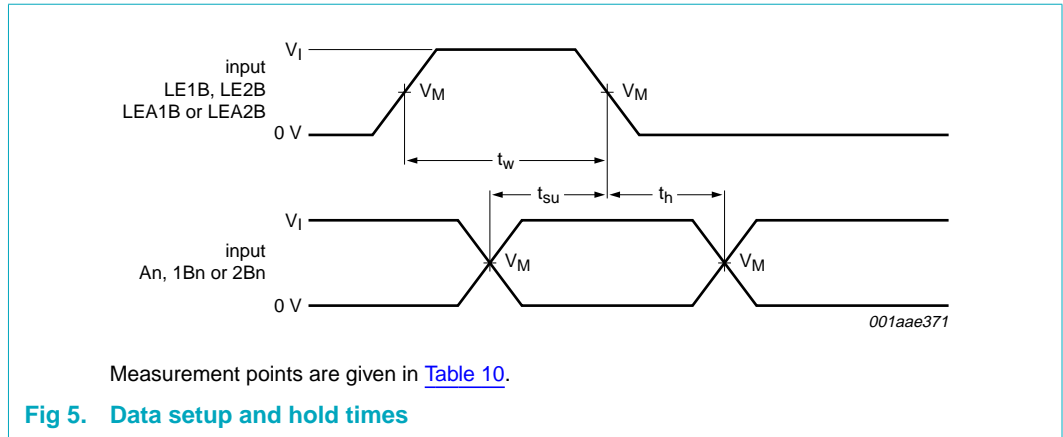


Table 10. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



**Table 11. Test data**

Input			Load		$V_{EXT}$		
$V_I$	$f_i$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$	$t_{PHZ}, t_{PZH}$
3.0 V	$\leq 10$ MHz	$\leq 2.5$ ns	50 pF	500 $\Omega$	7 V	open	GND

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

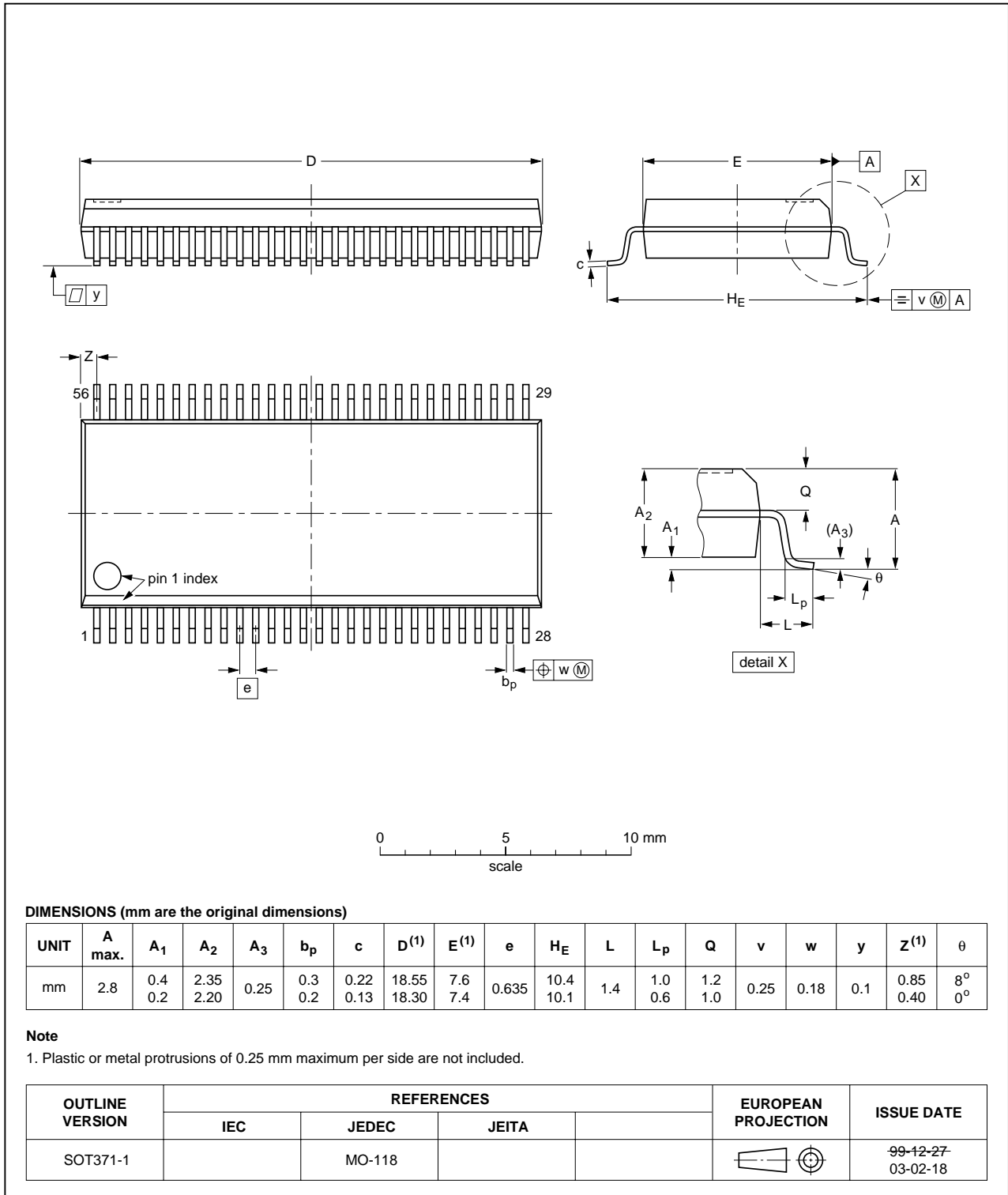


Fig 7. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

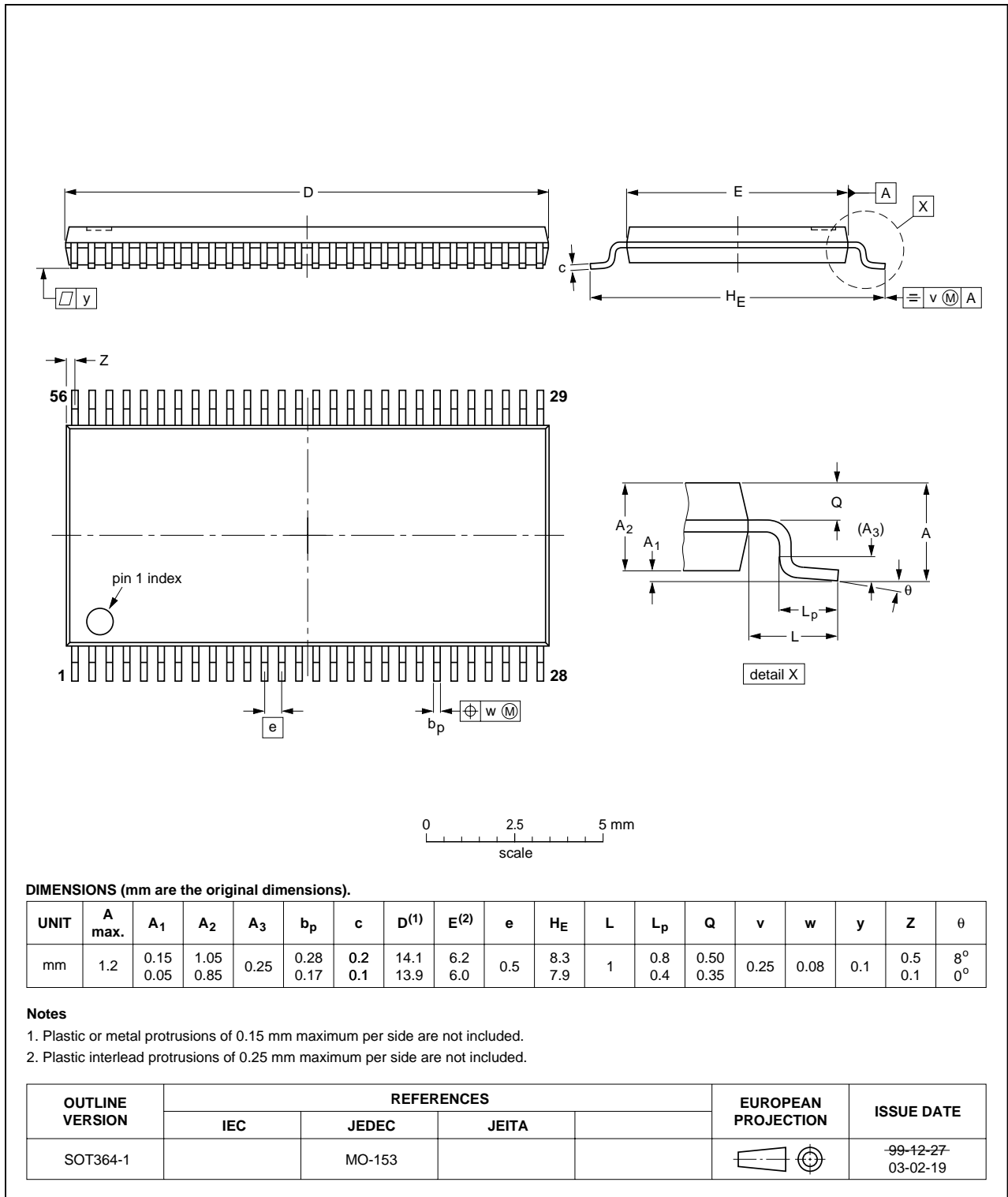


Fig 8. Package outline SOT364-1 (TSSOP56)

## 14. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
DUT	Device Under Test

## 15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVT16260_3	20060320	Product data sheet	-	74ALVT16260_2 (9397 750 03337)
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 2 "Features"</a>: modified 'JEDEC Std JESD-17' into 'JESD78'.</li> <li><a href="#">Table 9 "Dynamic characteristics"</a>: changed various values.</li> </ul>			
74ALVT16260_2 (9397 750 03337)	19980130	Product specification	-	74ALVT16260_1
74ALVT16260_1	-	-	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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