



**THE DATASHEET OF  
74ALVC574PW,118**



# 74ALVC574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 02 — 8 November 2007

Product data sheet

## 1. General description

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The 74ALVC574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock input (CP) and an outputs enable input ( $\overline{OE}$ ) are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW to HIGH CP transition.

When pin  $\overline{OE}$  is LOW, the contents of the eight flip-flops is available at the outputs. When pin  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74ALVC574 is functionally identical to the 74ALVC374, but has a different pin arrangement.

## 2. Features

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- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC574D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC574PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC574BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram

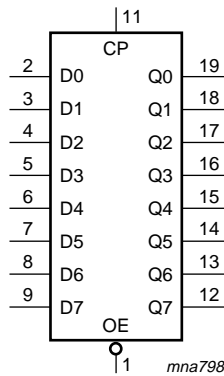


Fig 1. Logic symbol

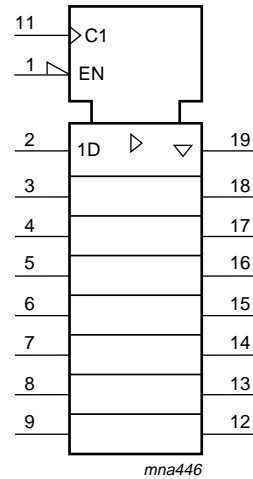


Fig 2. IEC logic symbol

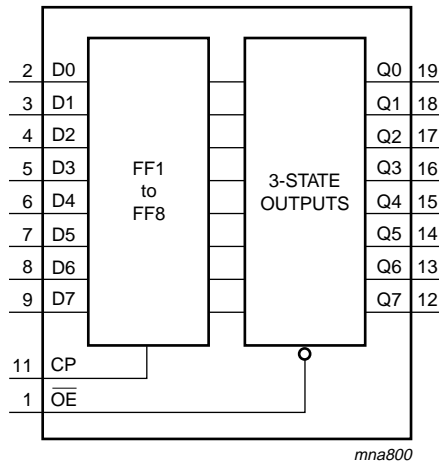


Fig 3. Functional diagram

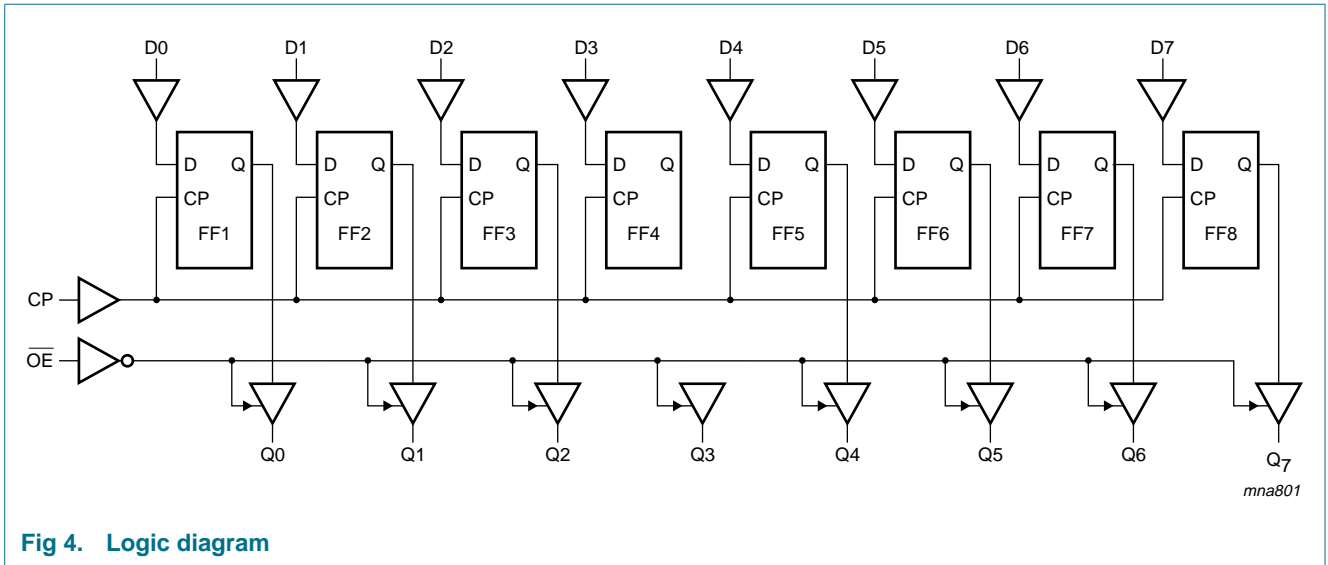
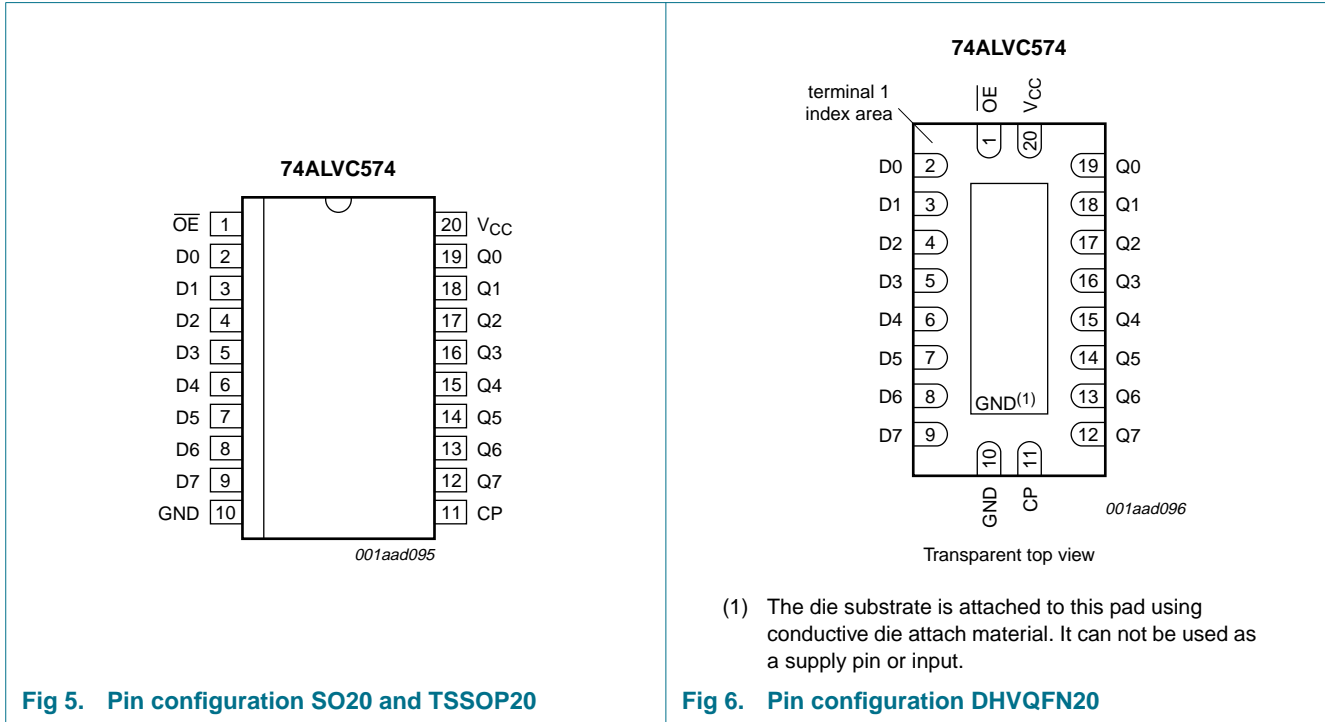


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
CP	11	clock input (LOW to HIGH, edge-triggered)
OE	1	output enable input (active LOW)
Q[0:7]	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
V <sub>CC</sub>	20	supply voltage
GND	10	ground (0 V)

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input			Internal flip-flop	Output Qn
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition  
Z = high-impedance OFF-state  
↑ = LOW to HIGH clock transition

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	output HIGH or LOW state	<sup>[1]</sup> <sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		power-down mode, $V_{CC} = 0$ V	<sup>[2]</sup> -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	<sup>[3]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
[2] When  $V_{CC} = 0$  V (power-down mode), the output voltage can be 3.6 V in normal operation.  
[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	output HIGH or LOW state	0	$V_{CC}$	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.2	2.68	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.30	0.55	V
$I_I$	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	$\pm 0.1$	$\pm 5$	$\mu$ A

**Table 6.** Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 1.65 V to 3.6 V; V <sub>O</sub> = 3.6 V or GND;	-	±0.1	±10	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	-	±0.1	±10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	10	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	µA
C <sub>I</sub>	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 7</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.1	6.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.3	3.9	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.5	3.6	ns
t <sub>en</sub>	enable time	V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	3.6	ns
		$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 8</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.2	6.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	4.5	ns
t <sub>dis</sub>	disable time	V <sub>CC</sub> = 2.7 V	1.0	3.2	4.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.4	4.0	ns
		$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 8</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	3.6	7.0	ns
t <sub>w</sub>	pulse width	V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.3	4.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	2.9	4.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.8	4.4	ns
		clock HIGH or LOW; see <a href="#">Figure 7</a>				
t <sub>w</sub>	pulse width	V <sub>CC</sub> = 1.65 V to 1.95 V	3.8	1.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.3	0.9	-	ns
		V <sub>CC</sub> = 2.7 V	3.3	0.8	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.3	1.2	-	ns

**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.8	–0.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	0.1	-	ns
		V <sub>CC</sub> = 2.7 V	0.8	0.3	-	ns
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.8	–0.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	0.1	-	ns
		V <sub>CC</sub> = 2.7 V	0.8	0.4	-	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	100	200	-	MHz
		V <sub>CC</sub> = 2.7 V	100	200	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	150	300	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[3]</sup>				
		outputs HIGH or LOW state	-	21	-	pF
		outputs 3-state	-	13	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C

- [2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.  
 t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.  
 t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

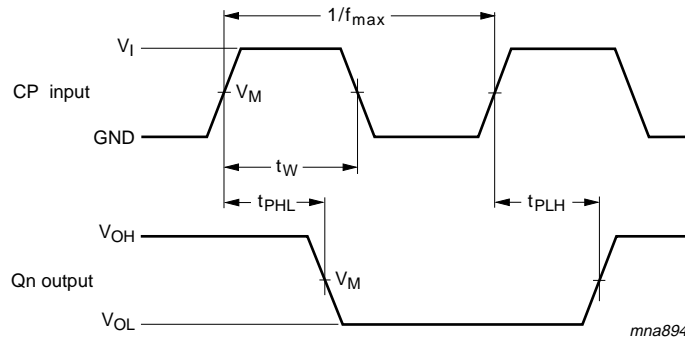
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

11. Waveforms



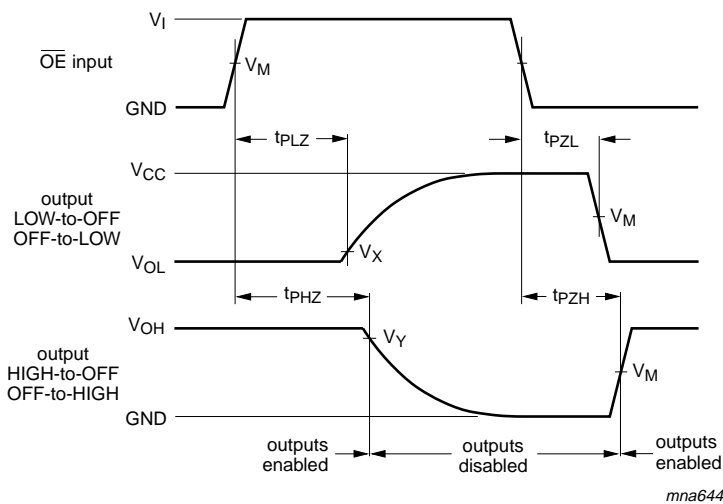
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 7. Clock (CP) to output (Qn) propagation delays, the clock pulse width, and the maximum frequency**

**Table 8. Measurement points**

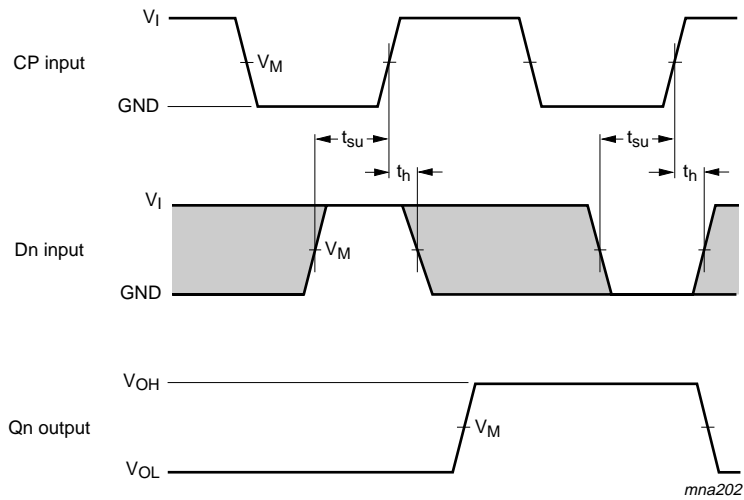
Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 8. Enable and disable times**

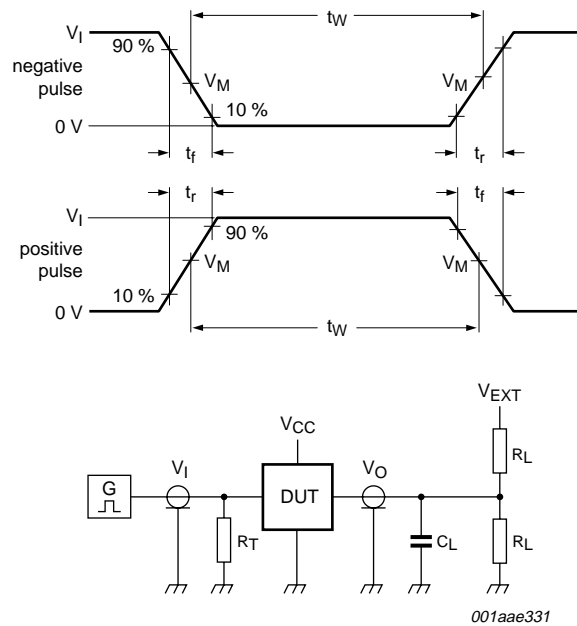


Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

**Fig 9. Data set-up and hold times for the Dn input to the CP input**



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 10. Test circuit for switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	$2V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

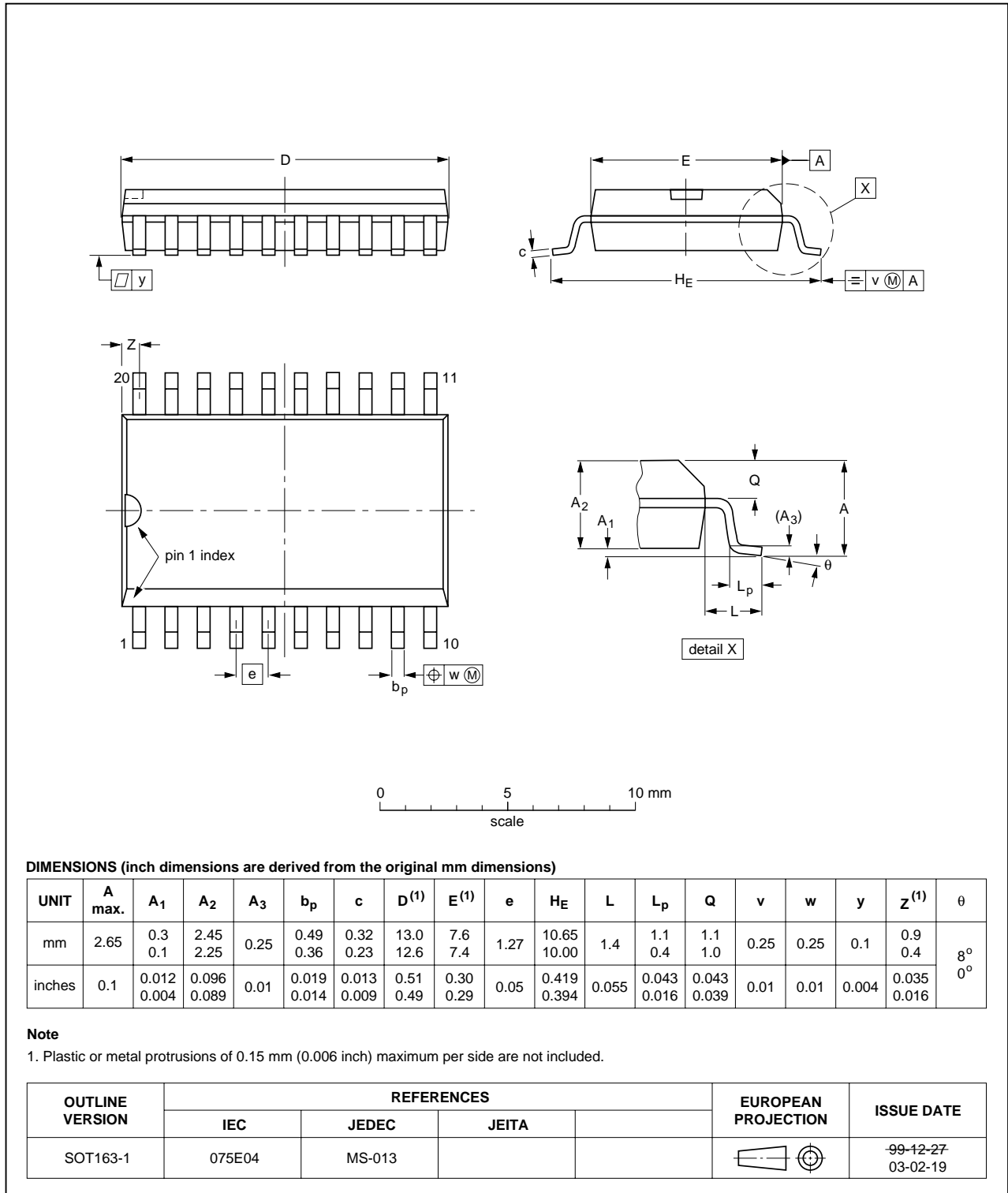


Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

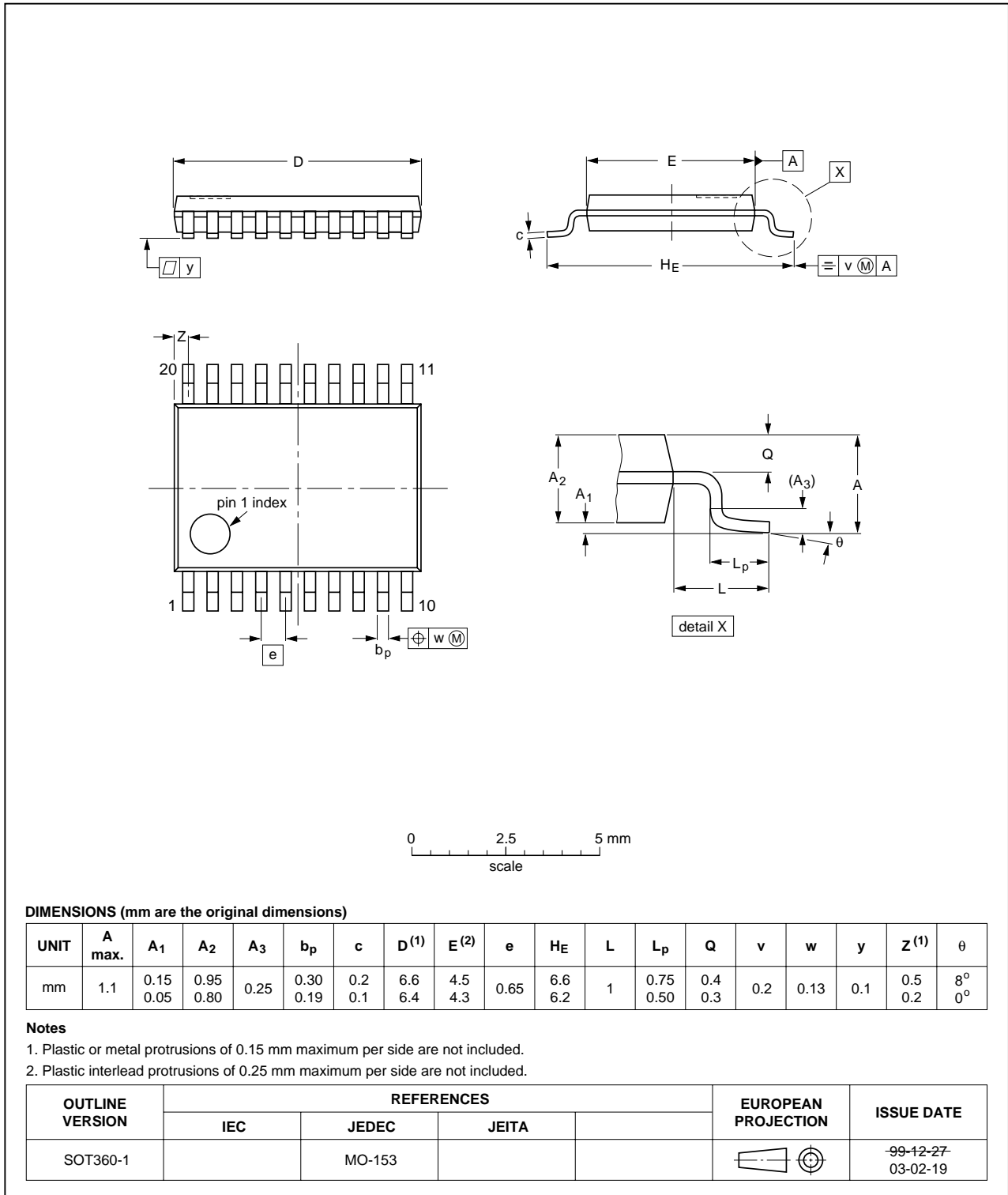


Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

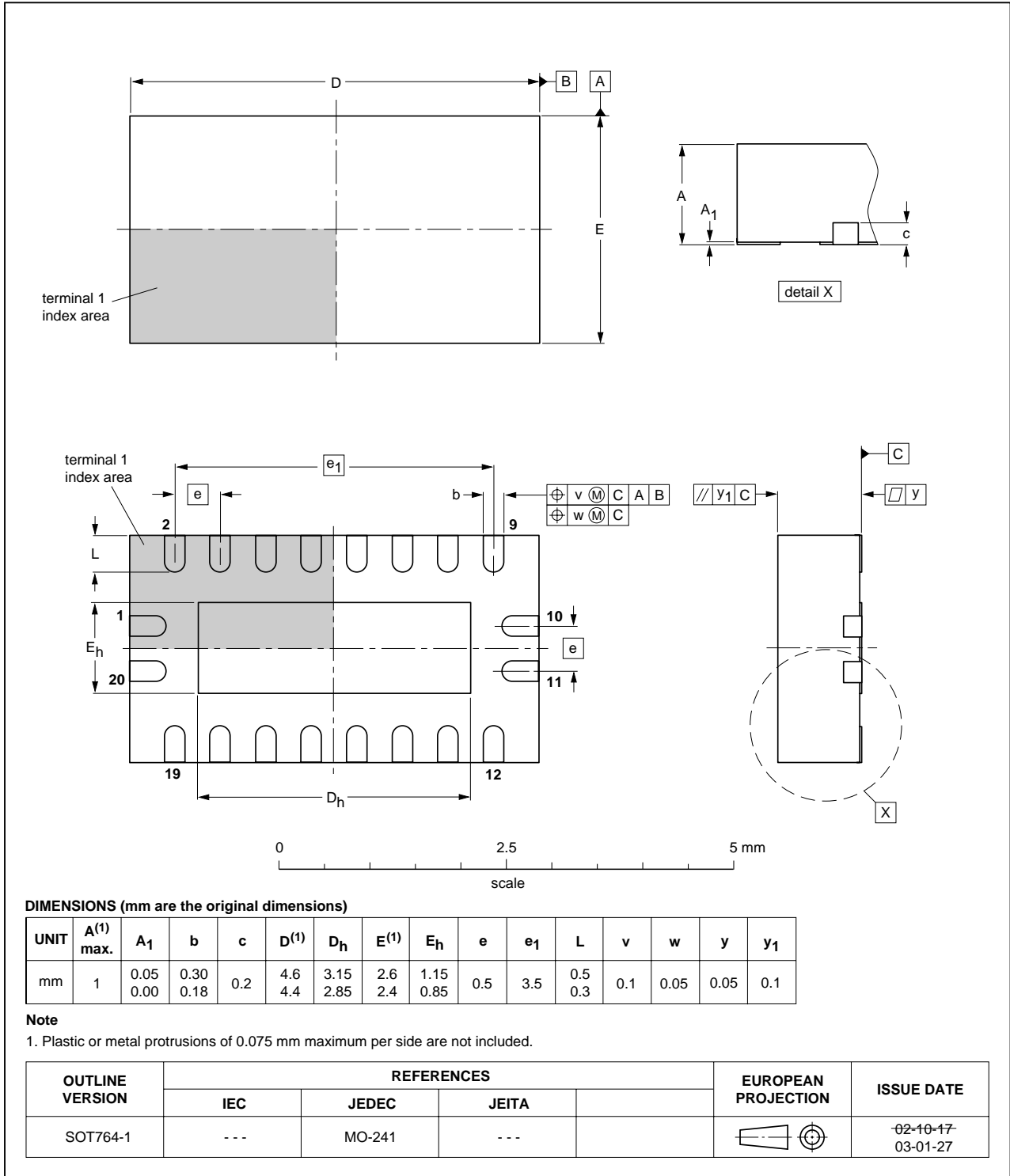


Fig 13. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC574_2	20071108	Product data sheet	-	74ALVC574_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 3</a>: DHVQFN20 package added.</li> <li>• <a href="#">Section 8</a>: derating values added for DHVQFN20 package.</li> <li>• <a href="#">Section 12</a>: outline drawing added for DHVQFN20 package.</li> </ul>			
74ALVC574_1	20020304	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 16. Contact information

For additional information, please visit: <http://www.nexperia.com>

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