



THE DATASHEET OF
SI3911DV-T3-E3



Dual P-Channel 20-V (D-S) MOSFET

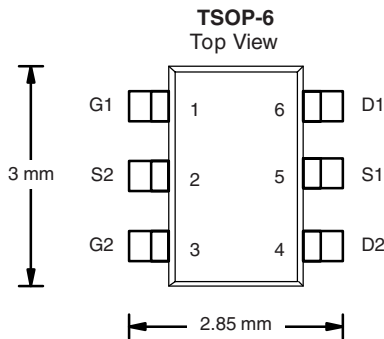
PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
- 20	0.145 at V _{GS} = - 4.5 V	- 2.2
	0.200 at V _{GS} = - 2.5 V	- 1.8
	0.300 at V _{GS} = - 1.8 V	- 1.5

FEATURES

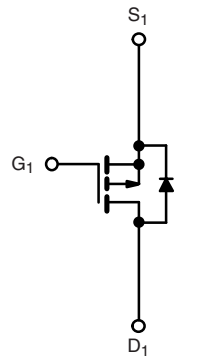
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs: 1.8 V Rated
- Compliant to RoHS Directive 2002/95/EC



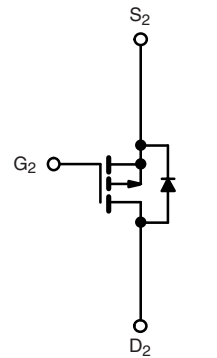
RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si3911DV-T1-E3 (Lead (Pb)-free)
Si3911DV-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	- 20		V	
Gate-Source Voltage	V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	- 2.2	- 1.8	A
		T _A = 70 °C	- 1.8	- 1.5	
Pulsed Drain Current	I _{DM}	± 8		W	
Continuous Diode Current (Diode Conduction) ^a	I _S	- 1.05	- 0.75		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	1.15	0.83	W
		T _A = 70 °C	0.73	0.53	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 s	93	110	°C/W
		Steady State	130	150	
Maximum Junction-to-Foot (Drain)	R _{thJF}	90	90		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

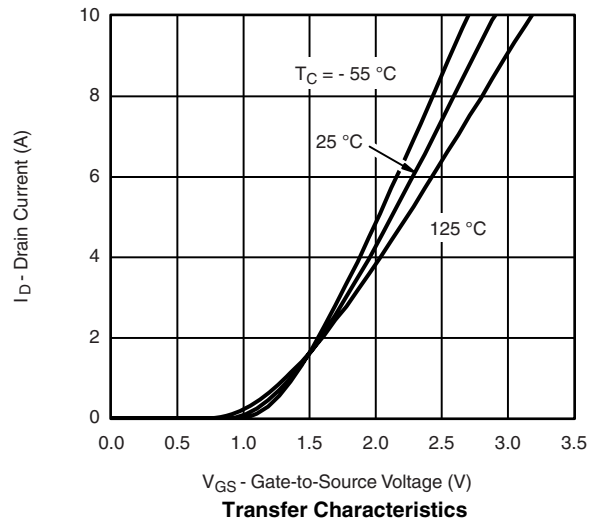
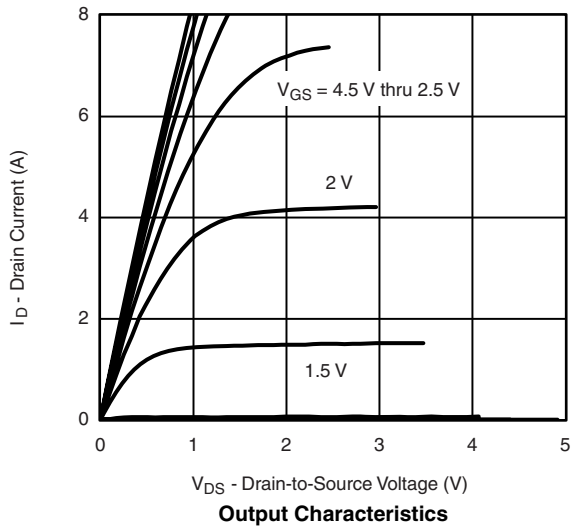
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -2.2\ \text{A}$		0.115	0.145	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -1.8\ \text{A}$		0.163	0.200	
		$V_{GS} = -1.8\ \text{V}, I_D = -1.0\ \text{A}$		0.240	0.300	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\ \text{V}, I_D = -2.2\ \text{A}$		5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.05\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -2.2\ \text{A}$		5	7.5	nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			0.9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\ \text{V}, R_L = 8\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_g = 6\ \Omega$		12	20	ns
Rise Time	t_r			29	50	
Turn-Off Delay Time	$t_{d(off)}$			24	45	
Fall Time	t_f			30	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.05\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		20	40	

Notes:

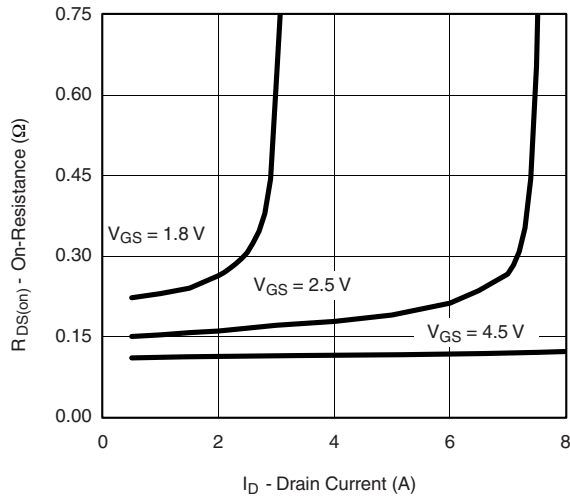
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

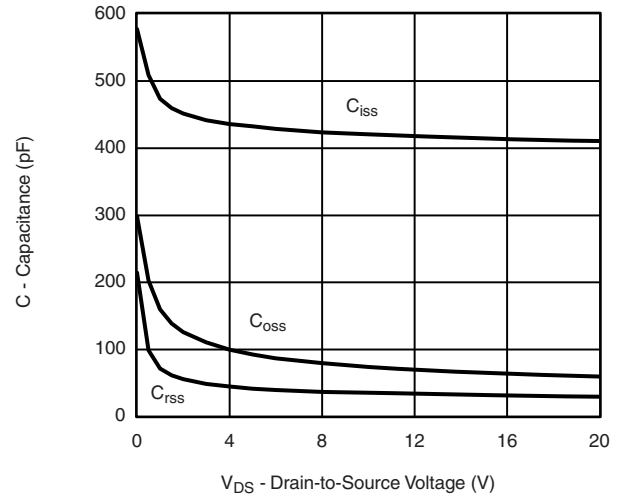
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



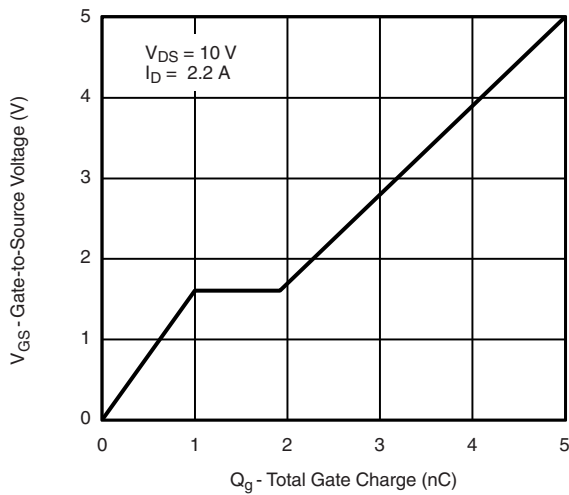
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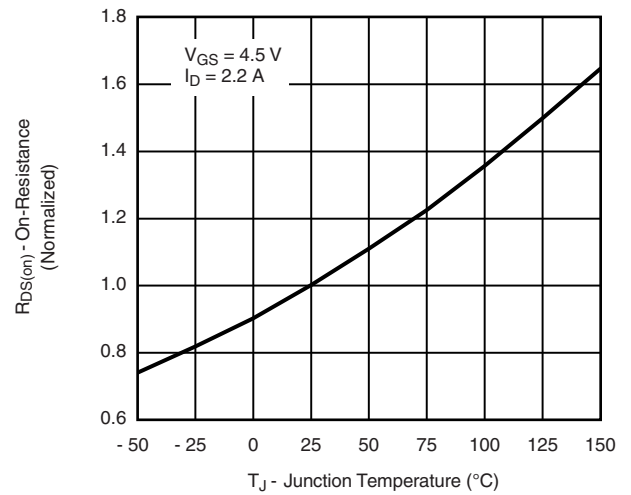
On-Resistance vs. Drain Current



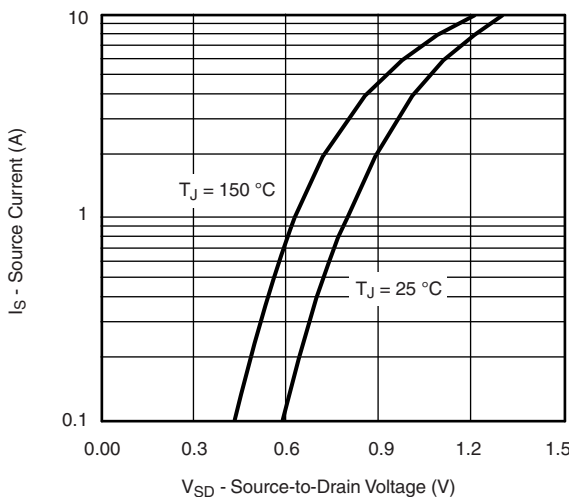
Capacitance



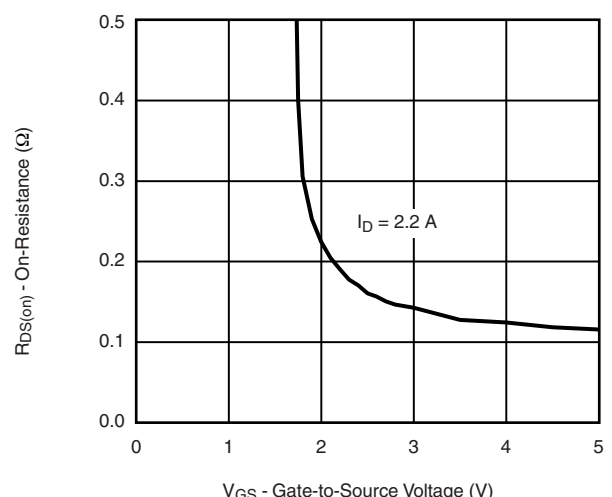
Gate Charge



On-Resistance vs. Junction Temperature

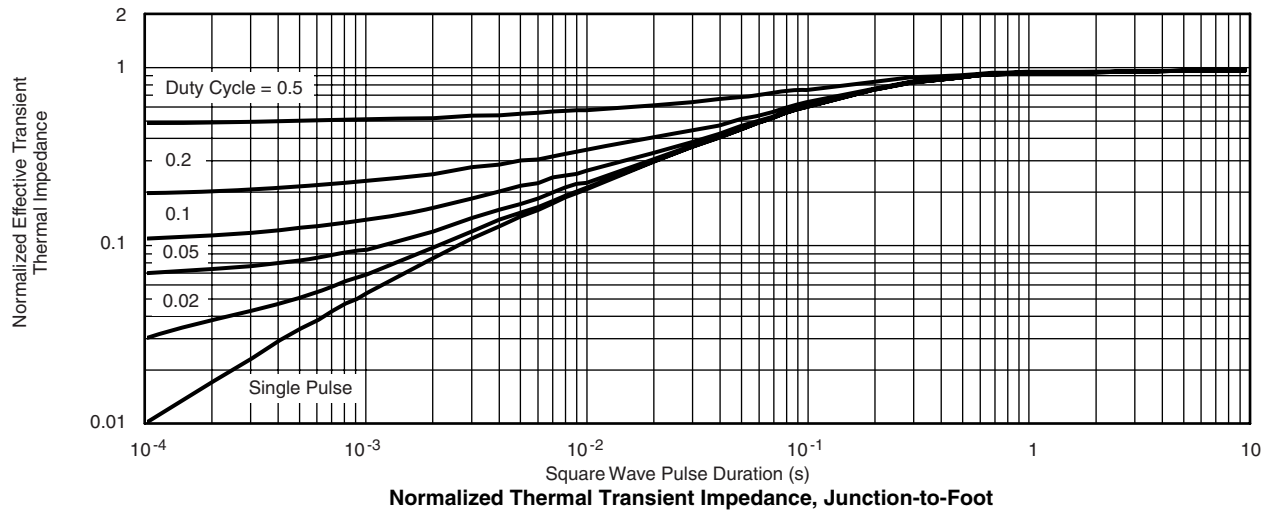
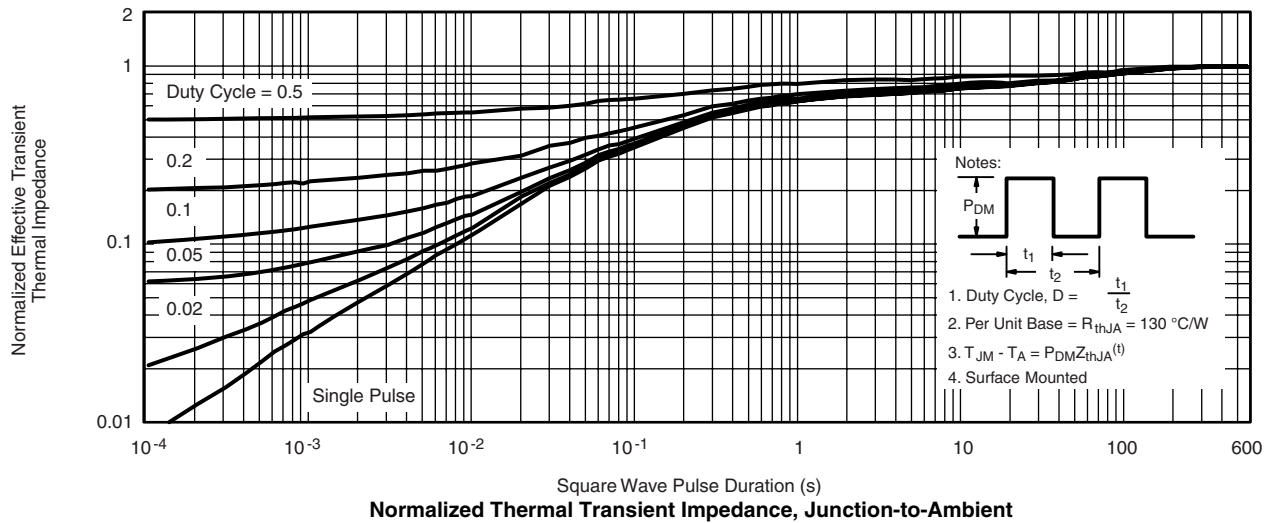
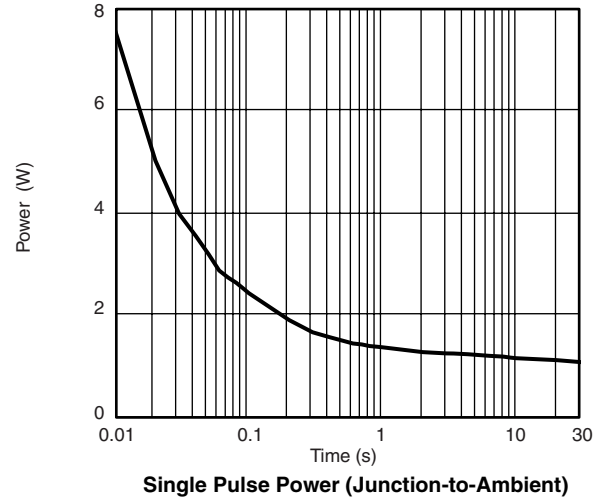
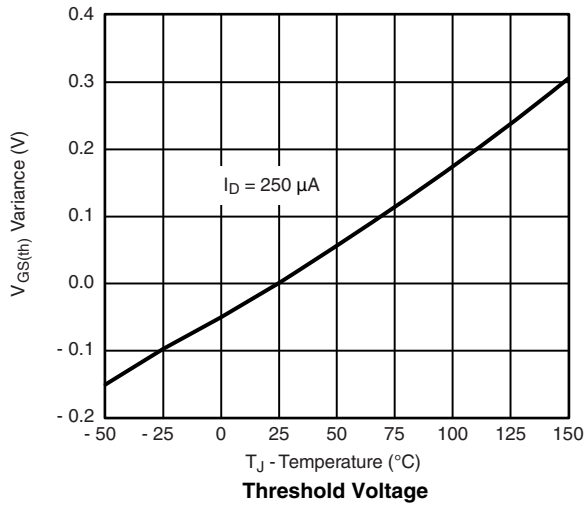


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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