



**THE DATASHEET OF
74AHC125D,118**



74AHC125; 74AHCT125

Quad buffer/line driver; 3-state

Rev. 04 — 11 January 2008

Product data sheet

1. General description

The 74AHC125; 74AHCT125 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74AHC125; 74AHCT125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74AHC125; 74AHCT125 is identical to the 74AHC126; 74AHCT126 but has active LOW enable inputs.

2. Features

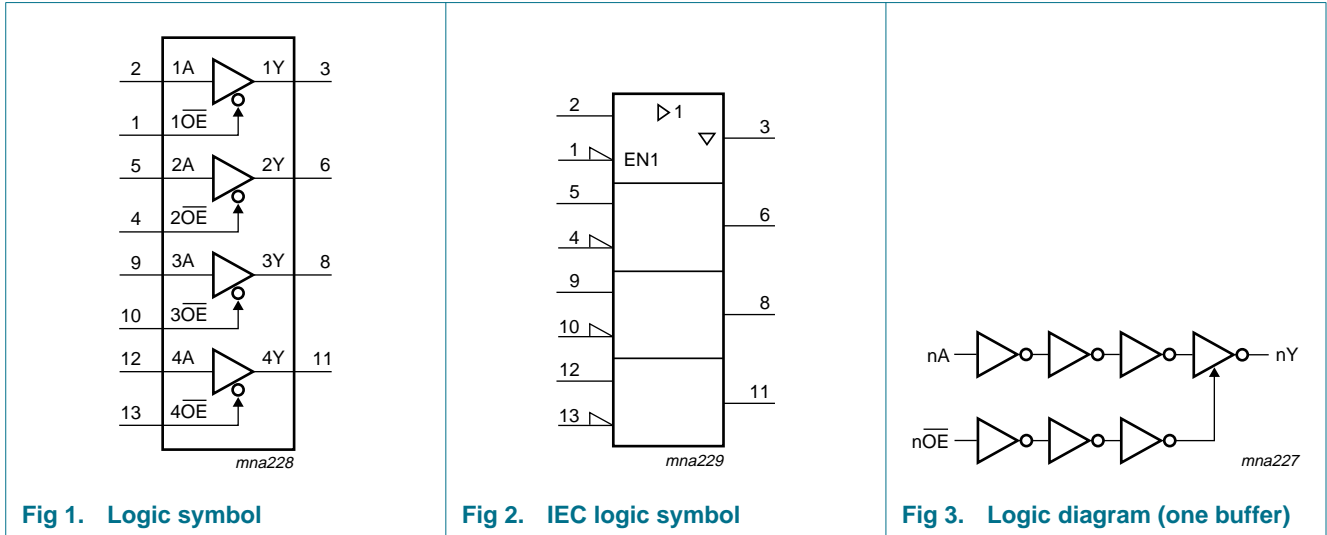
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC125 only: operates with CMOS input levels
- For 74AHCT125 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

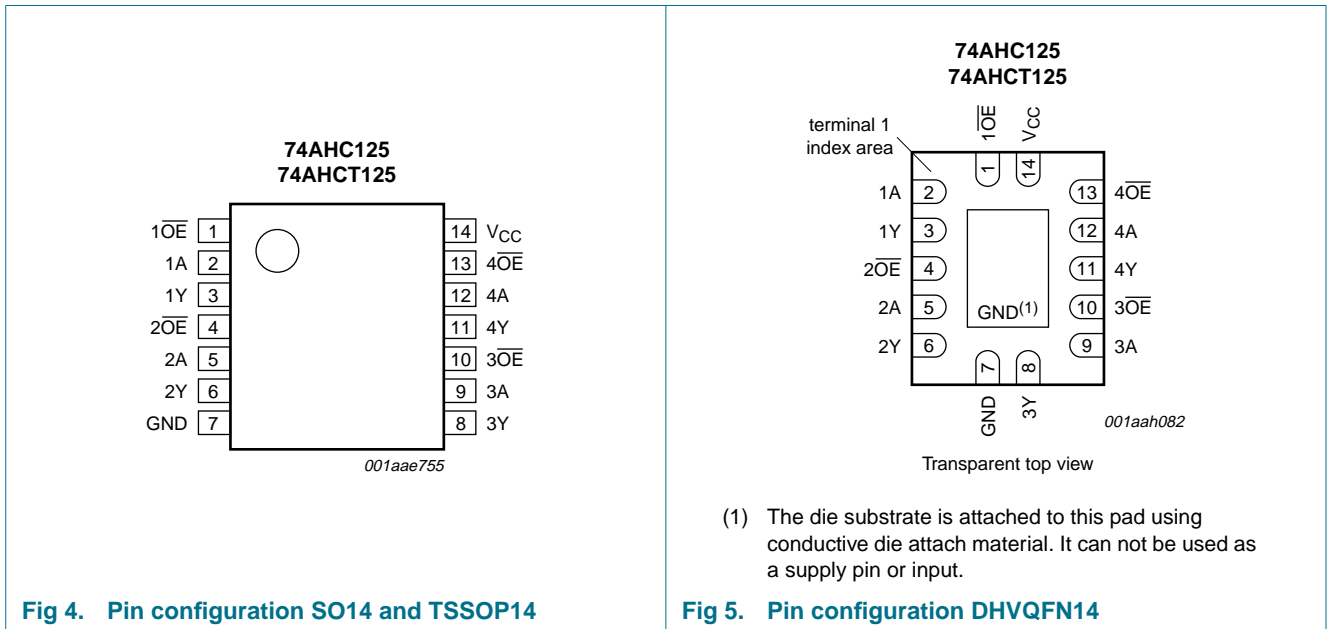
Type number	Package			
	Temperature range	Name	Description	Version
74AHC125D 74AHCT125D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC125PW 74AHCT125PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC125BQ 74AHCT125BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A	2	data input
1Y	3	data output
$2\overline{OE}$	4	output enable input (active LOW)
2A	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
$3\overline{OE}$	10	output enable input (active LOW)
4Y	11	data output
4A	12	data input
$4\overline{OE}$	13	output enable input (active LOW)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Control	Input	Output
nOE	nA	nY
L	L	L
	H	H
H	X	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$			
	SO14 package		[2] -	500	mW
	TSSOP14 package		[3] -	500	mW
	DHVQFN14 package		[4] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC125			74AHCT125			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_{I}	input voltage		0	-	5.5	0	-	5.5	V
V_{O}	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{\text{CC}} = 3.3\text{ V} \pm 0.3\text{ V}$	-	-	100	-	-	-	ns/V
		$V_{\text{CC}} = 5.0\text{ V} \pm 0.5\text{ V}$	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{\text{CC}} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{\text{CC}} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{\text{CC}} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	$V_{\text{CC}} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{\text{CC}} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{\text{CC}} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V

For type 74AHC125

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF
For type 74AHCT125										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; I _O = 0 A V _O = V _{CC} or GND; other pins at V _{CC} or GND	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other pins at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3.0	10	-	10	-	10	pF
C_O	output capacitance		-	4.0	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
 $GND = 0$ V; For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	

For type 74AHC125

t_{pd}	propagation delay	nA to nY; see Figure 6 ^[2] $V_{CC} = 3.0$ V to 3.6 V									
		$C_L = 15$ pF	-	4.4	8.0	1.0	9.5	1.0	11.5	ns	
		$C_L = 50$ pF	-	6.2	11.5	1.0	13.0	1.0	14.5	ns	
		$V_{CC} = 4.5$ V to 5.5 V									
		$C_L = 15$ pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns	
		$C_L = 50$ pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns	
t_{en}	enable time	nOE to nY; see Figure 7 ^[2] $V_{CC} = 3.0$ V to 3.6 V									
		$C_L = 15$ pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns	
		$C_L = 50$ pF	-	6.8	11.5	1.0	13.0	1.0	14.5	ns	
		$V_{CC} = 4.5$ V to 5.5 V									
		$C_L = 15$ pF	-	3.3	5.1	1.0	6.0	1.0	6.5	ns	
		$C_L = 50$ pF	-	4.7	7.1	1.0	8.0	1.0	9.0	ns	
t_{dis}	disable time	nOE to nY; see Figure 7 ^[2] $V_{CC} = 3.0$ V to 3.6 V									
		$C_L = 15$ pF	-	6.7	9.7	1.0	11.5	1.0	12.5	ns	
		$C_L = 50$ pF	-	9.6	13.2	1.0	15.0	1.0	16.5	ns	
		$V_{CC} = 4.5$ V to 5.5 V									
		$C_L = 15$ pF	-	4.8	6.8	1.0	8.0	1.0	8.5	ns	
		$C_L = 50$ pF	-	6.8	8.8	1.0	10.0	1.0	11.0	ns	
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f_i = 1$ MHz; $V_I = GND$ to V_{CC}	^[3]	-	10	-	-	-	-	pF	

Table 7. Dynamic characteristics ...continued
GND = 0 V; For test circuit see Figure 8.

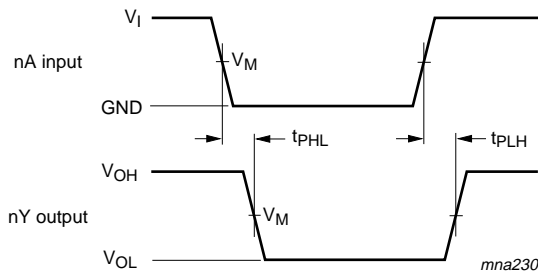
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
For type 74AHCT125										
t _{pd}	propagation delay	nA to nY; see Figure 6 ^[2] V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t _{en}	enable time	nOE to nY; see Figure 7 V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	5.1	1.0	6.0	1.0	6.5	ns
		C _L = 50 pF	-	4.9	7.3	1.0	8.3	1.0	9.5	ns
t _{dis}	disable time	nOE to nY; see Figure 7 ^[2] V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF	-	6.5	8.8	1.0	10.0	1.0	11.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _i = GND to V _{CC} ^[3]	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
 t_{en} is the same as t_{PZL} and t_{PZH}.
 t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz, f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

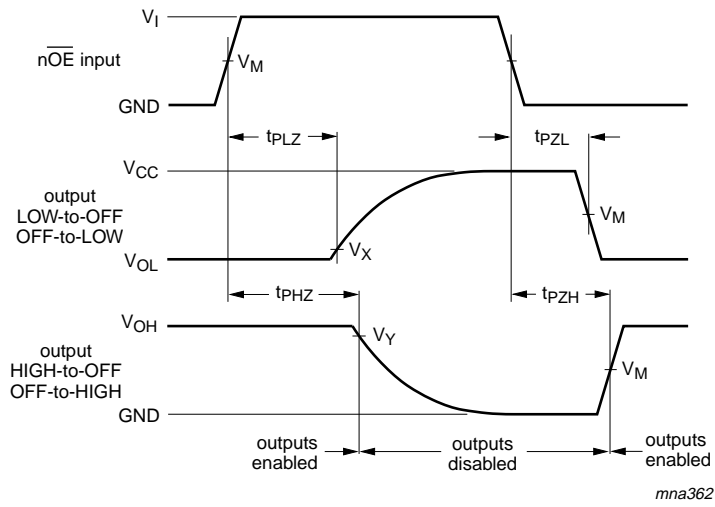
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (nA) to output (nY)



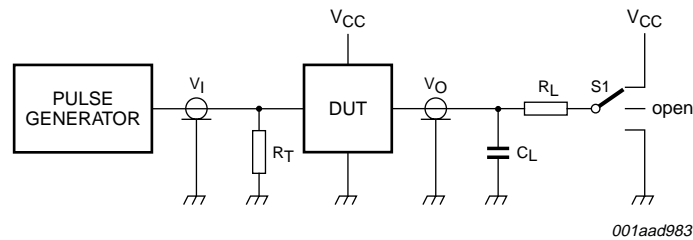
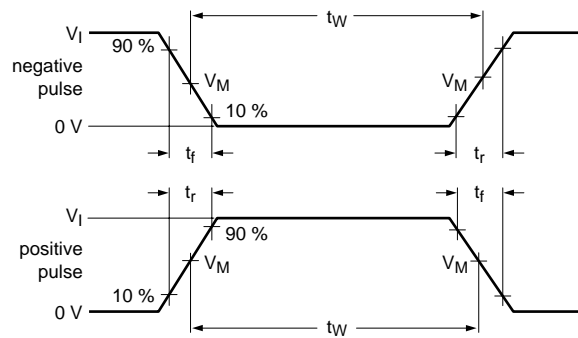
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC125	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$
74AHCT125	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$



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Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuit for switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC125	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT125	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

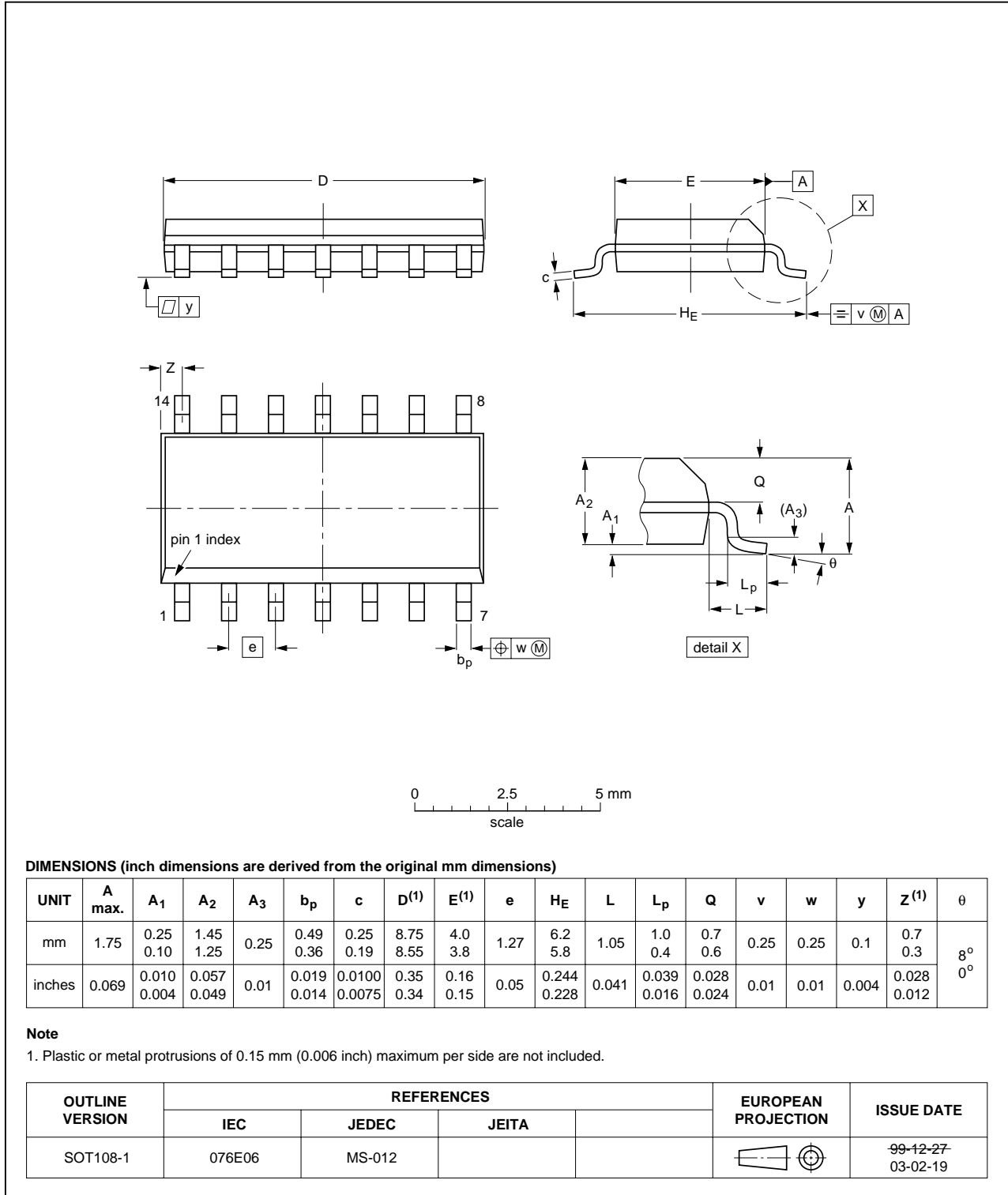


Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

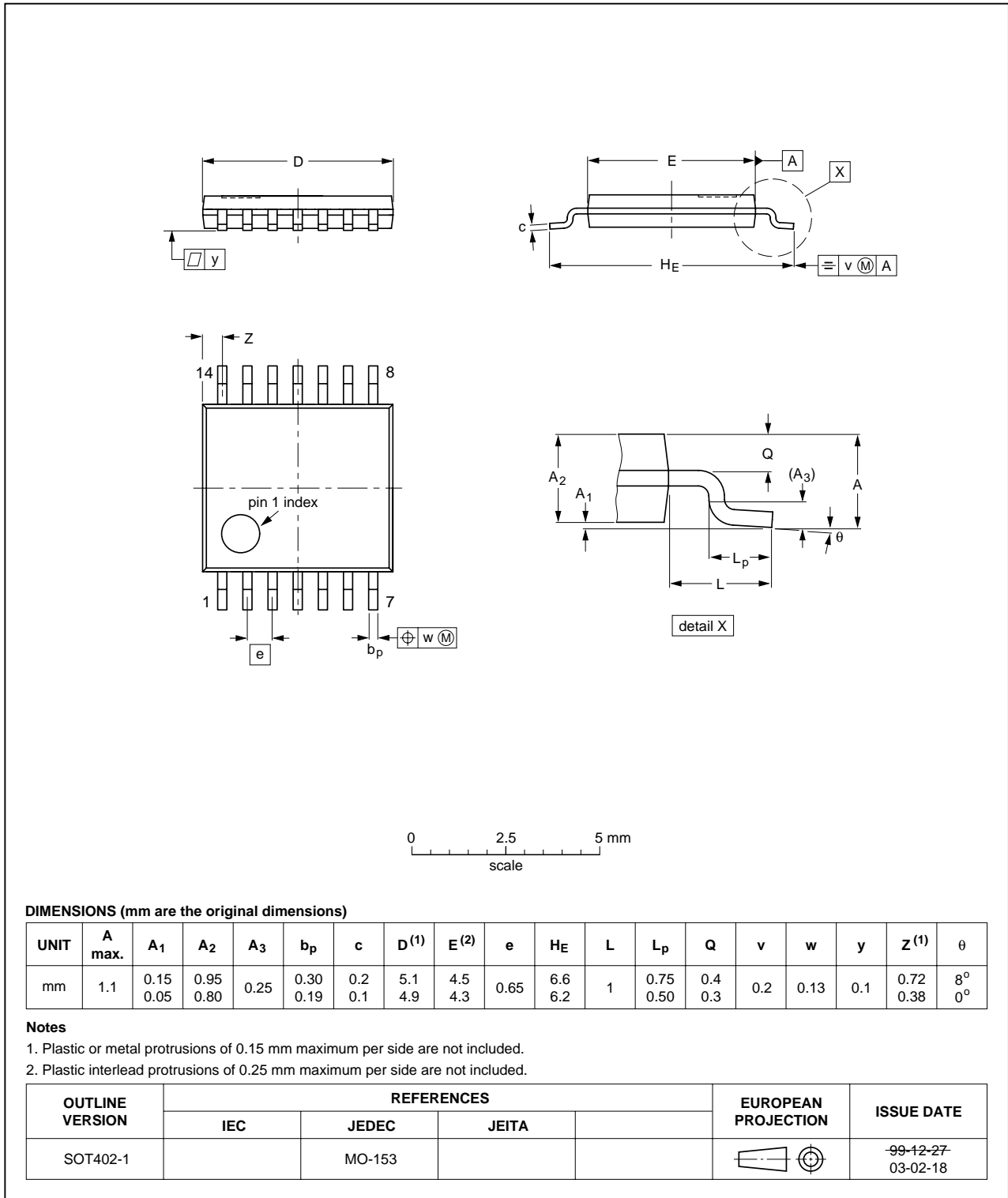


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

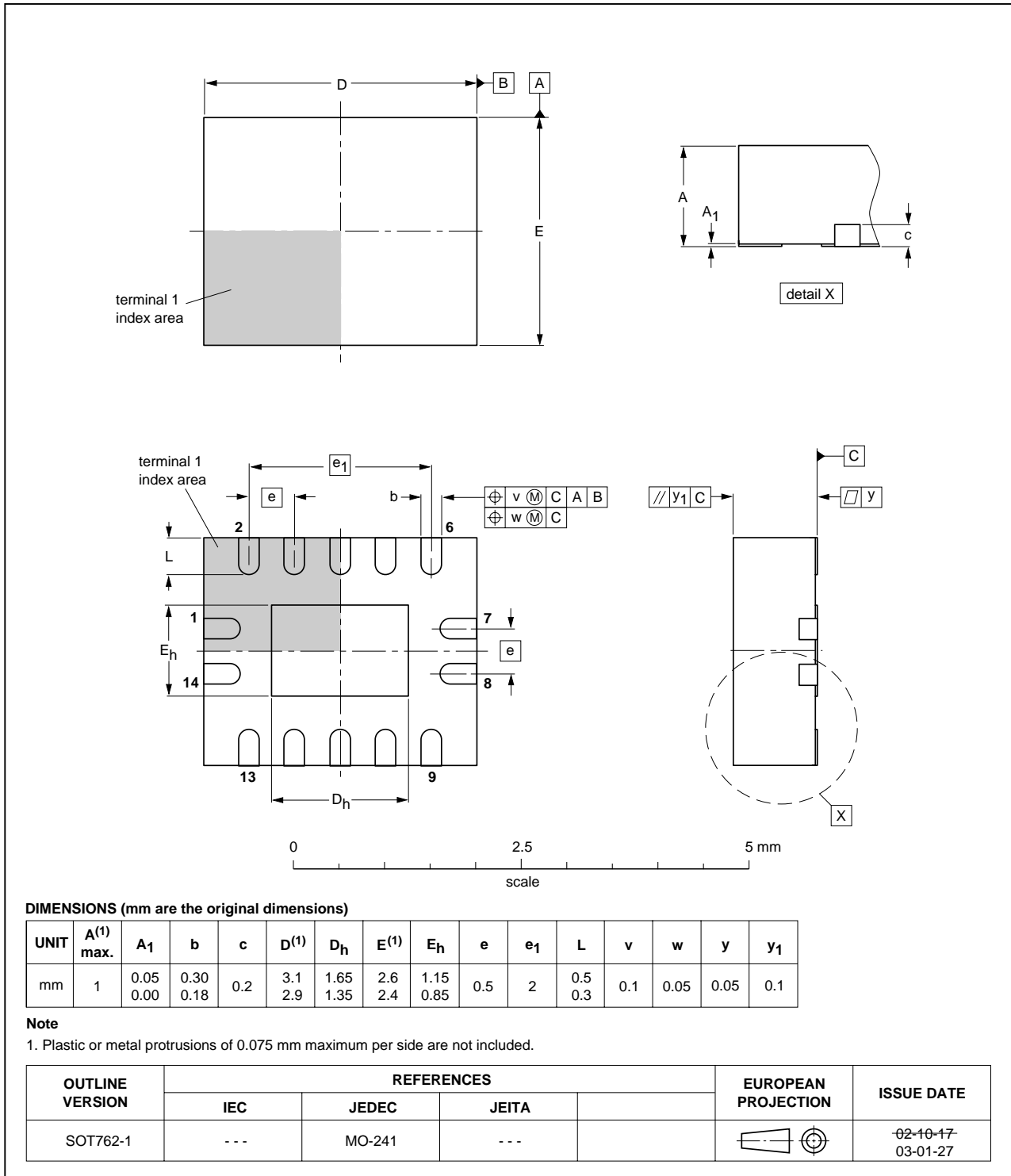


Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT125_4	20080111	Product data sheet	-	74AHC_AHCT125_3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN14 package added. • Section 7: derating values added for DHVQFN14 package. • Section 12: outline drawing added for DHVQFN14 package. 			
74AHC_AHCT125_3	20060324	Product data sheet	-	74AHC_AHCT125_2
74AHC_AHCT125_2	19990927	Product specification	-	74AHC_AHCT125_N_1
74AHC_AHCT125_N_1	19990111	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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