



**THE DATASHEET OF
S5U13706P00C000**



S1D13706 Embedded Memory LCD Controller

The S1D13706 is a color/monochrome LCD graphics controller with an embedded 80K byte SRAM display buffer. While supporting all other panel types, the S1D13706 is the only LCD controller to directly interface to both the Epson D-TFD and the Sharp HR-TFT family of products thus removing the requirement of an external Timing Control IC. This high level of integration provides a low cost, low power, single chip solution to meet the demands of embedded markets such as Mobile Communications devices and Palm-size PCs, where board size and battery life are major concerns.

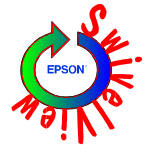
The S1D13706 utilizes a guaranteed low-latency CPU architecture thus providing support for microprocessors without READY/WAIT# handshaking signals. The 32-bit internal data path provides high performance bandwidth into display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13706 also provides support for “Picture-in-Picture Plus” (a variable size Overlay window).

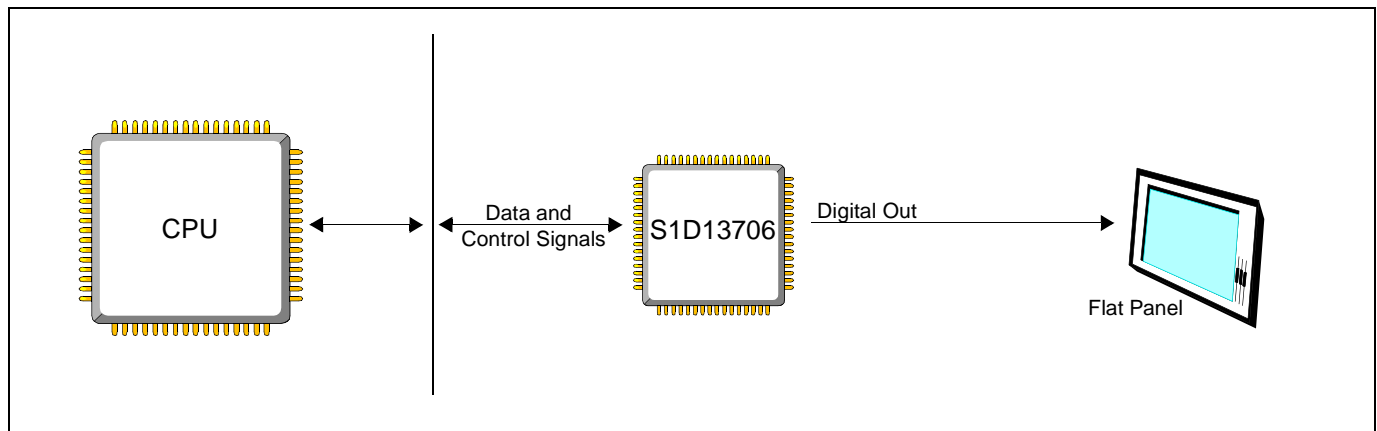
The S1D13706 provides impressive support for Palm OS® handhelds, however its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

■ FEATURES

- Embedded Display Buffer.
- Low Operating Voltage.
- Low-latency CPU interface.
- Direct support for the multiple CPU types.
- Programmable Resolutions and Color depths.
- STN LCD support.
- Active Matrix LCD support.
- Reflective Active Matrix support.
- SwivelView™ (90, 180, 270° hardware rotation of displayed image).
- “Picture-in-Picture Plus”.
- Software Initiated Power Save Mode.
- Hardware or Software Video Invert.
- 100-pin TQFP15 package.
- 104-pin CFLGA package.



■ SYSTEM BLOCK DIAGRAM



S1D13706

DESCRIPTION

Memory Interface

- Embedded 80K byte SRAM display buffer.

CPU Interface

- 'Fixed' low-latency CPU access times.
- Direct support for:
 - Hitachi SH-4 / SH-3.
 - Motorola M68xxx (REDCAP2, DragonBall, ColdFire).
 - MPU bus interface with programmable READY.

Display Support

- 4/8-bit monochrome LCD interface.
- 4/8/16-bit color STN LCD interface.
- Single-panel, single-drive passive displays.
- 9/12/18-bit Active matrix TFT interface.
- 'Direct' support for Epson D-TFD and Sharp HR-TFT (external timing control IC not required).
- Typical resolutions supported:
 - 320x240@8bpp
 - 160x160 @16bpp
 - 160x240 @16bpp

Clock Source

- Two clock inputs (single clock possible).
- Clock source can be internally divided down for a higher frequency clock input.

Display Modes

- 1/2/4/8/16 bit-per-pixel (bpp) support.
- Up to 64 gray shades using FRM and dithering on monochrome passive LCD panels.
- Up to 64K colors on passive STN panels.
- Up to 64K colors on active matrix panels.
- SwivelView: direct hardware rotation of display image by 90°, 180°, 270°.
- "Picture-in-Picture Plus": displays a variable size window overlaid over background image.
- Double Buffering/multi-pages: provides smooth animation and instantaneous screen update.

Power Down Modes

- Software Initiated Power Save Mode.

Operating Voltage

- CORE_{VDD} 1.8 to 2.2 volts and 3.0 to 3.6 volts.
- HIO_{VDD} 1.8 to 2.2 volts and 3.0 to 3.6 volts.
- NIO_{VDD} 3.0 to 3.6 volts.

Package

- 100-pin TQFP15.
- 104-pin CFLGA.

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13706 Technical Manual
- S5U13706 Evaluation Boards
- CPU Independent Software Utilities
- Palm OS[®] Hardware Abstraction Layer
- Windows[®] CE Display Driver
- VXWorks[®] Tornado[™] Display Driver

Japan

Seiko Epson Corporation
IC International Sales Group
421-8, Hino, Hino-shi
Tokyo 191-8501, Japan
Tel: +81-42-587-5814
Fax: +81-42-587-5117

North America

Epson Electronics America, Inc.
2580 Orchard Parkway
San Jose, CA 95131, USA
Tel: +1-800-228-3964
Fax: +1-408-922-0238

China

Epson (China) Co., Ltd.
7F, Jinbao Bldg.
No. 89 Jinbao St.
Dongcheng District
Beijing 100005, China
Tel: +86-10-6410-6555
Fax: +86-10-6410-7320

Taiwan

Epson Taiwan Technology & Trading Ltd.
14F, No. 7
Song Ren Road
Taipei 110, Taiwan
Tel: +886-2-8786-6688
Fax: +886-2-8786-6660

Hong Kong

Epson Hong Kong Ltd.
20/F, Harbour Centre
25 Harbour Road
Wanchai, Hong Kong
Tel: +852-2585-4600
Fax: +852-2827-4346

Europe

Epson Europe Electronics GmbH
Riesstrasse 15
80992 Munich, Germany
Tel: +49-89-14005-0
Fax: +49-89-14005-110

Singapore

Epson Singapore Pte., Ltd.
1 HarbourFront Place
#03-02 HarbourFront Tower One
Singapore 098633
Tel: +65-6586-5500
Fax: +65-6271-3182

Korea

Seiko Epson Corp.
Korea Office
50F, LKI 63 Bldg.
60 Yoido-dong, Youngdeungpo-Ku,
Seoul, 150-763, Korea
Tel: +82-2-784-6027
Fax: +82-2-767-3677

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VDC

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