



**THE DATASHEET OF
74ACT175MTCX**



74AC175, 74ACT175 Quad D-Type Flip-Flop

Features

- I_{CC} reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24mA
- ACT175 has TTL-compatible inputs

General Description

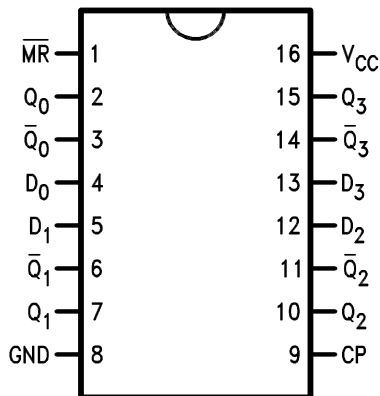
The AC/ACT175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D-type inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D-type inputs, when LOW.

Ordering Information

Order Number	Package Number	Package Description
74AC175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC175PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

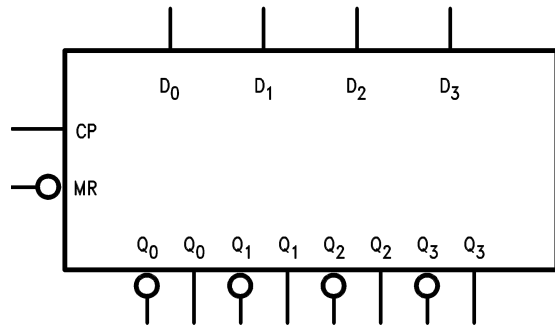
Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₃	Data Inputs
CP	Clock Pulse Input
\overline{MR}	Master Reset Input
Q ₀ -Q ₃	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Complement Outputs

Logic Symbol



Functional Description

The AC/ACT175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The AC/ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs @ t_n , $\overline{MR} = H$	Outputs @ t_{n+1}	
D_n	Q_n	\bar{Q}_n
L	L	H
H	H	L

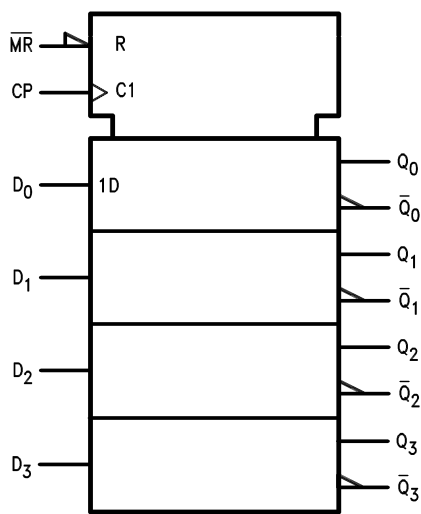
H = HIGH Voltage Level

L = LOW Voltage Level

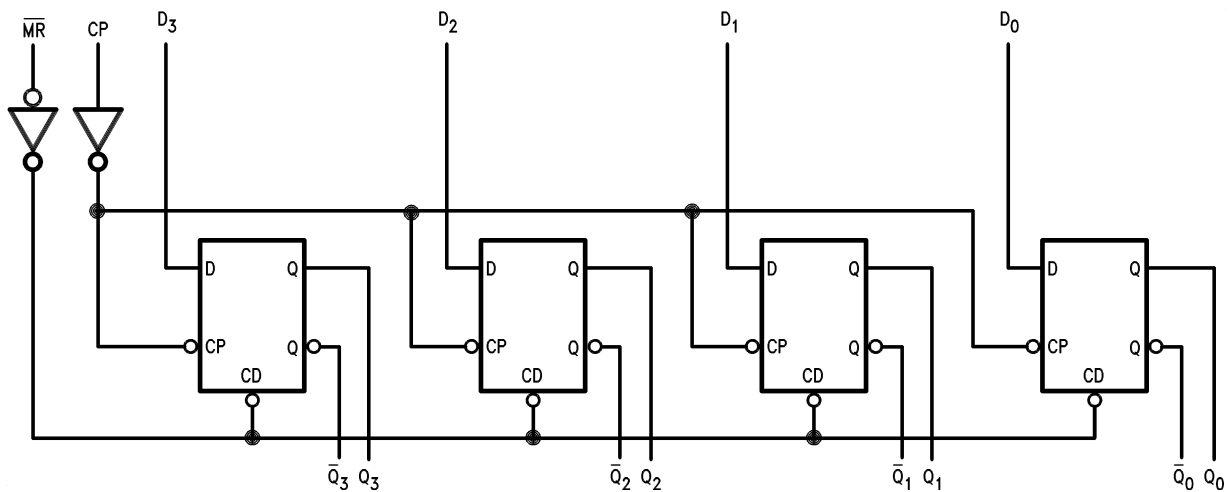
t_n = Bit Time before Clock Pulse

t_{n+1} = Bit Time after Clock Pulse

IEEE/IEC



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V _{IN} = V _{IL} or V _{IH} : I _{OH} = -12mA			2.56	2.46		
		4.5	I _{OH} = -24mA			3.86	3.76		
		5.5	I _{OH} = -24mA ⁽¹⁾			4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50μA	0.002	0.1	0.1		V	
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V _{IN} = V _{IL} or V _{IH} : I _{OL} = 12mA			0.36	0.44		
		4.5	I _{OL} = 24mA			0.36	0.44		
		5.5	I _{OL} = 24mA ⁽¹⁾			0.36	0.44		
I _{IN} ⁽³⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA	
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA	
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA	
I _{CC} ⁽³⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA	

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0		V	
		5.5		1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8		V	
		5.5		1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50μA	4.49	4.4	4.4		V	
		5.5		5.49	5.4	5.4			
		4.5	V _{IN} = V _{IL} or V _{IH} : I _{OH} = -24mA			3.86	3.76		
		5.5	I _{OH} = -24mA ⁽⁴⁾			4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V	
		5.5		0.001	0.1	0.1			
		4.5	V _{IN} = V _{IL} or V _{IH} : I _{OL} = 24mA			0.36	0.44		
		5.5	I _{OL} = 24mA ⁽⁴⁾			0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA	
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V	0.6		1.5		mA	
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			75		mA	
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA	
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA	

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) ⁽⁶⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3	149	214		139		MHz
		5.0	187	244		187		
t_{PLH}	Propagation Delay, CP to Q_n or \overline{Q}_n	3.3	2.0	9.5	12.0	2.0	13.5	ns
		5.0	1.5	7.0	9.0	1.0	9.5	
t_{PHL}	Propagation Delay, CP to Q_n or \overline{Q}_n	3.3	2.5	8.5	13.0	2.0	14.5	ns
		5.0	1.5	6.0	9.5	1.5	10.5	
t_{PLH}	Propagation Delay, $\overline{\text{MR}}$ to Q_n	3.3	3.0	7.5	12.5	2.5	13.5	ns
		5.0	2.0	5.5	9.0	1.5	10.0	
t_{PHL}	Propagation Delay, $\overline{\text{MR}}$ to Q_n	3.3	3.0	8.5	11.0	2.5	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.0	

Note:

6. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V) ⁽⁷⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW, D_n to CP	3.3	2.0	4.5	4.5		ns
		5.0	1.0	3.0	3.0		
t_H	Hold Time, HIGH or LOW, D_n to CP	3.3	1.0	1.0	1.0		ns
		5.0	1.0	1.0	1.0		
t_W	CP Pulse Width, HIGH or LOW	3.3	2.5	4.5	4.5		ns
		5.0	2.0	3.5	3.5		
t_W	$\overline{\text{MR}}$ Pulse Width, LOW	3.3	2.5	4.5	5.0		ns
		5.0	2.0	3.5	3.5		
t_{REC}	Recovery Time, $\overline{\text{MR}}$ to CP	3.3	-2.0	0	0		ns
		5.0	-1.0	0	0		

Note:

7. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) ⁽⁸⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency	5.0	175	236		145		MHz
t _{PLH}	Propagation Delay, CP to Q _n or \overline{Q}_n	5.0	2.0	6.0	10.0	1.5	11.0	ns
t _{PHL}	Propagation Delay, CP to Q _n or \overline{Q}_n	5.0	2.0	7.0	11.0	1.5	12.0	ns
t _{PLH}	Propagation Delay, \overline{MR} to \overline{Q}_n	5.0	2.0	6.0	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay, \overline{MR} to Q _n	5.0	2.0	5.5	9.5	1.5	10.5	ns

Note:

8. Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for ACT

Symbol	Parameter	V _{CC} (V) ⁽⁹⁾	T _A = +25°C, C _L = 50pF		T _A = -40°C to +85°C, C _L = 50pF		Units
			Typ.	Guaranteed Minimum			
t _S (H)	Setup Time, D _n to CP	5.0	3.0	2.0	2.0		ns
t _S (L)			3.0	2.5	2.5		
t _H	Hold Time, HIGH or LOW, D _n to CP	5.0	0	1.0	1.0		ns
t _W	CP Pulse Width, HIGH or LOW	5.0	4.0	3.0	3.5		ns
t _W	\overline{MR} Pulse Width, LOW	5.0	4.0	3.0	4.0		ns
t _{rec}	Recovery Time, \overline{MR} to CP	5.0	0	0	0		ns

Note:

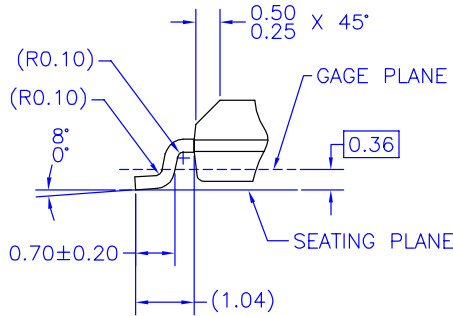
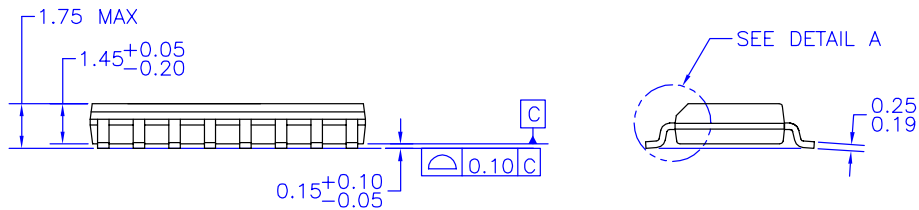
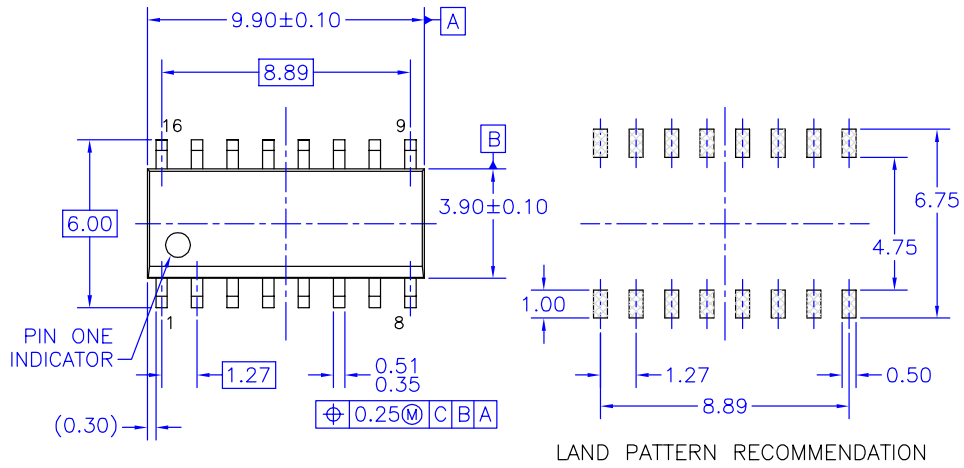
9. Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	45.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

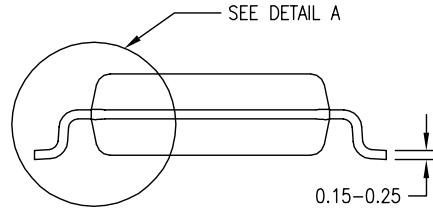
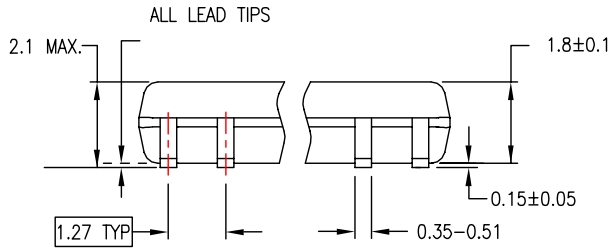
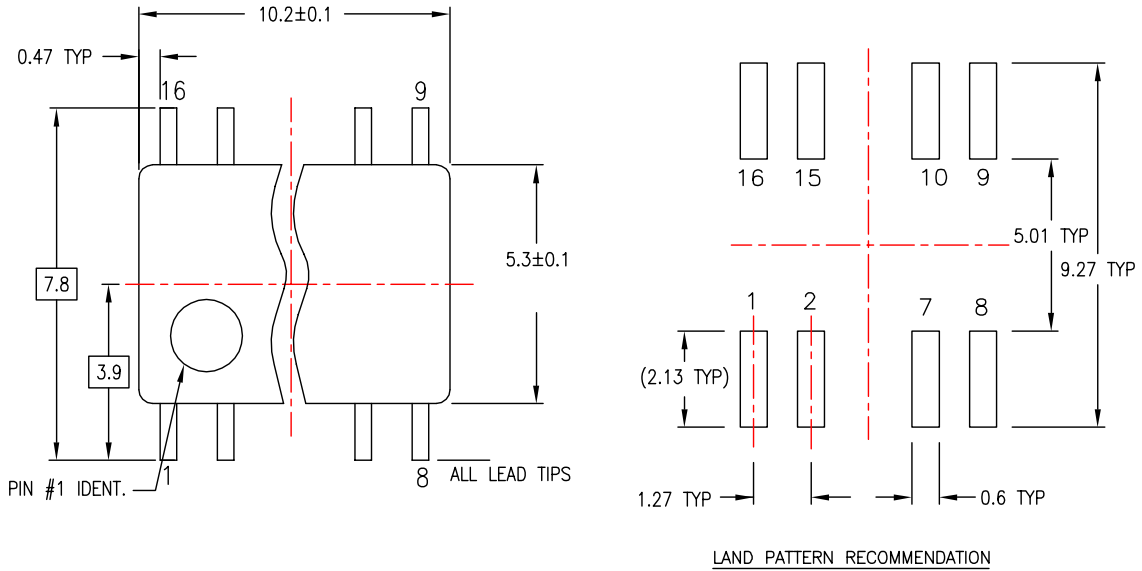
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:
200 MICRONS / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

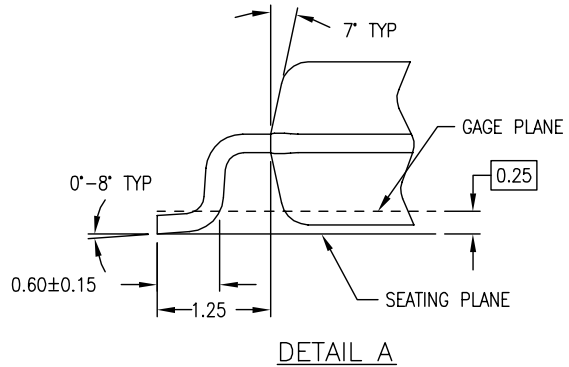
Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

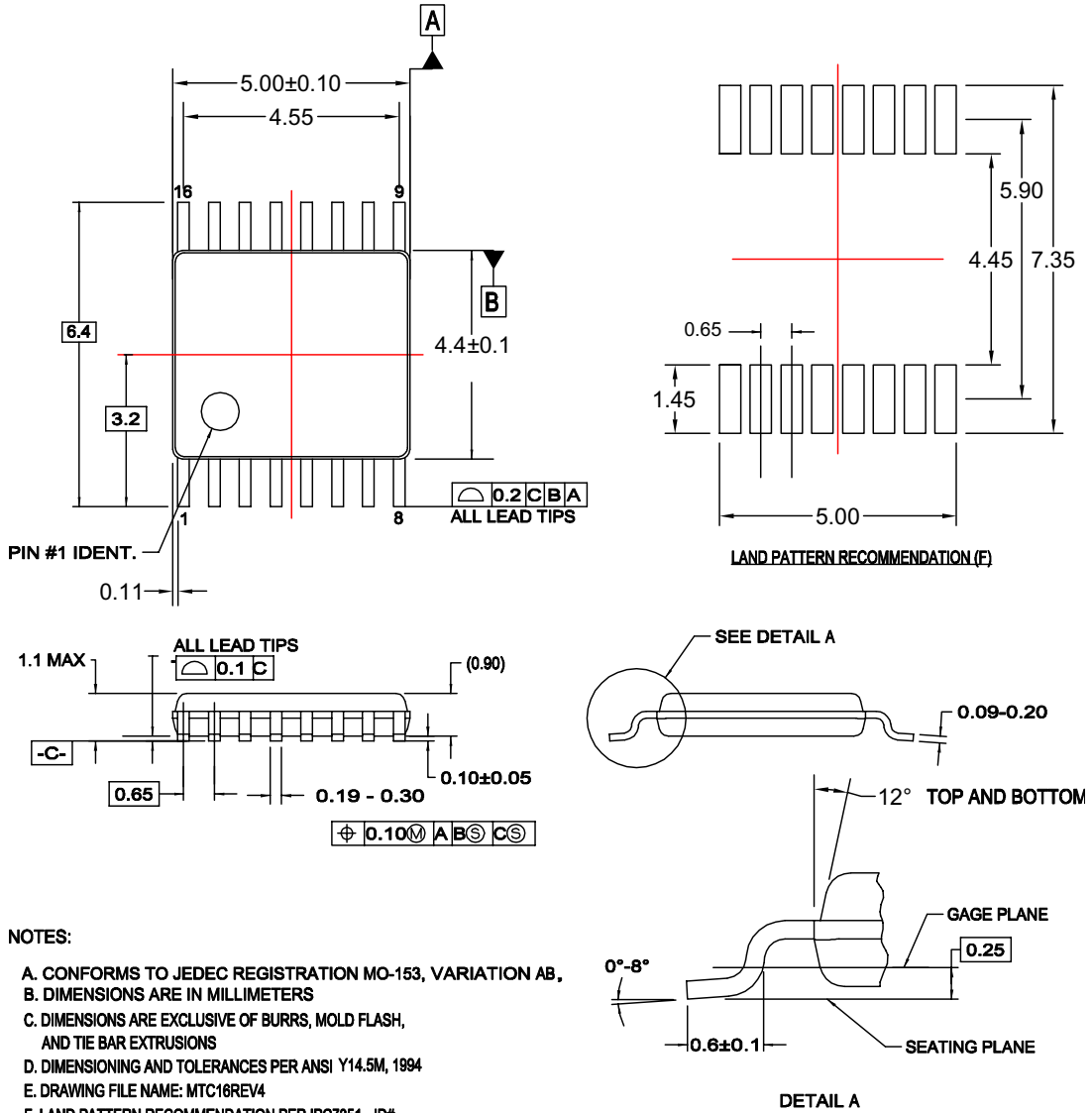


M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



- NOTES:**
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
 - B. DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
 - E. DRAWING FILE NAME: MTC16REV4
 - F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

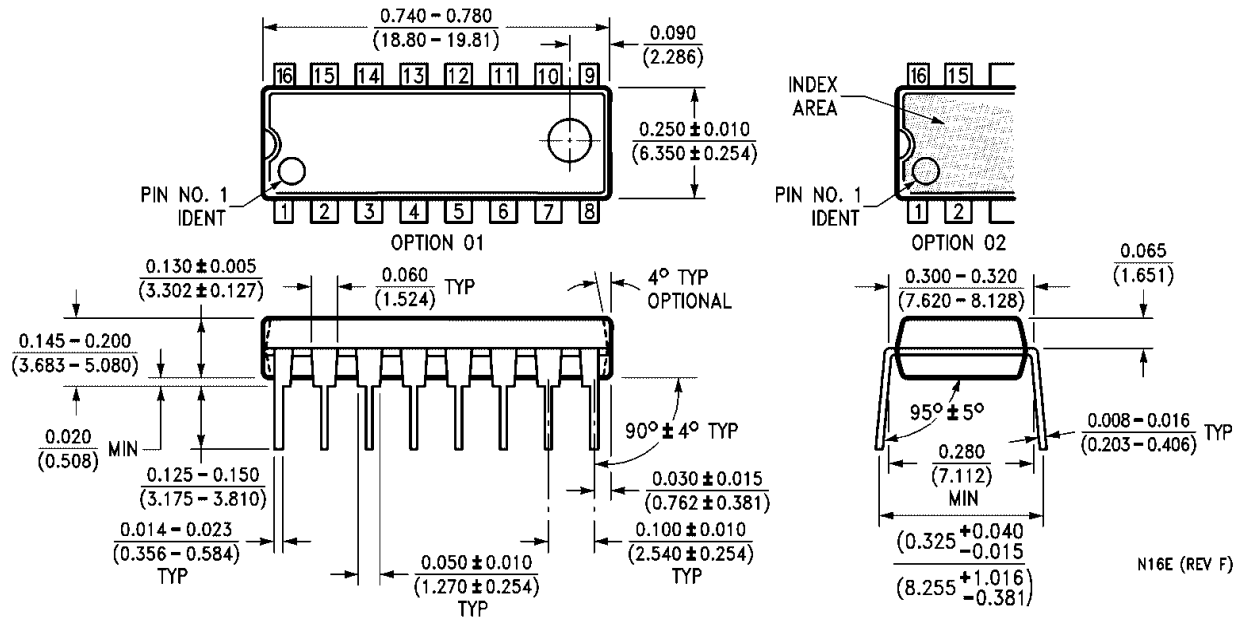



Figure 5. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

N16E (REV F)



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	HiSeC [™]	Programmable Active Droop [™]	TinyLogic [®]
Across the board. Around the world. [™]	<i>i-Lo</i> [™]	QFET [®]	TINYOPTO [™]
ActiveArray [™]	ImpliedDisconnect [™]	QS [™]	TinyPower [™]
Bottomless [™]	IntelliMAX [™]	QT Optoelectronics [™]	TinyWire [™]
Build it Now [™]	ISOPLANAR [™]	Quiet Series [™]	TruTranslation [™]
CoolFET [™]	MICROCOUPLER [™]	RapidConfigure [™]	μSerDes [™]
CROSSVOLT [™]	MicroPak [™]	RapidConnect [™]	UHC [®]
CTL [™]	MICROWIRE [™]	ScalarPump [™]	UniFET [™]
Current Transfer Logic [™]	MSX [™]	SMART START [™]	VCX [™]
DOME [™]	MSXPro [™]	SPM [®]	Wire [™]
E ² CMOS [™]	OCX [™]	STEALTH [™]	
EcoSPARK [®]	OCXPro [™]	SuperFET [™]	
EnSigna [™]	OPTOLOGIC [®]	SuperSOT [™] -3	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperSOT [™] -6	
FACT [®]	PACMAN [™]	SuperSOT [™] -8	
FAST [®]	POP [™]	SyncFET [™]	
FASTr [™]	Power220 [®]	TCM [™]	
FPS [™]	Power247 [®]	The Power Franchise [®]	
FRFET [®]	PowerEdge [™]	 ™	
GlobalOptoisolator [™]	PowerSaver [™]	TinyBoost [™]	
GTO [™]	PowerTrench [®]	TinyBuck [™]	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I24

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 74ACT175MTCX on WIN SOURCE](#)
-  [Fairchild/ON Semiconductor Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management