



**THE DATASHEET OF
74AC273SJX**



74AC273, 74ACT273 Octal D-Type Flip-Flop

Features

- Ideal buffer for microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See 377 for clock enable version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- Outputs source/sink 24mA
- 74ACT273 has TTL-compatible inputs

General Description

The AC273 and ACT273 have eight edge-triggered D-type flip-flops with individual D-type inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) input load and reset (clear) all flip-flops simultaneously.


The register is fully edge-triggered. The state of each D-type input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

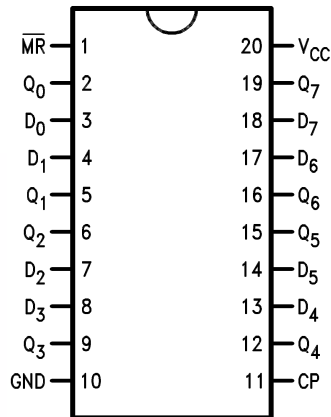
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|-----------------------------------------------------------------------------|
| 74AC273SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC273SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC273MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC273PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT273SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT273SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT273MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

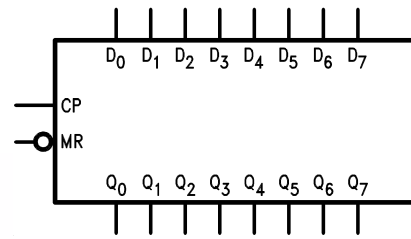
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

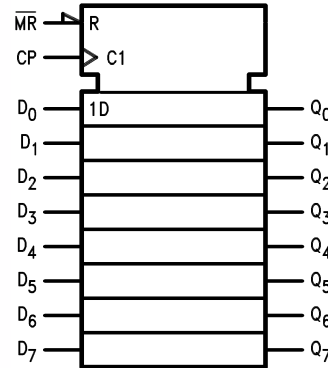
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Description

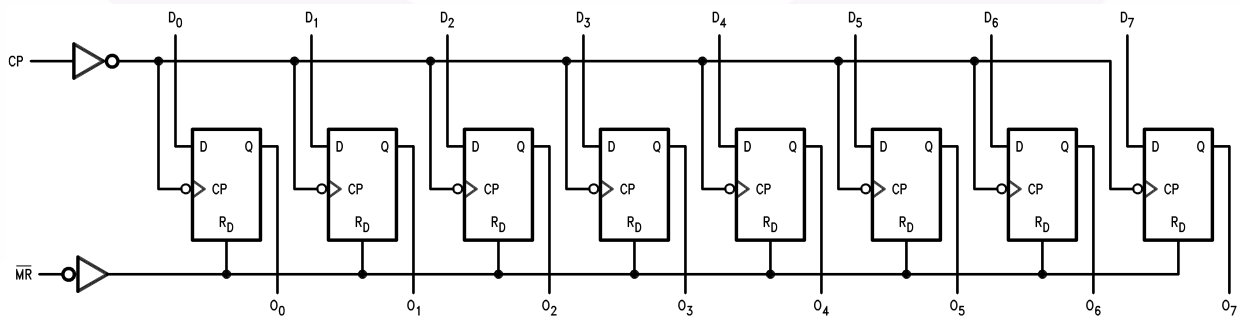
| Pin Names | Description |
|--------------------------------|-------------------|
| D ₀ -D ₇ | Data Inputs |
| $\overline{\text{MR}}$ | Master Reset |
| CP | Clock Pulse Input |
| Q ₀ -Q ₇ | Data Outputs |

Mode Select-Function Table

| Operating Mode | Inputs | | | Outputs |
|----------------|------------------------|----|----------------|----------------|
| | $\overline{\text{MR}}$ | CP | D _n | Q _n |
| Reset (Clear) | L | X | X | L |
| Load '1' | H | ↗ | H | H |
| Load '0' | H | ↗ | L | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|----------------------------------------------|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ | -20mA |
| | $V_I = V_{CC} + 0.5$ | +20mA |
| V_I | DC Input Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ | -20mA |
| | $V_O = V_{CC} + 0.5V$ | +20mA |
| V_O | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | $\pm 50mA$ |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|------------------------------------------------------------------------------------------------------------|----------------|
| V_{CC} | Supply Voltage AC | 2.0V to 6.0V |
| | ACT | 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | -40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units | |
|--------------------------------|-----------------------------------------------|---------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-------------------|---------------------------------|------|-------|--|
| | | | | Typ. | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.1 | 2.1 | | V | |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.9 | 0.9 | | V | |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50μA | 2.99 | 2.9 | 2.9 | | V | |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA | | 2.56 | 2.46 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽¹⁾ | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | 0.1 | 0.1 | | V | |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA | | 0.36 | 0.44 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾ | | 0.36 | 0.44 | | |
| I _{IN} ⁽²⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA | |
| I _{OLD} | Minimum Dynamic Output Current ⁽³⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA | |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA | |
| I _{CC} ⁽²⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA | |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
- Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units |
|------------------|-----------------------------------------------|---------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-------------------|---------------------------------|------|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50μA | 4.49 | 4.4 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾ | | 4.86 | 4.76 | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾ | | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1V | 0.6 | | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁵⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁶⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|---------------------------------------|------------------------------------|--------------------------------------------------|------|------|-----------------------------------------------------------|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 3.3 | 90 | 125 | | 75 | | MHz |
| | | 5.0 | 140 | 175 | | 125 | | |
| t _{PLH} | Propagation Delay, Clock to Output | 3.3 | 4.0 | 7.0 | 12.5 | 3.0 | 14.0 | ns |
| | | 5.0 | 3.0 | 5.5 | 9.0 | 2.5 | 10.0 | |
| t _{PHL} | Propagation Delay, Clock to Output | 3.3 | 4.0 | 7.0 | 13.0 | 3.5 | 14.5 | ns |
| | | 5.0 | 3.0 | 5.0 | 10.0 | 2.5 | 11.0 | |
| t _{PHL} | Propagation Delay, MR to Output | 3.3 | 4.0 | 7.0 | 13.0 | 3.5 | 14.0 | ns |
| | | 5.0 | 3.0 | 5.0 | 10.0 | 2.5 | 10.5 | |

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁷⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|----------------------------------------|------------------------------------|--------------------------------------------------|--------------------|-----------------------------------------------------------|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW, Data to CP | 3.3 | 3.5 | 5.5 | 6.0 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |
| t _H | Hold Time, HIGH or LOW, Data to CP | 3.3 | -2.0 | 0 | 0 | | ns |
| | | 5.0 | -1.0 | 1.0 | 1.0 | | |
| t _W | Clock Pulse Width, HIGH or LOW | 3.3 | 3.5 | 5.5 | 6.0 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |
| t _W | MR Pulse Width, HIGH or LOW | 3.3 | 2.0 | 5.5 | 6.0 | | ns |
| | | 5.0 | 1.5 | 4.0 | 4.5 | | |
| t _{rec} | Recovery Time, MR to CP | 3.3 | 1.5 | 3.5 | 4.5 | | ns |
| | | 5.0 | 1.0 | 2.0 | 3.0 | | |

Note:

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

| Symbol | Parameter | V_{CC} (V) ⁽⁸⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|-----------------------|------------------------------------------------|-----------------------------|----------------------------------------------------|------|------|--------------------------------------------------------------------------|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f_{MAX} | Maximum Clock Frequency | 2.0 | 125 | 189 | | 110 | | MHz |
| t_{PLH} , t_{PHL} | Propagation Delay, CP to Q_n | 5.0 | 1.5 | 6.5 | 8.5 | 1.5 | 9.0 | ns |
| t_{PHL} | Propagation Delay, \overline{MR} to Q_n | 5.0 | 1.5 | 7.0 | 9.0 | 1.5 | 8.5 | ns |

Note:

8. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Operating Requirements for ACT

| Symbol | Parameter | V_{CC} (V) ⁽⁹⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|--------|------------------------------------------|-----------------------------|----------------------------------------------------|--------------------|--------------------------------------------------------------------------|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t_S | Setup Time, HIGH or LOW, D_n to CP | 5.0 | 1.0 | 3.5 | 3.5 | | ns |
| t_H | Hold Time, HIGH or LOW, D_n to CP | 5.0 | -0.5 | 1.5 | 1.5 | | ns |
| t_W | Clock Pulse Width, HIGH or LOW | 5.0 | 2.0 | 4.0 | 4.0 | | ns |
| t_W | \overline{MR} Pulse Width, HIGH or LOW | 5.0 | 1.5 | 4.0 | 4.0 | | ns |
| t_W | Recovery Time, \overline{MR} to CP | 5.0 | 0.5 | 3.0 | 3.0 | | ns |

Note:

9. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|----------|---------------------------------------|------------------------|------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{OPEN}$ | 4.5 | pF |
| C_{PD} | Power Dissipation Capacitance for AC | $V_{CC} = 5.0\text{V}$ | 50.0 | pF |
| | Power Dissipation Capacitance for ACT | | 40.0 | |

Physical Dimensions

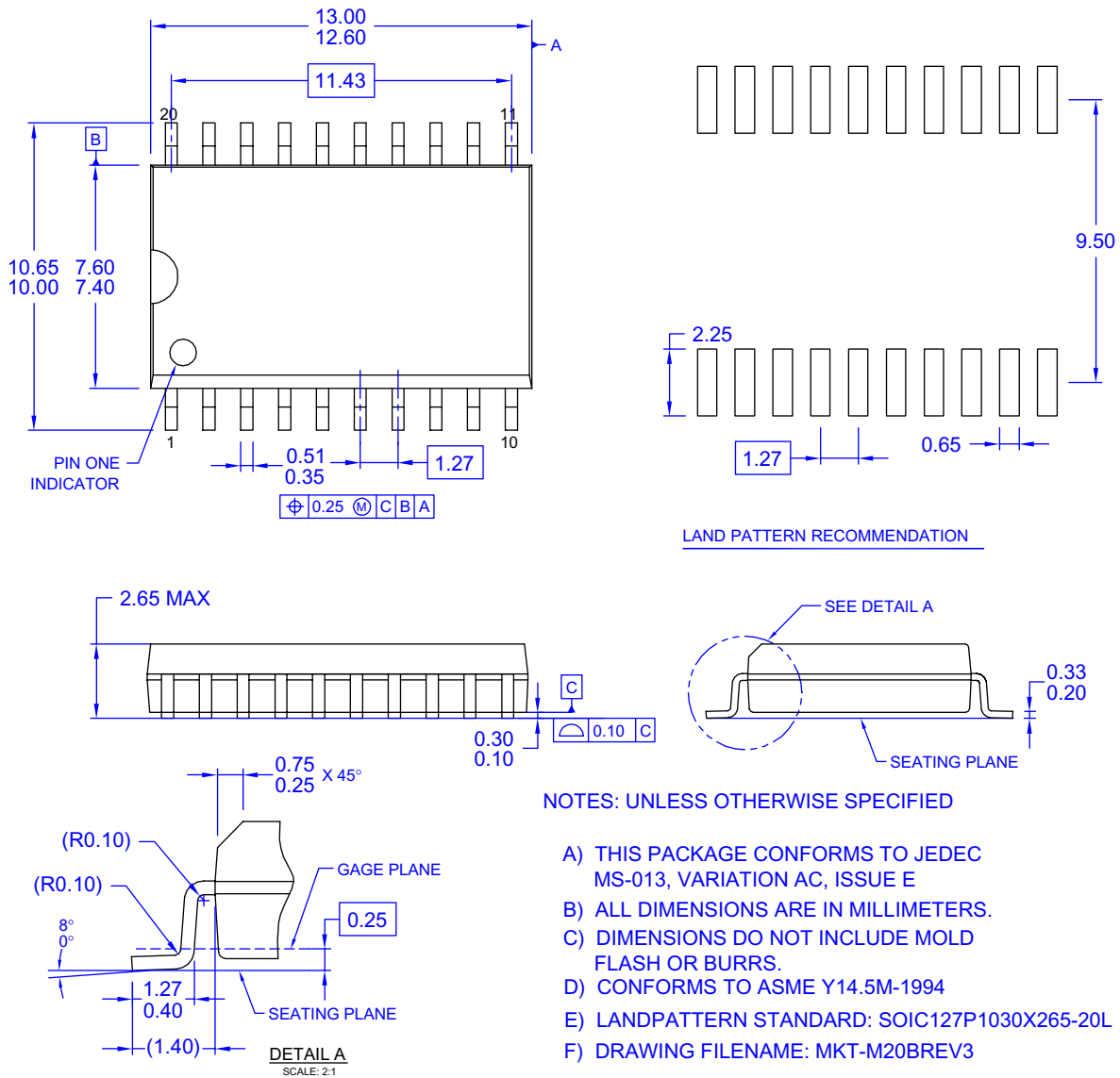


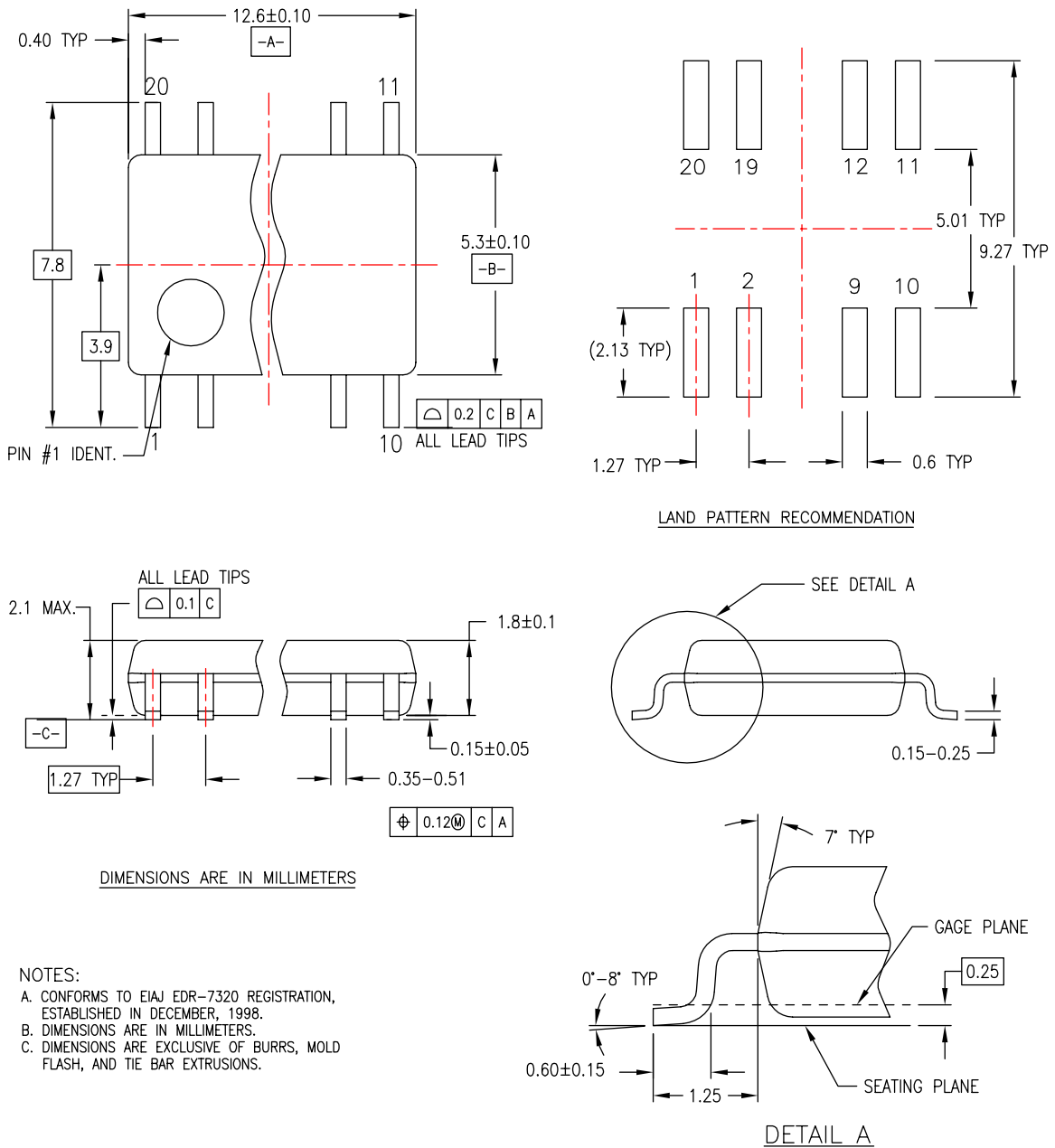
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Physical Dimensions (Continued)



M20DREVC

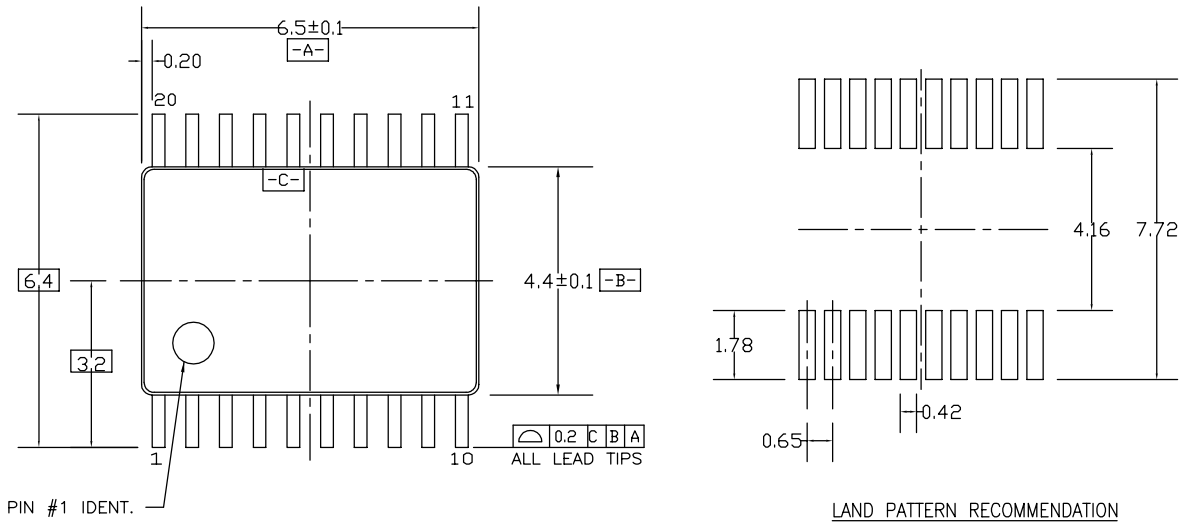
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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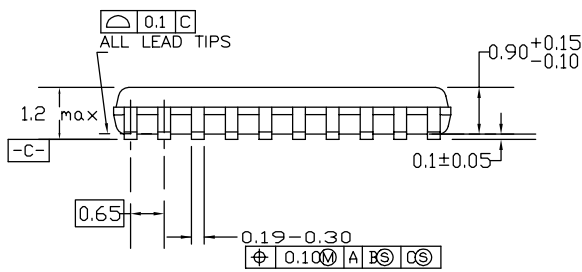
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Physical Dimensions (Continued)

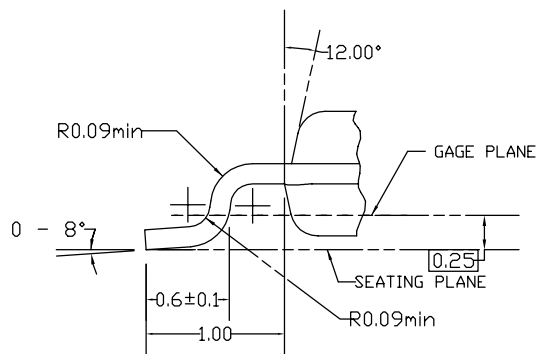
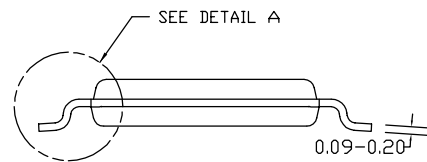


PIN #1 IDENT.

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

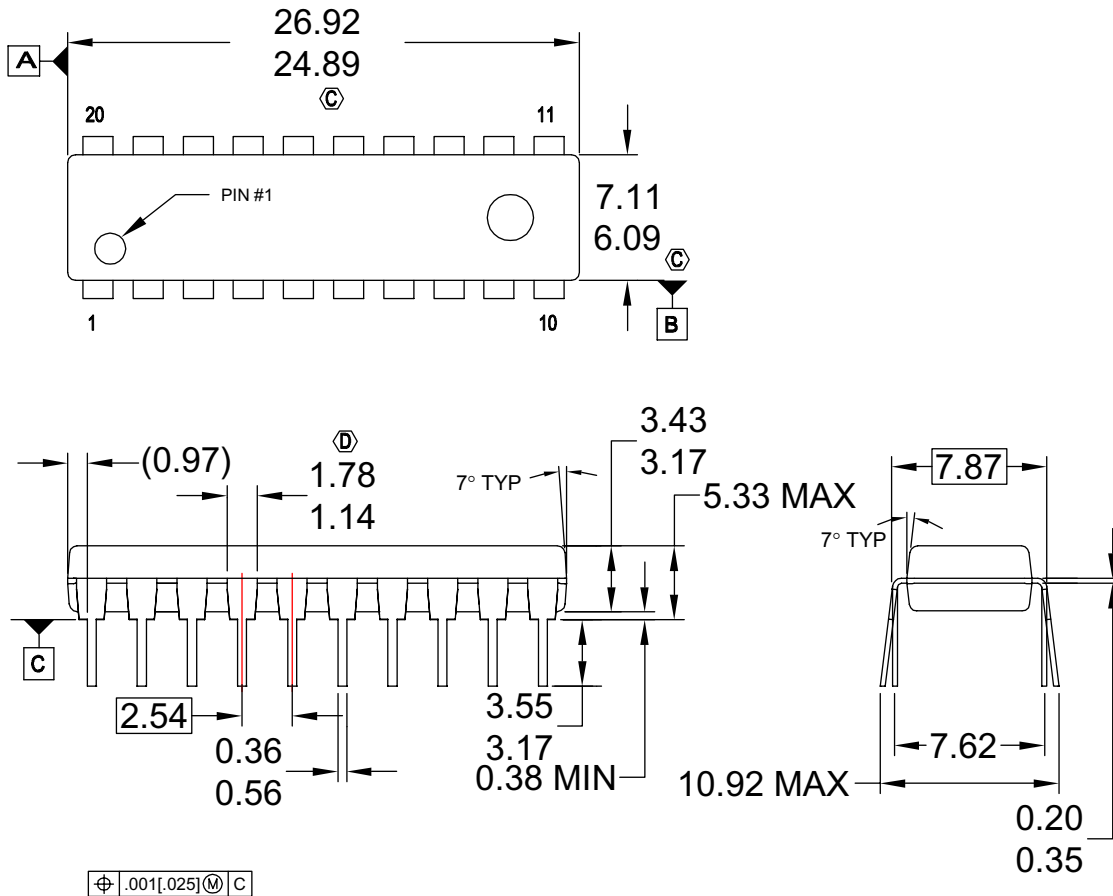
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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

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|--------------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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