



# THE DATASHEET OF 74AC174MTR





## HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:  
 $f_{MAX} = 250\text{MHz}$  (TYP.) at  $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A}$ (MAX.) at  $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

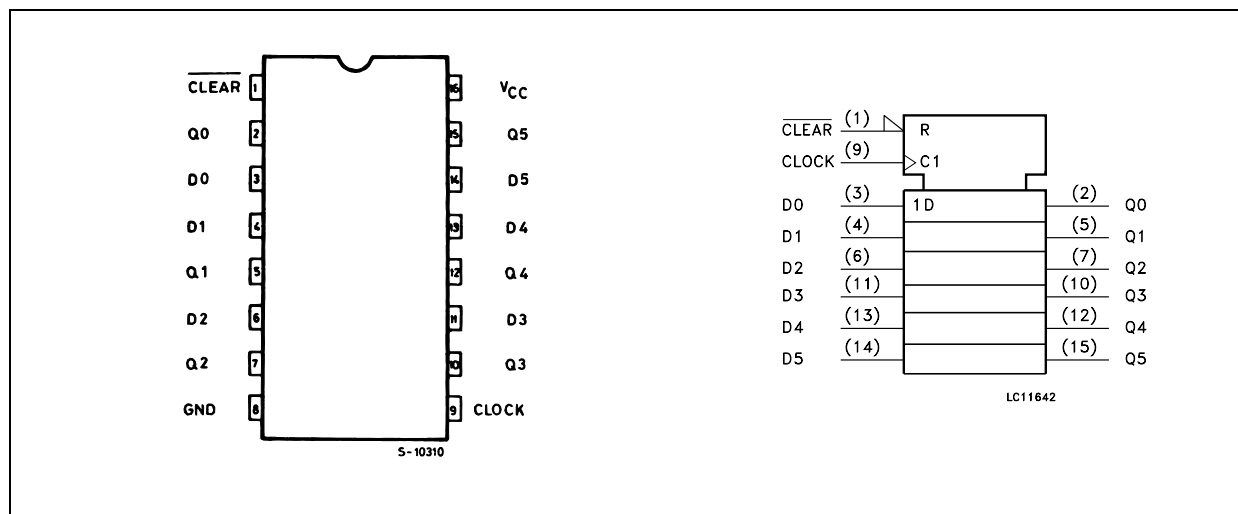
PACKAGE	TUBE	T & R
DIP	74AC174B	
SOP	74AC174M	74AC174MTR
TSSOP		74AC174TTR

### DESCRIPTION

The 74AC174 is an advanced high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

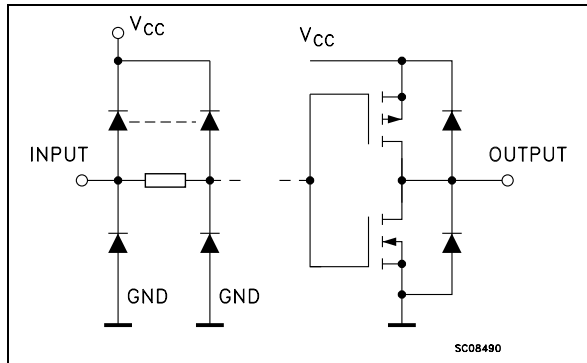
Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse. When the  $\overline{\text{CLEAR}}$  input is held low, the Q outputs are held low independently of the other inputs. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# 74AC174

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

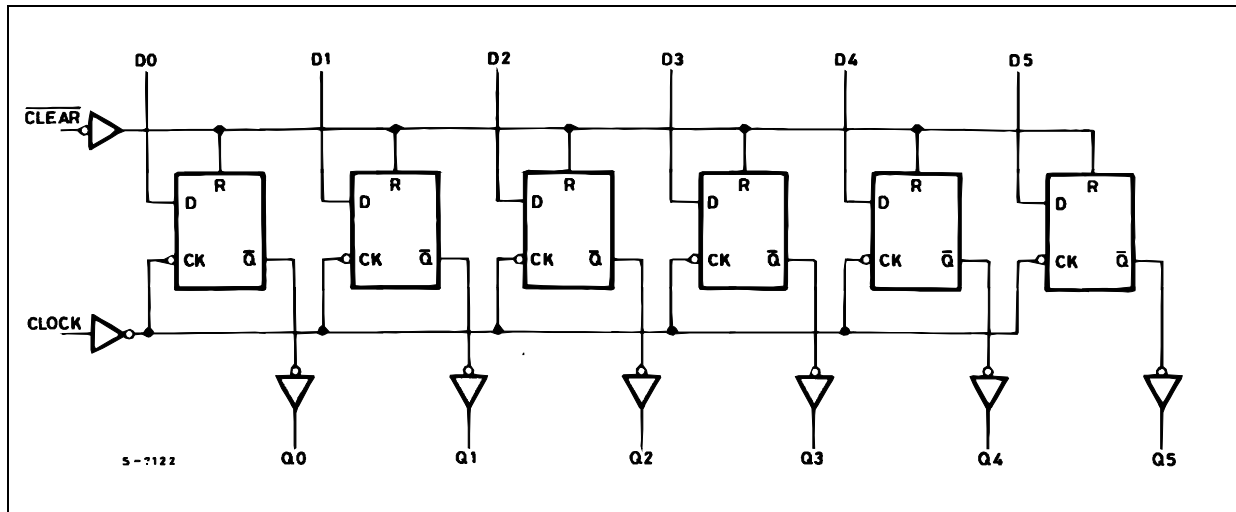
PIN No	SYMBOL	NAME AND FUNCTION
1	CLEAR	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW-to-HIGH, Edge Trigger)
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

## TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
CLEAR	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

X : Don't Care

## LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 300$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2 to 6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 30% to 70% of  $V_{CC}$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V <sub>IL</sub>	Low Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V <sub>OH</sub>	High Level Output Voltage	3.0	I <sub>O</sub> = -50 μA	2.9	2.99		2.9		2.9		V
		4.5	I <sub>O</sub> = -50 μA	4.4	4.49		4.4		4.4		
		5.5	I <sub>O</sub> = -50 μA	5.4	5.49		5.4		5.4		
		3.0	I <sub>O</sub> = -12 mA	2.56			2.46		2.4		
		4.5	I <sub>O</sub> = -24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> = -24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	3.0	I <sub>O</sub> = 50 μA		0.002	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> = 50 μA		0.001	0.1		0.1		0.1	
		5.5	I <sub>O</sub> = 50 μA		0.001	0.1		0.1		0.1	
		3.0	I <sub>O</sub> = 12 mA			0.36		0.44		0.5	
		4.5	I <sub>O</sub> = 24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> = 24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , Input  $t_r = t_f = 3\text{ns}$ )

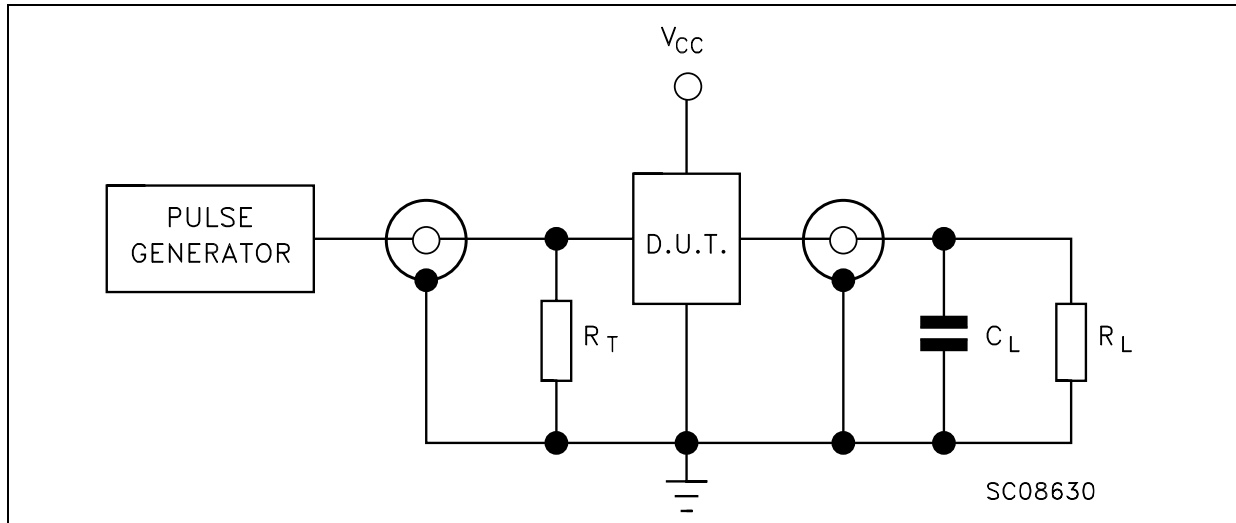
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CLOCK to Y	3.3 <sup>(*)</sup>		1.5	8.5	11.0		12.5		14.0	ns
		5.0 <sup>(**)</sup>		1.5	6.0	8.0		9.5		10.5	
$t_{PHL}$	Propagation Delay Time CLEAR to Y	3.3 <sup>(*)</sup>		1.5	9.0	11.5		12.5		13.5	ns
		5.0 <sup>(**)</sup>		1.5	7.0	9.0		10.5		11.0	
$t_{WL}$	CLEAR Pulse Width, LOW	3.3 <sup>(*)</sup>			1.0	5.5		7.0		7.0	ns
		5.0 <sup>(**)</sup>			1.0	5.0		5.0		5.0	
$t_W$	CLOCK Pulse Width	3.3 <sup>(*)</sup>			1.0	5.5		7.0		7.0	ns
		5.0 <sup>(**)</sup>			1.0	5.0		5.0		5.0	
$t_s$	Setup Time D to CLOCK, HIGH or LOW	3.3 <sup>(*)</sup>			2.5	6.5		7.0		7.0	ns
		5.0 <sup>(**)</sup>			2.0	5.0		5.5		5.5	
$t_h$	Hold Time D to CLOCK, HIGH or LOW	3.3 <sup>(*)</sup>			1.0	3.0		3.0		3.0	ns
		5.0 <sup>(**)</sup>			0.5	3.0		3.0		3.0	
$t_{REM}$	Recovery Time CLEAR to CK	3.3 <sup>(*)</sup>			0	2.5		2.5		2.5	ns
		5.0 <sup>(**)</sup>			0	2.0		2.0		2.0	
$f_{MAX}$	Maximum Clock Frequency	3.3 <sup>(*)</sup>		90	200		70		70		MHz
		5.0 <sup>(**)</sup>		100	250		100		100		

(\*) Voltage range is  $3.3\text{V} \pm 0.3\text{V}$ (\*\*) Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance	5.0			4.5						pF
$C_{PD}$	Power Dissipation Capacitance (note1)	5.0	$f_{IN} = 10\text{MHz}$		33						pF

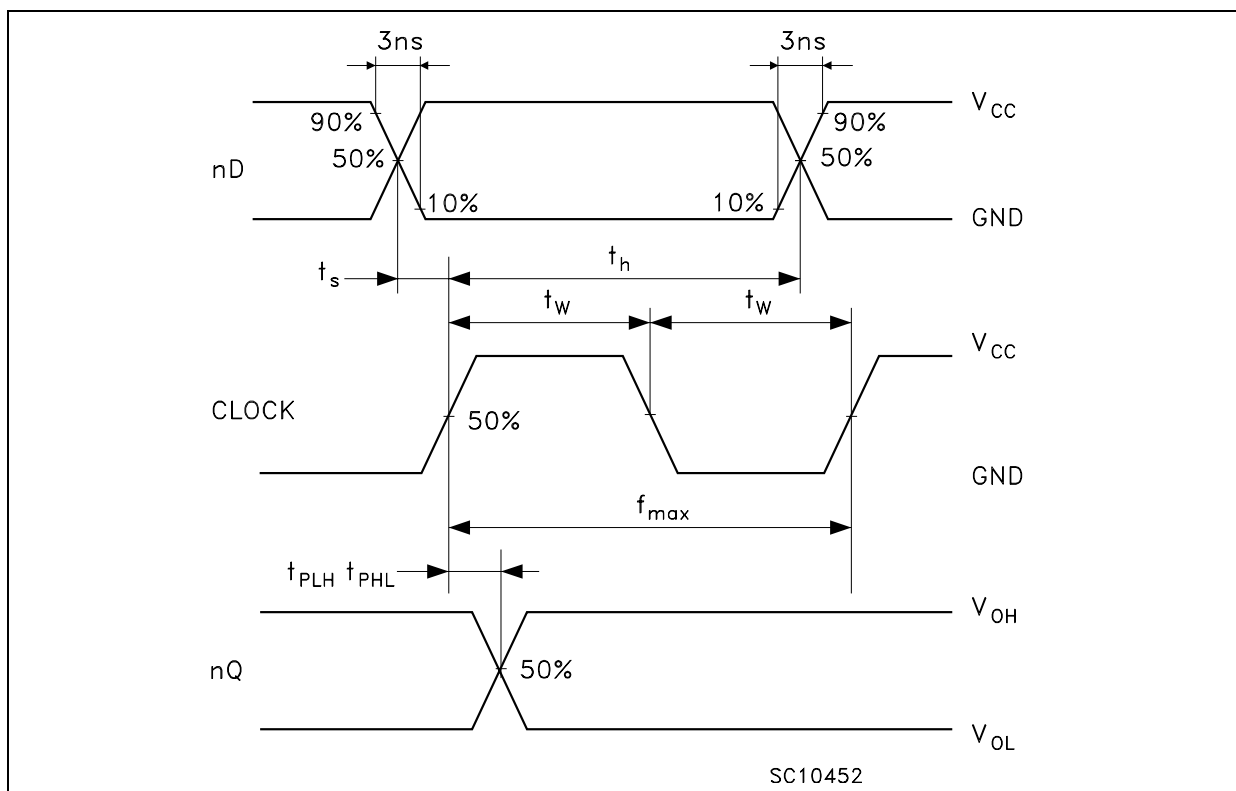
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$  (per circuit)

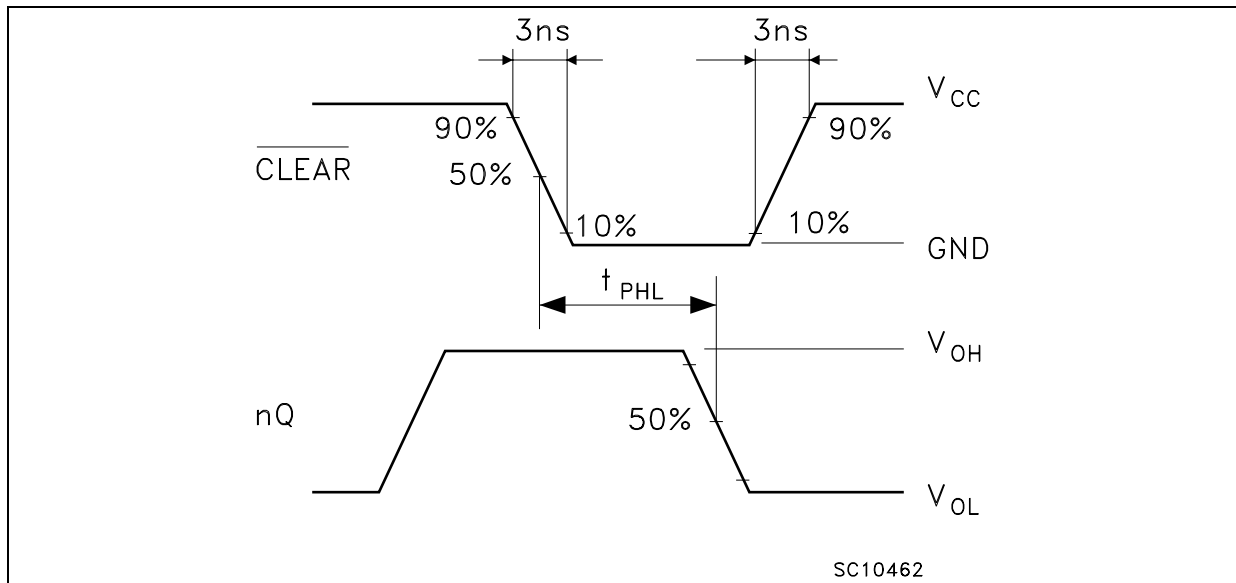
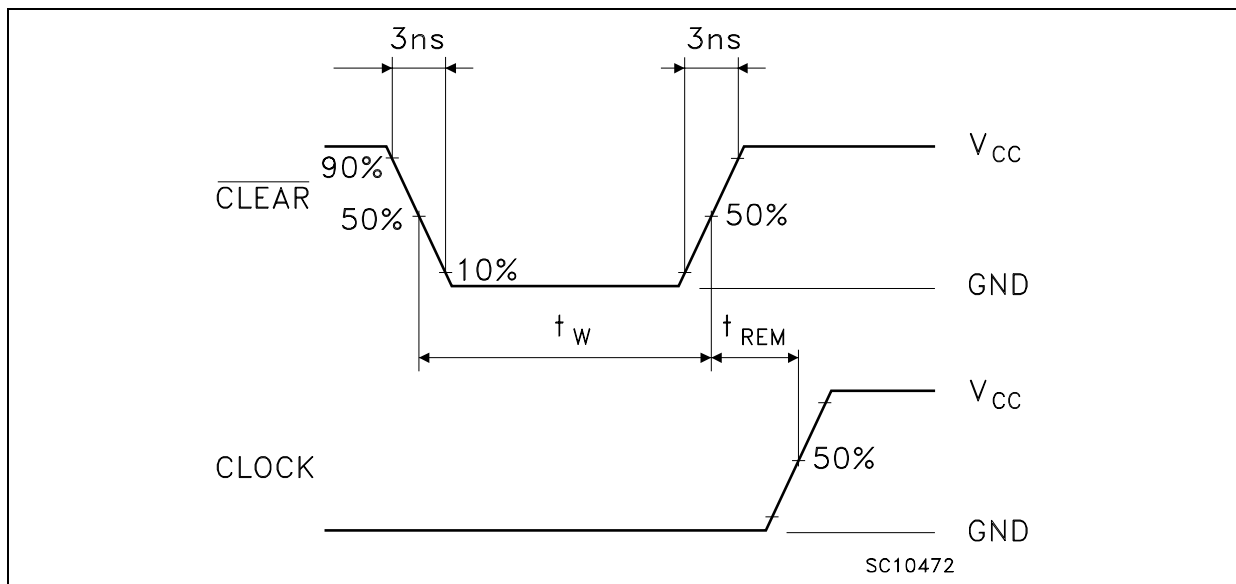
TEST CIRCUIT



$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

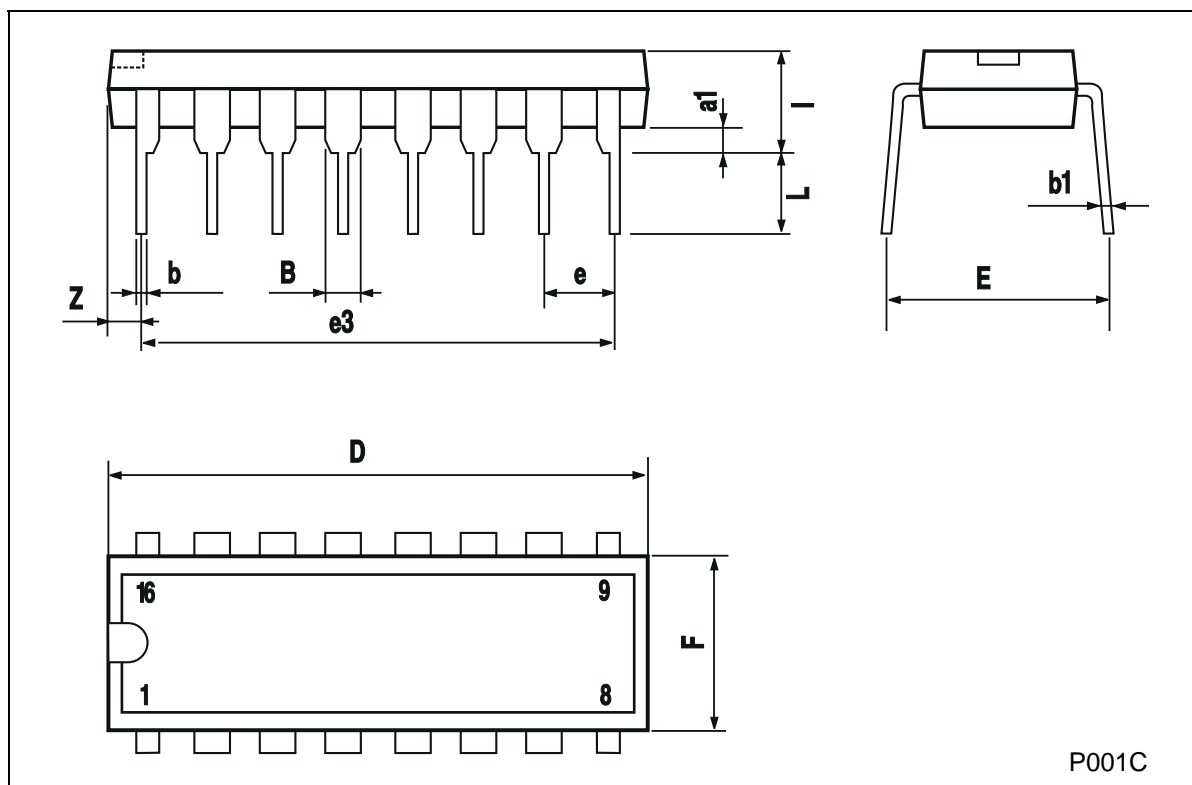
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)**WAVEFORM 3: RECOVERY TIME** (f=1MHz; 50% duty cycle)

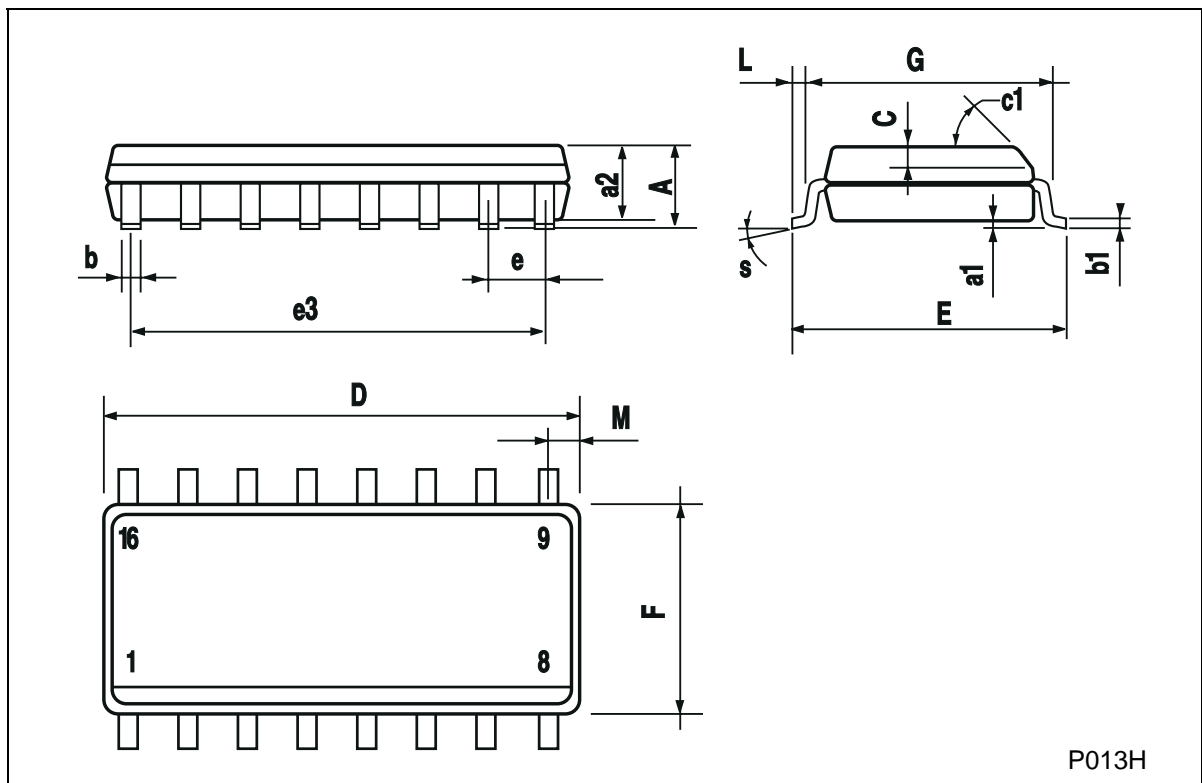
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



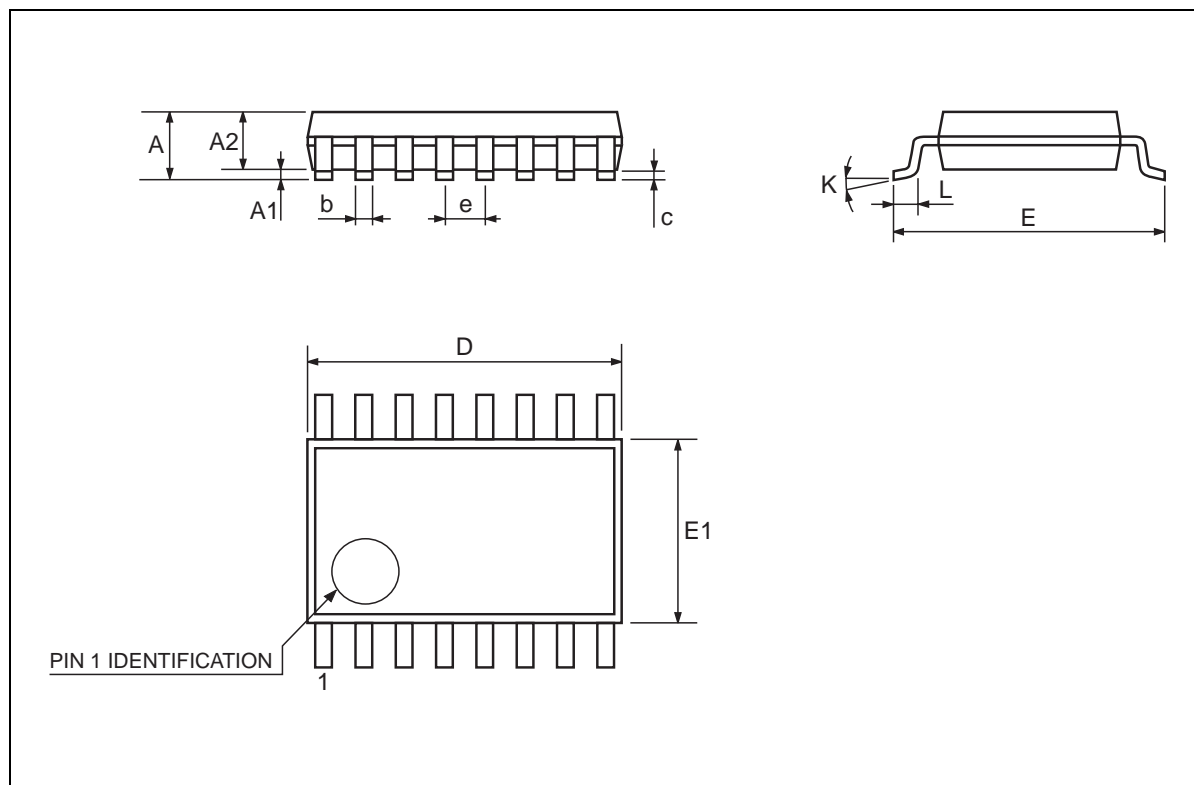
## SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



## TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES



Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>



## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 74AC174MTR](#) on WIN SOURCE
-  [STMicroelectronics](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management