



**THE DATASHEET OF  
74AC109SC**



# 74AC109, 74ACT109 Dual $\overline{JK}$ Positive Edge-Triggered Flip-Flop

## Features

- $I_{CC}$  reduced by 50%
- Outputs source/sink 24mA
- ACT109 has TTL-compatible inputs

## General Description

The AC/ACT109 consists of two high-speed completely independent transition clocked  $\overline{JK}$  flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The  $\overline{JK}$  design allows operation as a D-Type flip-flop (refer to AC/ACT74 data sheet) by connecting the J and  $\overline{K}$  inputs together.

Asynchronous Inputs:

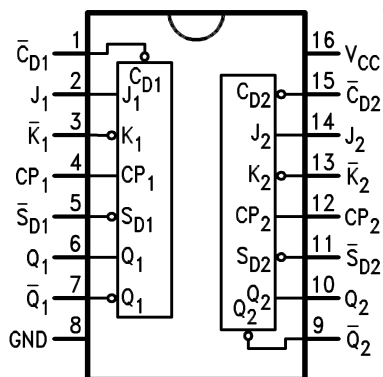
- LOW input to  $\overline{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\overline{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\overline{C}_D$  and  $\overline{S}_D$  makes both Q and  $\overline{Q}$  HIGH

## Ordering Information

Order Number	Package Number	Package Description
74AC109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC109SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC109MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC109MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT109PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

## Connection Diagram

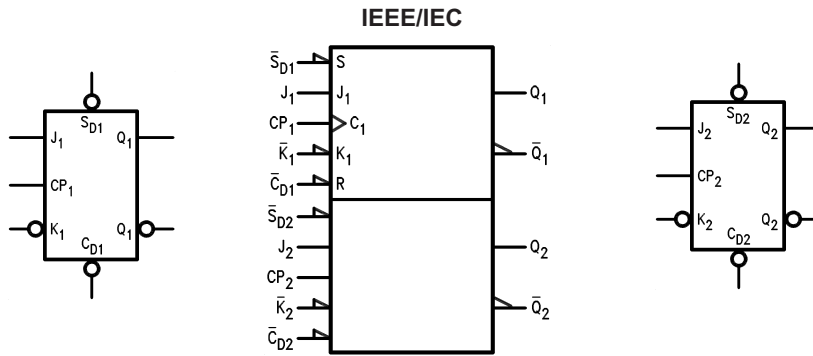


## Pin Descriptions

Pin Names	Description
$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

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### Logic Symbols



### Truth Table

Each half.

Inputs					Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↗	L	L	L	H
H	H	↗	H	L	Toggle	
H	H	↗	L	H	$Q_0$	$\bar{Q}_0$
H	H	↗	H	H	H	L
H	H	L	X	X	$Q_0$	$\bar{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

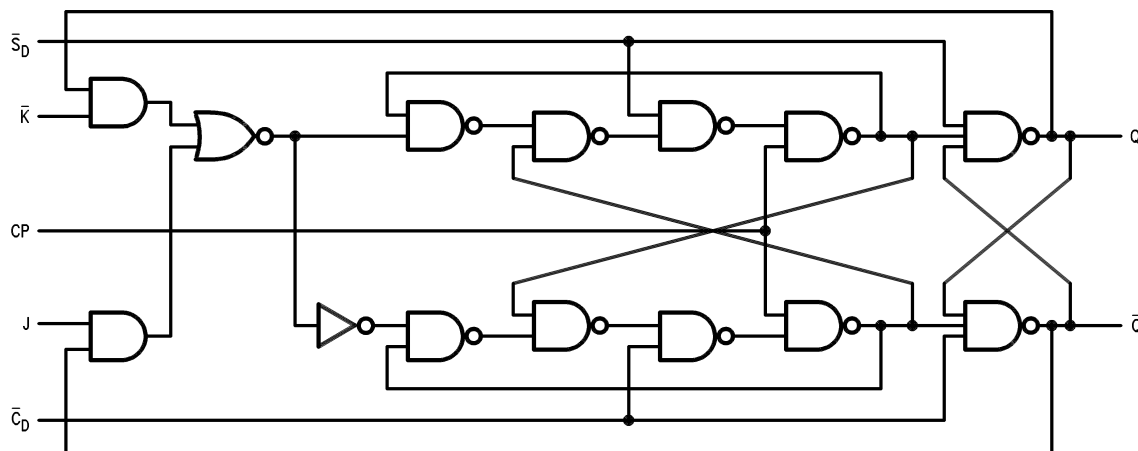
↗ = LOW-to-HIGH Transition

X = Immaterial

$Q_0(\bar{Q}_0)$  = Previous  $Q_0(\bar{Q}_0)$  before LOW-to-HIGH Transition of Clock

### Logic Diagram

One half shown.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -12mA		2.56	2.46			
		4.5		I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1		V	
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 12mA		0.36	0.44			
		4.5		I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44		
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA	
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0		μA	

**Notes:**

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5	I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5	I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	± 1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85V Min.			-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0		μA

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(6)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3	125	150		100		MHz
		5.0	150	175		125		
t <sub>PLH</sub>	Propagation Delay, CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	3.3	4.0	8.0	13.5	3.5	16.0	ns
		5.0	2.5	6.0	10.0	2.0	10.5	
t <sub>PHL</sub>	Propagation Delay, CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	3.3	3.0	8.0	14.0	3.0	14.5	ns
		5.0	2.0	6.0	10.0	1.5	10.5	
t <sub>PLH</sub>	Propagation Delay, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	3.3	3.0	8.0	12.0	2.5	13.0	ns
		5.0	2.5	6.0	9.0	2.0	10.0	
t <sub>PHL</sub>	Propagation Delay, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	3.3	3.0	10.0	12.0	3.0	13.5	ns
		5.0	2.0	7.5	9.5	2.0	10.5	

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF		Units
			Typ.	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW, J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	3.3	3.5	6.5	7.5		ns
		5.0	2.0	4.5	5.0		
t <sub>H</sub>	Hold Time, HIGH or LOW, J <sub>n</sub> or $\bar{K}_n$ to CP <sub>n</sub>	3.3	-1.5	0	0		ns
		5.0	-0.5	0.5	0.5		
t <sub>W</sub>	Pulse Width, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$	3.3	2.0	7.0	7.5		ns
		5.0	2.0	4.5	5.0		
t <sub>REC</sub>	Recovery Time, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP <sub>n</sub>	3.3	-2.5	0	0		ns
		5.0	-1.5	0	0		

**Note:**

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(8)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Clock Frequency	5.0	145	210		125		MHz
$t_{PLH}$	Propagation Delay, $CP_n$ to $Q_n$ or $\bar{Q}_n$	5.0	4.0	7.0	11.0	3.5	13.0	ns
$t_{PHL}$	Propagation Delay, $CP_n$ to $Q_n$ or $\bar{Q}_n$	5.0	3.0	6.0	10.0	2.5	11.5	ns
$t_{PLH}$	Propagation Delay, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $Q_n$ or $\bar{Q}_n$	5.0	2.5	5.5	9.5	2.0	10.5	ns
$t_{PHL}$	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $Q_n$ or $\bar{Q}_n$	5.0	2.5	6.0	10.0	2.0	11.5	ns

**Note:**8. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ 

## AC Operating Requirements for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(9)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum		
$t_S$	Setup Time, HIGH or LOW, $J_n$ or $\bar{K}_n$ to $CP_n$	5.0	0.5	2.0	2.5	ns
$t_H$	Hold Time, HIGH or LOW, $J_n$ or $\bar{K}_n$ to $CP_n$	5.0	0	2.0	2.0	ns
$t_W$	Pulse Width, $CP_n$ or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$	5.0	3.0	5.0	6.0	ns
$t_{rec}$	Recovery Time, $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $CP_n$	5.0	-2.5	0	0	ns

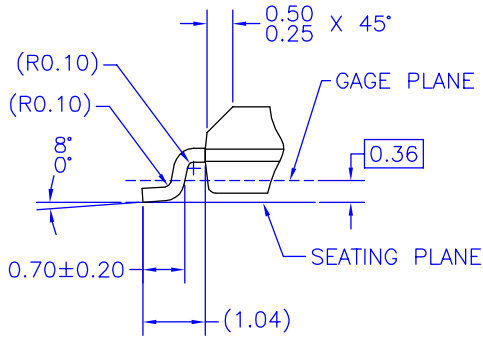
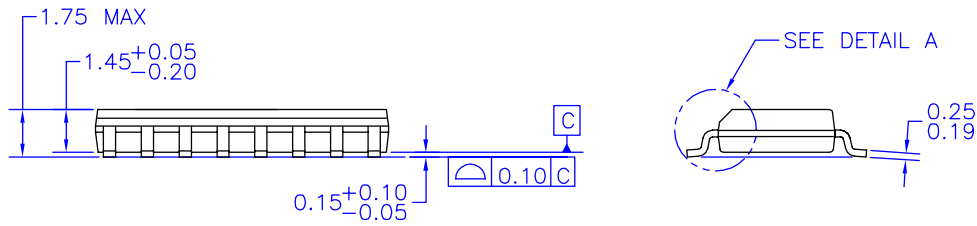
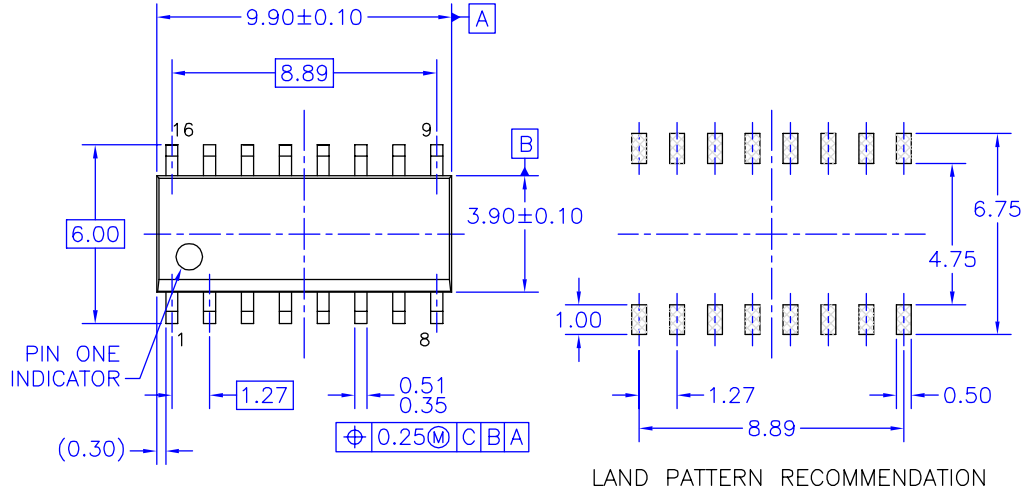
**Note:**9. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ 

## Capacitance

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	35.0	pF

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

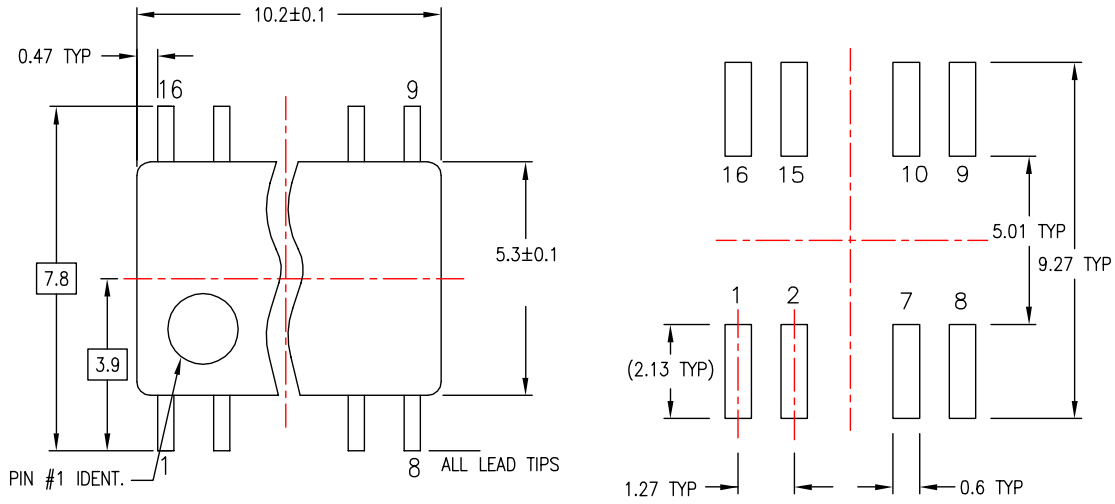
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICRONS / 5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

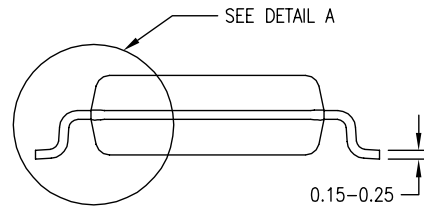
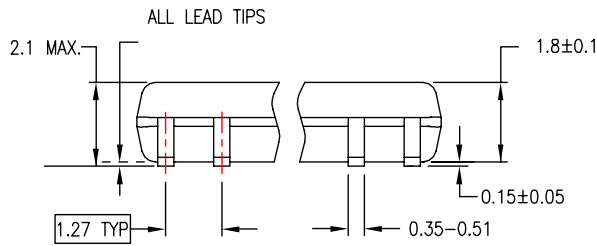
**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



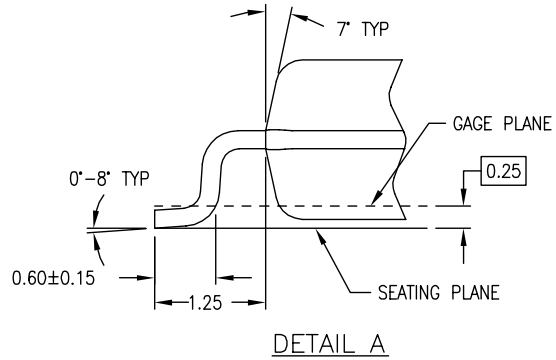
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

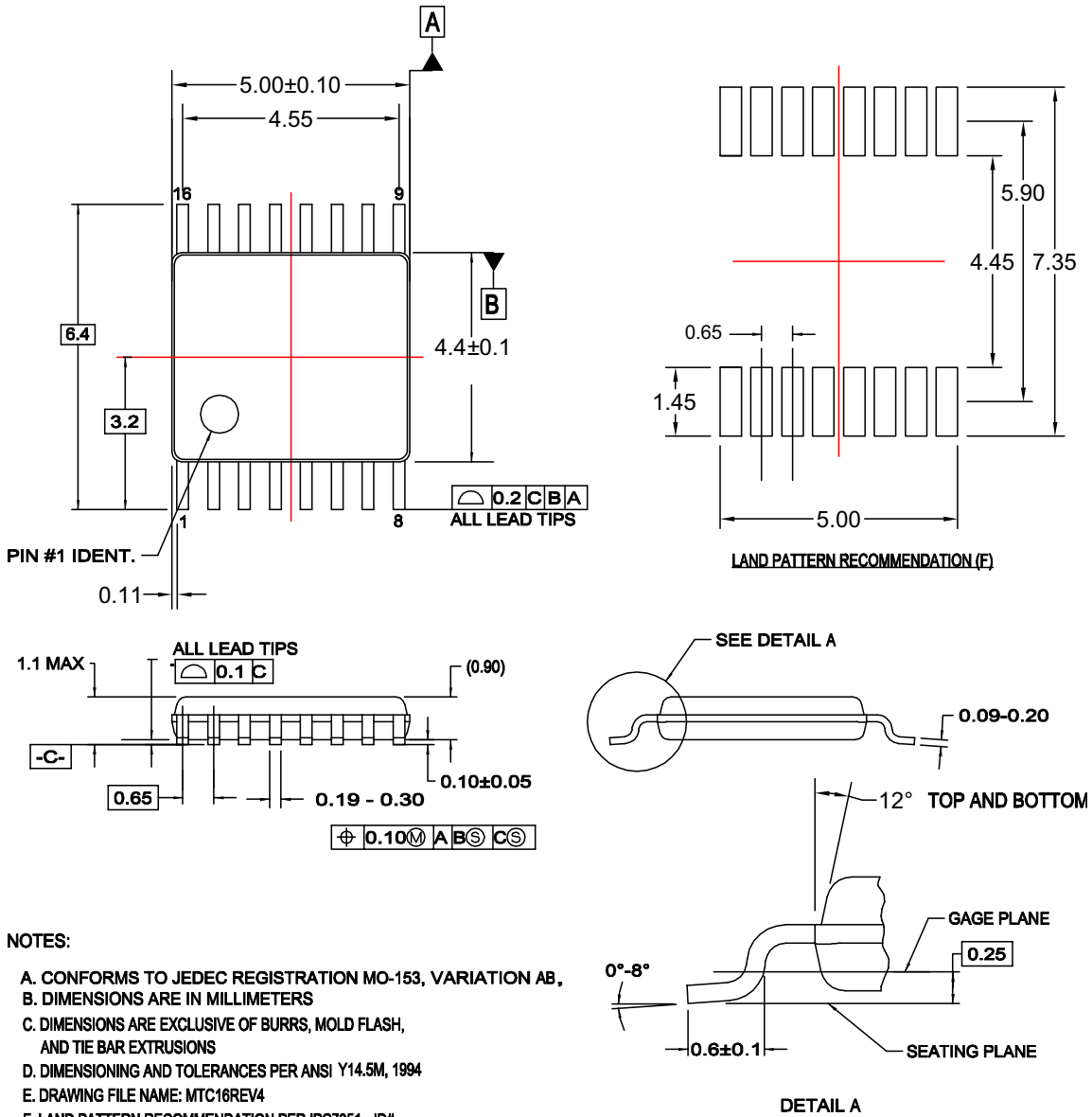


M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

### Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
- E. DRAWING FILE NAME: MTC16REV4
- F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

**Physical Dimensions** (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

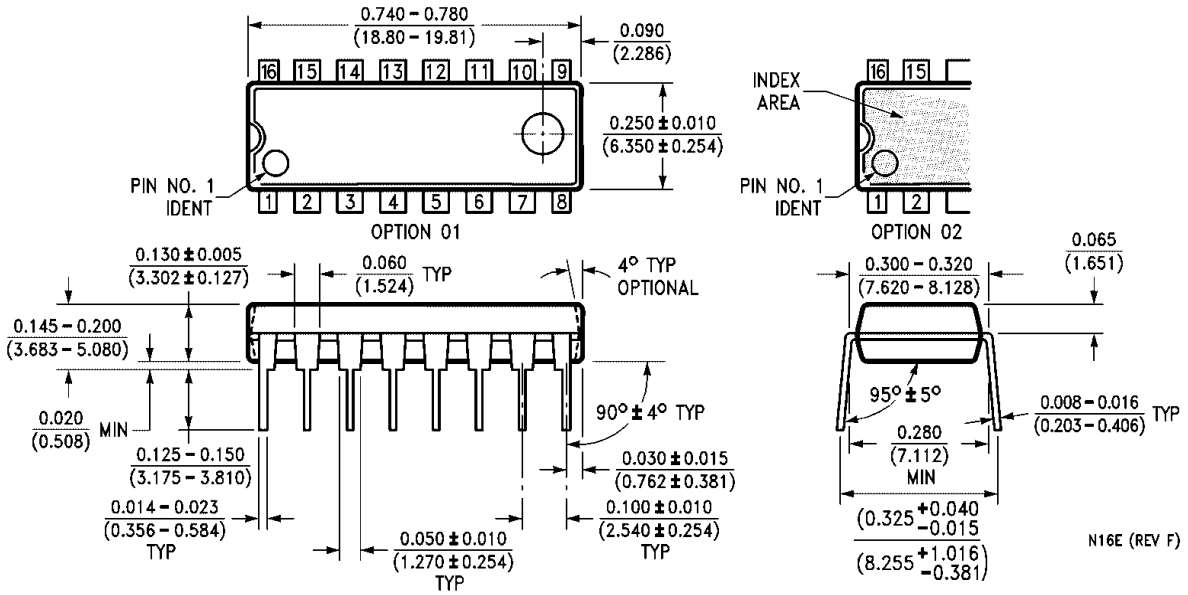


Figure 4. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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ActiveArray <sup>™</sup>	ImpliedDisconnect <sup>™</sup>	QS <sup>™</sup>	TinyPower <sup>™</sup>
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CTL <sup>™</sup>	MICROWIRE <sup>™</sup>	ScalarPump <sup>™</sup>	UniFET <sup>™</sup>
Current Transfer Logic <sup>™</sup>	MSX <sup>™</sup>	SMART START <sup>™</sup>	VCX <sup>™</sup>
DOME <sup>™</sup>	MSXPro <sup>™</sup>	SPM <sup>®</sup>	Wire <sup>™</sup>
E <sup>2</sup> CMOS <sup>™</sup>	OCX <sup>™</sup>	STEALTH <sup>™</sup>	
EcoSPARK <sup>®</sup>	OCXPro <sup>™</sup>	SuperFET <sup>™</sup>	
EnSigna <sup>™</sup>	OPTOLOGIC <sup>®</sup>	SuperSOT <sup>™</sup> -3	
FACT Quiet Series <sup>™</sup>	OPTOPLANAR <sup>®</sup>	SuperSOT <sup>™</sup> -6	
FACT <sup>®</sup>	PACMAN <sup>™</sup>	SuperSOT <sup>™</sup> -8	
FAST <sup>®</sup>	POP <sup>™</sup>	SyncFET <sup>™</sup>	
FASTr <sup>™</sup>	Power220 <sup>®</sup>	TCM <sup>™</sup>	
FPS <sup>™</sup>	Power247 <sup>®</sup>	The Power Franchise <sup>®</sup>	
FRFET <sup>®</sup>	PowerEdge <sup>™</sup>	 ™	
GlobalOptoisolator <sup>™</sup>	PowerSaver <sup>™</sup>	TinyBoost <sup>™</sup>	
GTO <sup>™</sup>	PowerTrench <sup>®</sup>	TinyBuck <sup>™</sup>	

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## PRODUCT STATUS DEFINITIONS


### Definition of Terms

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