

74ABT841

10-bit bus interface latch; 3-state

Rev. 4 — 7 November 2011

Product data sheet

1. General description

The 74ABT841 high performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT841 bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when latch enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the output enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the output is in the high-impedance state.

2. Features and benefits

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Broadside pinout
- Output capability: +64 mA and -32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

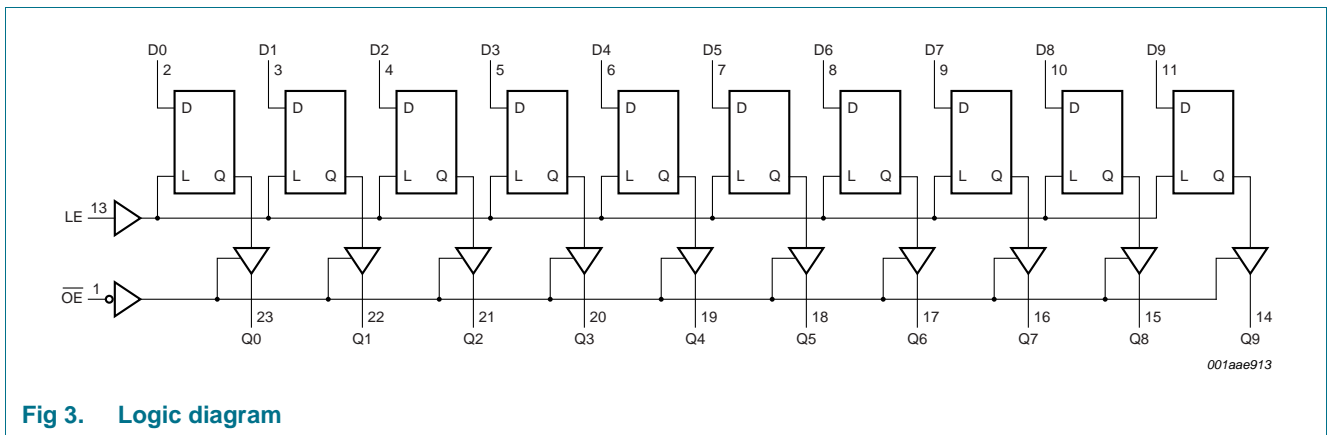
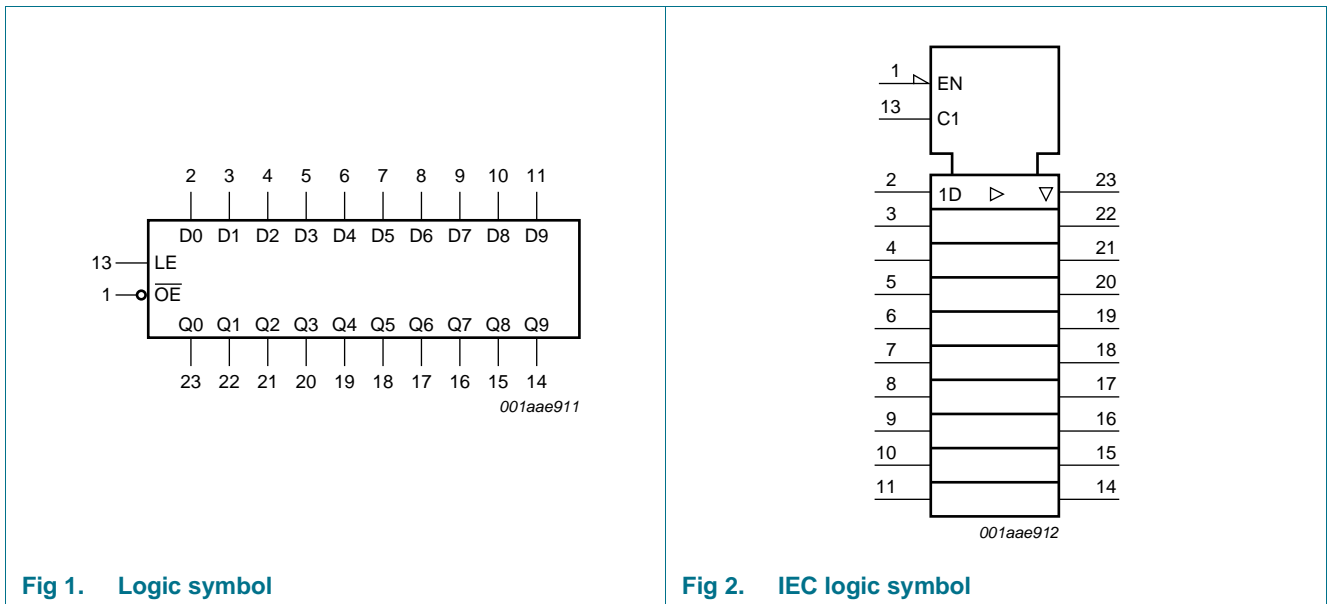


3. Ordering information

Table 1. Ordering information

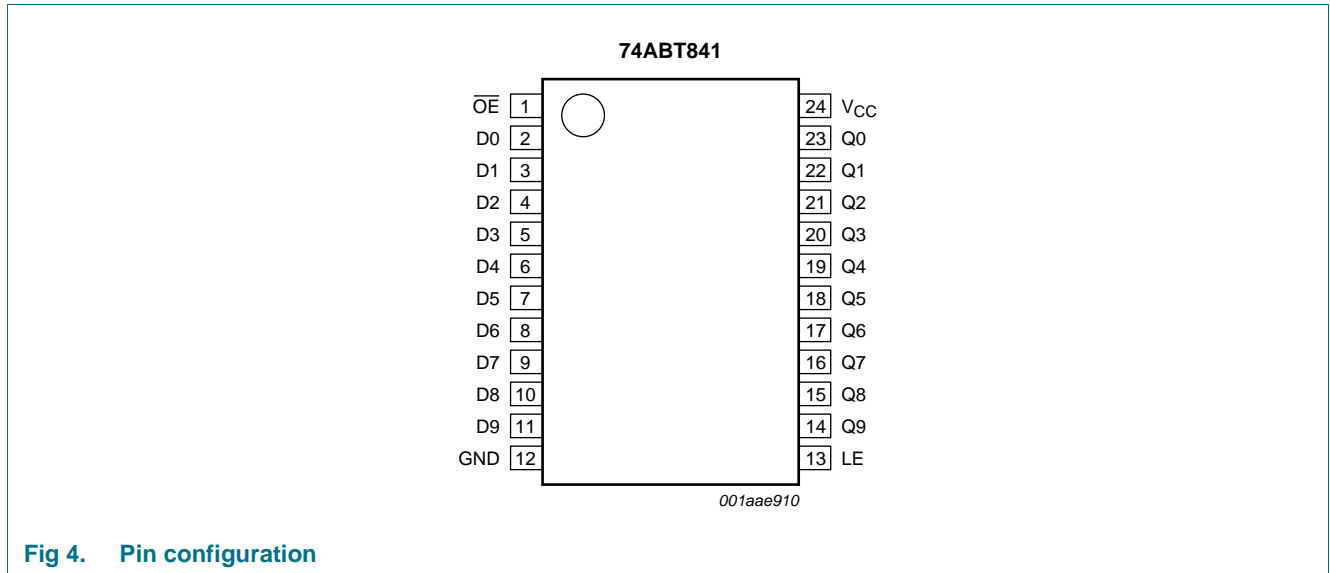
| Type number | Package | | | Version |
|-------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74ABT841D | -40 °C to +85 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| 74ABT841DB | -40 °C to +85 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| 74ABT841PW | -40 °C to +85 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--|--|
| \overline{OE} | 1 | output enable input (active LOW) |
| D0 to D9 | 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | data input |
| GND | 12 | ground (0 V) |
| LE | 13 | latch enable input (active falling edge) |
| Q0 to Q9 | 23, 22, 21, 20, 19, 18, 17, 16, 15, 14 | data output |
| V_{CC} | 24 | positive supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | Output | Operating mode |
|-------|----|----|----------|----------------|
| OE | LE | nD | Q0 to Q9 | |
| L | H | L | L | transparent |
| L | H | H | H | |
| L | ↓ | l | L | latched |
| L | ↓ | h | H | |
| H | X | X | Z | high-impedance |
| L | L | X | NC | hold |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition;
 ↓ = HIGH-to-LOW clock transition;
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|---------------------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | ^[1] -1.2 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | ^[1] -0.5 | +5.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -18 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| T_j | junction temperature | | ^[2] - | 150 | °C |
| T_{stg} | storage temperature | | -65 | +150 | °C |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------|-----|-----|----------|------|
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | -32 | - | - | mA |
| I_{OL} | LOW-level output current | | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 5 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

9. Static characteristics

Table 6. Static characteristics

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit | |
|----------------|------------------------------------|--|-------|-------|------|------------------|------|------|----|
| | | | Min | Typ | Max | Min | Max | | |
| V_{IK} | input clamping voltage | $V_{CC} = 4.5\text{ V}; I_{IK} = -18\text{ mA}$ | -1.2 | -0.9 | - | -1.2 | - | V | |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IL}$ or V_{IH} | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}; I_{OH} = -3\text{ mA}$ | 2.5 | 3.5 | - | 2.5 | - | V | |
| | | $V_{CC} = 5.0\text{ V}; I_{OH} = -3\text{ mA}$ | 3.0 | 4.0 | - | 3.0 | - | V | |
| | | $V_{CC} = 4.5\text{ V}; I_{OH} = -32\text{ mA}$ | 2.0 | 2.6 | - | 2.0 | - | V | |
| V_{OL} | LOW-level output voltage | $V_{CC} = 4.5\text{ V}; I_{OL} = 64\text{ mA}; V_I = V_{IL}$ or V_{IH} | - | 0.42 | 0.55 | - | 0.55 | V | |
| $V_{OL(pu)}$ | power-up LOW-level output voltage | $V_{CC} = 5.5\text{ V}; I_O = 1\text{ mA}; V_I = \text{GND}$ or V_{CC} | [1] | - | 0.13 | 0.55 | - | 0.55 | V |
| I_I | input leakage current | $V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or 5.5 V | | | | | | | |
| | | control pins | - | ±0.01 | ±1.0 | - | ±1.0 | μA | |
| | | data pins | - | ±5 | ±100 | - | ±100 | μA | |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}; V_I$ or $V_O \leq 4.5\text{ V}$ | - | ±5.0 | ±100 | - | ±100 | μA | |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} = 2.0\text{ V}; V_O = 0.5\text{ V}; V_I = \text{GND}$ or $V_{CC}; \overline{\text{OE}}\text{n HIGH}$ | [2] | - | ±5.0 | ±50 | - | ±50 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 5.5\text{ V}; V_I = V_{IL}$ or V_{IH} | | | | | | | |
| | | $V_O = 2.7\text{ V}$ | - | 5.0 | 50 | - | 50 | μA | |
| | | $V_O = 0.5\text{ V}$ | - | -5.0 | -50 | - | -50 | μA | |
| I_{LO} | output leakage current | HIGH-state; $V_O = 5.5\text{ V}; V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or V_{CC} | - | 5.0 | 50 | - | 50 | μA | |
| I_O | output current | $V_{CC} = 5.5\text{ V}; V_O = 2.5\text{ V}$ | [3] | -180 | -100 | -50 | -180 | -50 | mA |

Table 6. Static characteristics ...continued

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit | |
|------------------|---------------------------|--|-------|-----|-----|------------------|-----|------|----|
| | | | Min | Typ | Max | Min | Max | | |
| I _{CC} | supply current | V _{CC} = 5.5 V; V _I = GND or V _{CC} | | | | | | | |
| | | outputs HIGH-state | - | 0.5 | 250 | - | 250 | μA | |
| | | outputs LOW-state | - | 25 | 38 | - | 38 | mA | |
| | | outputs disabled | - | 0.5 | 250 | - | 250 | μA | |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 5.5 V; one input at 3.4 V; other inputs at V _{CC} or GND | [4] | - | 0.5 | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | V _I = 0 V or V _{CC} | - | 4 | - | - | - | pF | |
| C _O | output capacitance | outputs disabled; V _O = 0 V or V _{CC} | - | 7 | - | - | - | pF | |

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

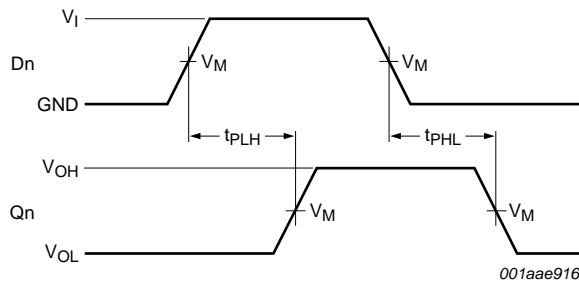
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see [Figure 9](#).

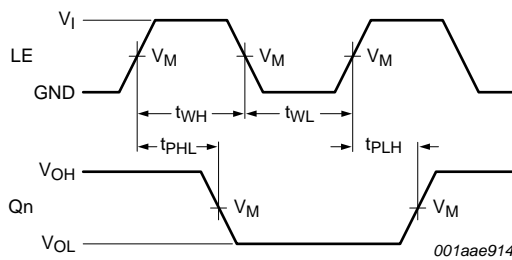
| Symbol | Parameter | Conditions | 25 °C; V _{CC} = 5.0 V | | | -40 °C to +70 °C; V _{CC} = 5.0 V ± 0.5 V | | Unit |
|--------------------|-------------------------------------|---|--------------------------------|------|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | LOW to HIGH propagation delay | Dn to Qn; see Figure 5 | 2.1 | 4.1 | 5.5 | 2.1 | 6.2 | ns |
| | | LE to Qn; see Figure 6 | 2.1 | 4.1 | 5.9 | 2.1 | 6.5 | ns |
| t _{PHL} | HIGH to LOW propagation delay | Dn to Qn; see Figure 5 | 2.0 | 4.0 | 5.5 | 2.0 | 6.2 | ns |
| | | LE to Qn; see Figure 6 | 2.8 | 4.6 | 6.2 | 2.8 | 6.7 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | \overline{OE} to Qn; see Figure 7 | 1.0 | 3.0 | 4.5 | 1.0 | 5.3 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | \overline{OE} to Qn; see Figure 7 | 2.2 | 4.1 | 5.6 | 2.2 | 6.3 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | \overline{OE} to Qn; see Figure 7 | 2.7 | 4.7 | 6.2 | 2.7 | 7.1 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | \overline{OE} to Qn; see Figure 7 | 2.8 | 4.6 | 6.1 | 2.8 | 6.5 | ns |
| t _{su(H)} | set-up time HIGH | Dn to LE; see Figure 8 | 2.5 | 1.0 | - | 2.5 | - | ns |
| t _{su(L)} | set-up time LOW | Dn to LE; see Figure 8 | 1.5 | 0 | - | 1.5 | - | ns |
| t _{h(H)} | hold time HIGH | Dn to LE; see Figure 8 | 1.5 | 0.2 | - | 1.5 | - | ns |
| t _{h(L)} | hold time LOW | Dn to LE; see Figure 8 | +1.0 | -0.8 | - | 1.0 | - | ns |
| t _{WH} | pulse width HIGH | LE; see Figure 6 | 3.3 | 1.9 | - | 3.3 | - | ns |
| t _{WL} | pulse width LOW | LE; see Figure 6 | 3.3 | 1.9 | - | 3.3 | - | ns |

11. Waveforms



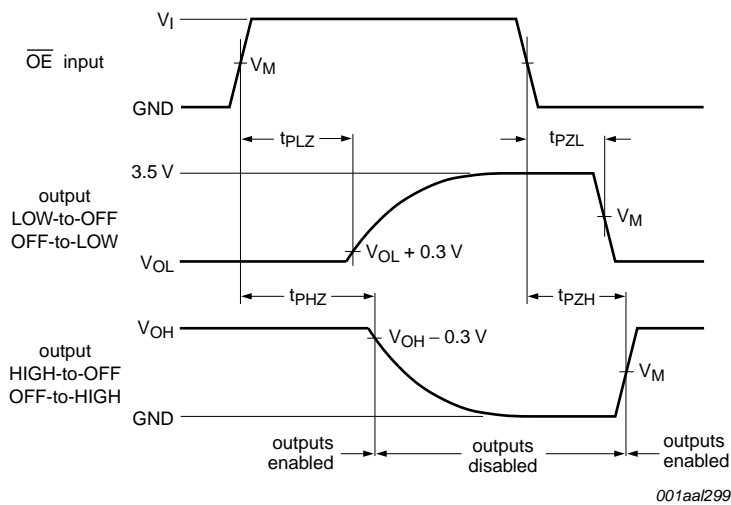
$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay for data to output



$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay, latch enable input to output and enable pulse width



$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. 3-state output (Qn) enable and disable times

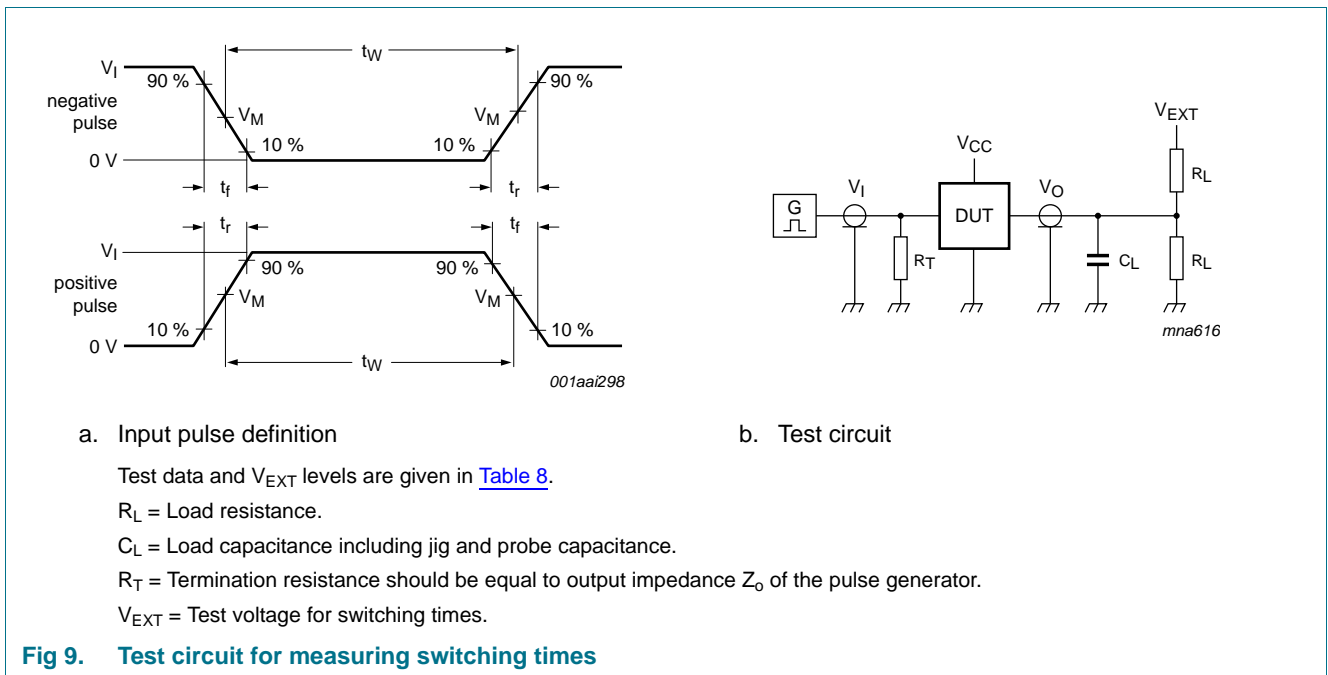
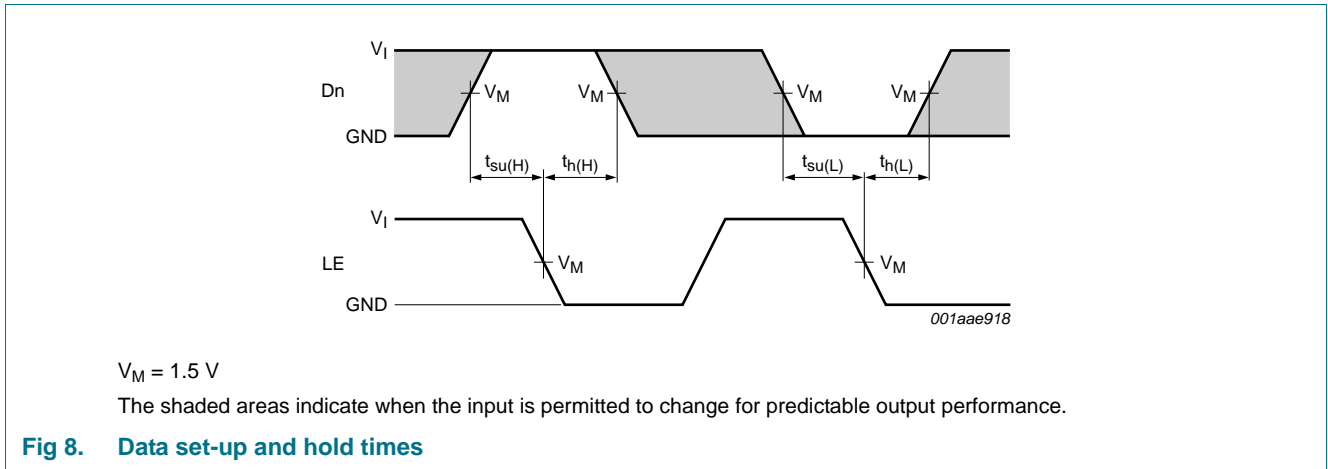


Table 8. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|-------|--------|----------------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_I | t_w | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 3.0 V | 1 MHz | 500 ns | $\leq 2.5\text{ ns}$ | 50 pF | 500 Ω | open | open | 7.0 V |

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

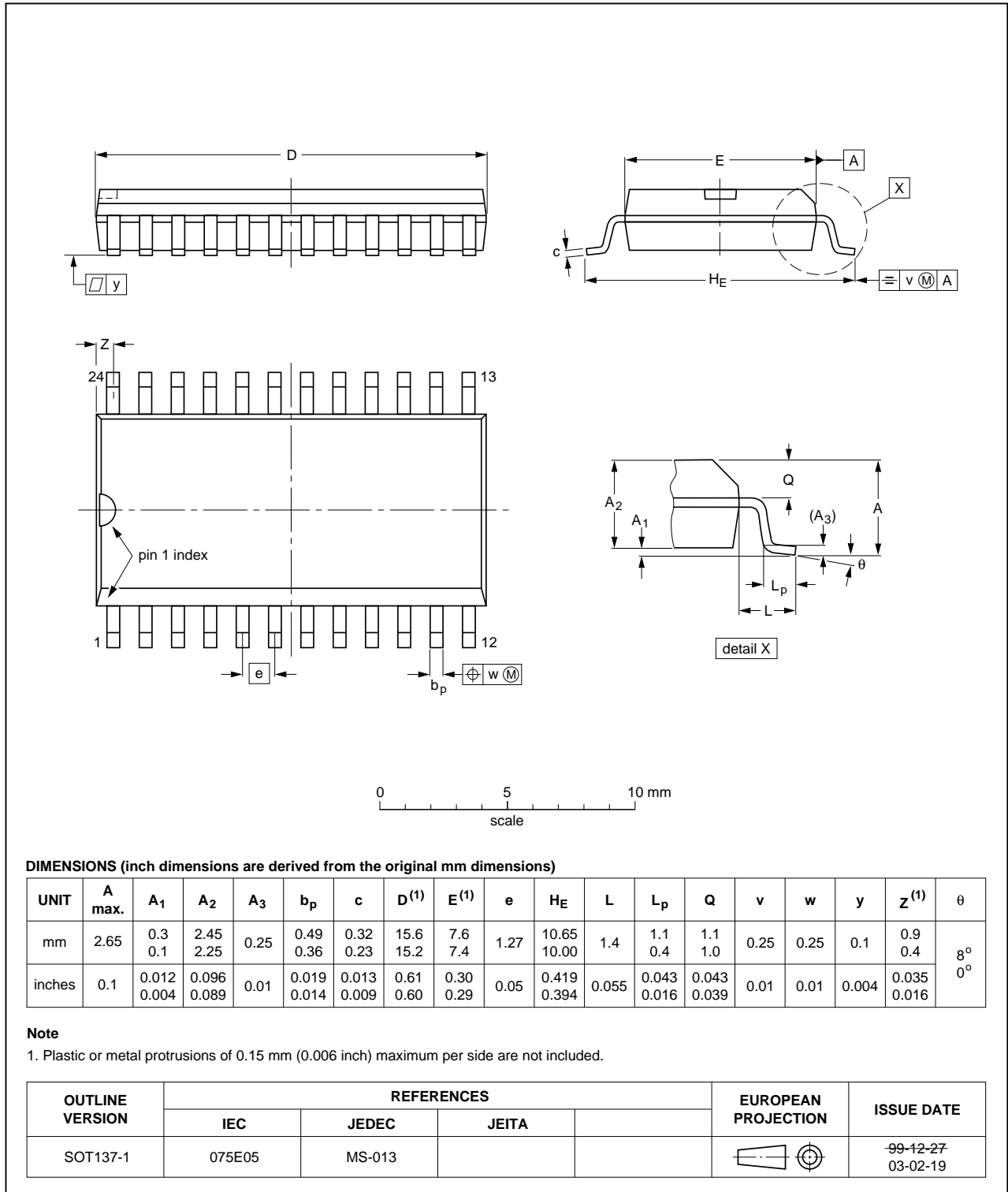


Fig 10. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

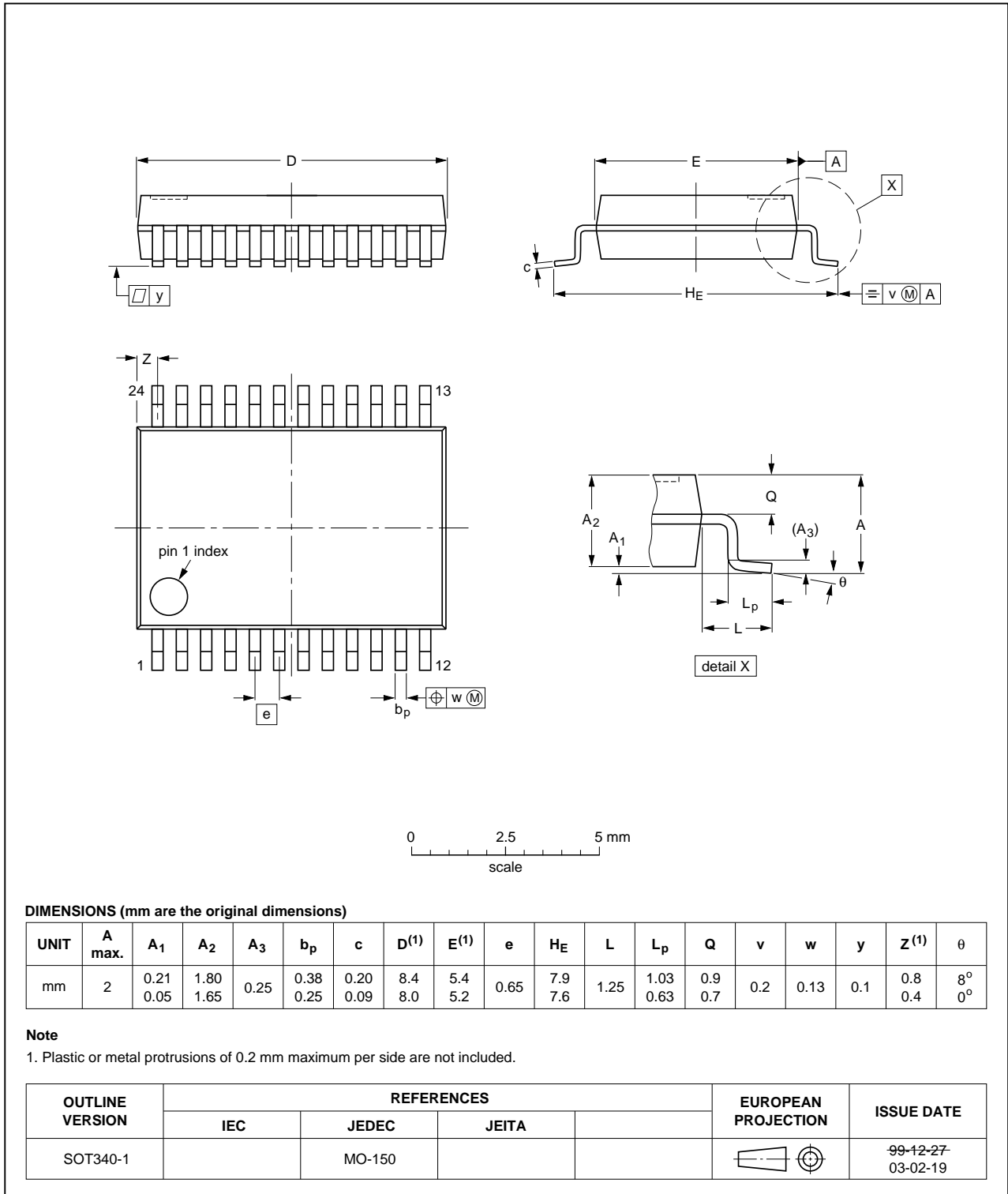


Fig 11. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

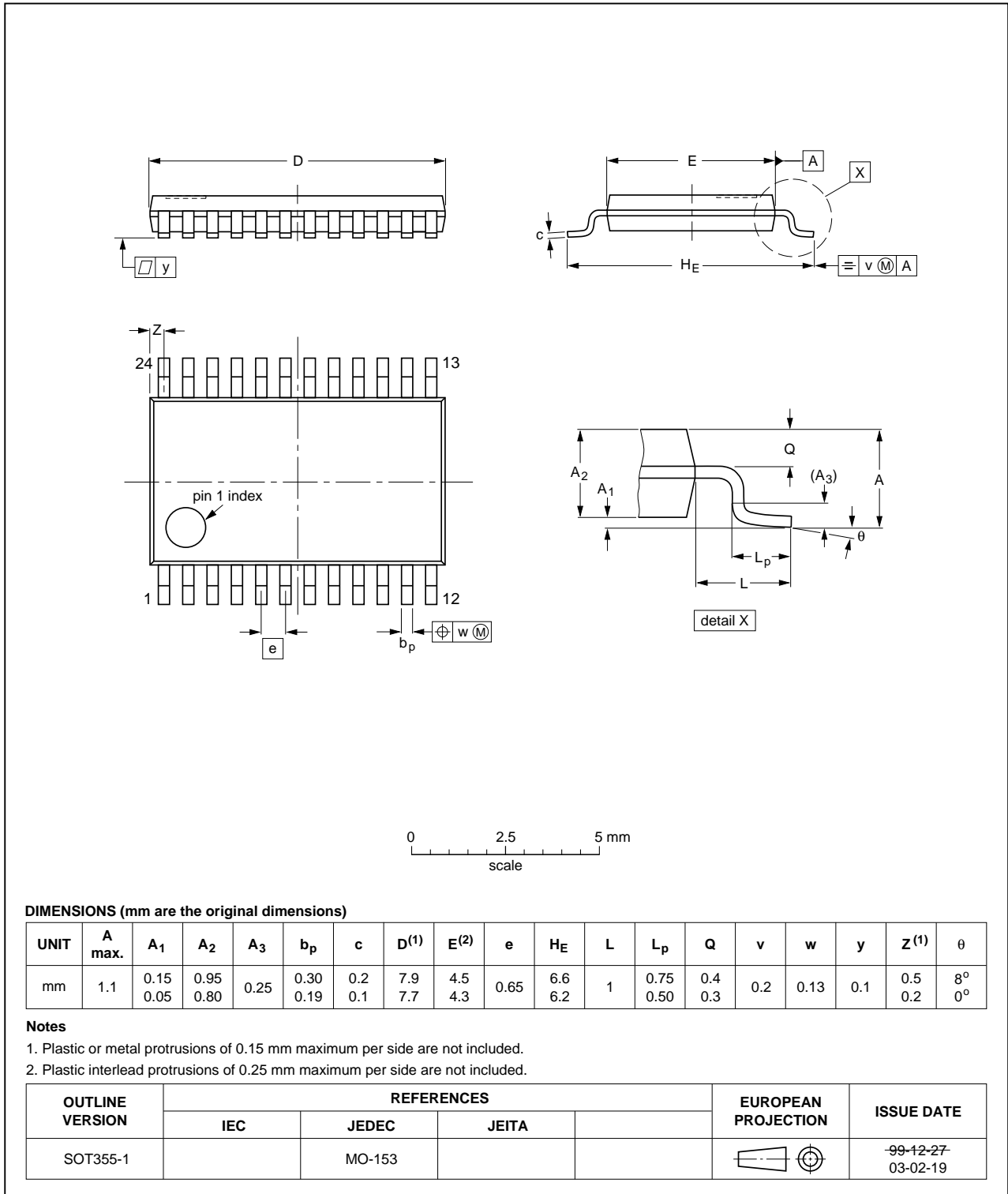


Fig 12. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|--------------|
| 74ABT841 v.4 | 20111107 | Product data sheet | - | 74ABT841 v.3 |
| Modifications: | <ul style="list-style-type: none">Legal pages updated. | | | |
| 74ABT841 v.3 | 20100325 | Product data sheet | - | 74ABT841 v.2 |
| 74ABT841 v.2 | 20100302 | Product data sheet | - | 74ABT841 |
| 74ABT841 | 19950906 | Product specification | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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