THE DATASHEET OF

S25FL164K0XMFIS11

www.win-source.net 0086-755-83957316

S25FL116K/S25FL132K/S25FL164K

16-Mbit (2 Mbyte)/32-Mbit (4 Mbyte)/ 64-Mbit (8 Mbyte), 3.0 V, SPI Flash Memory

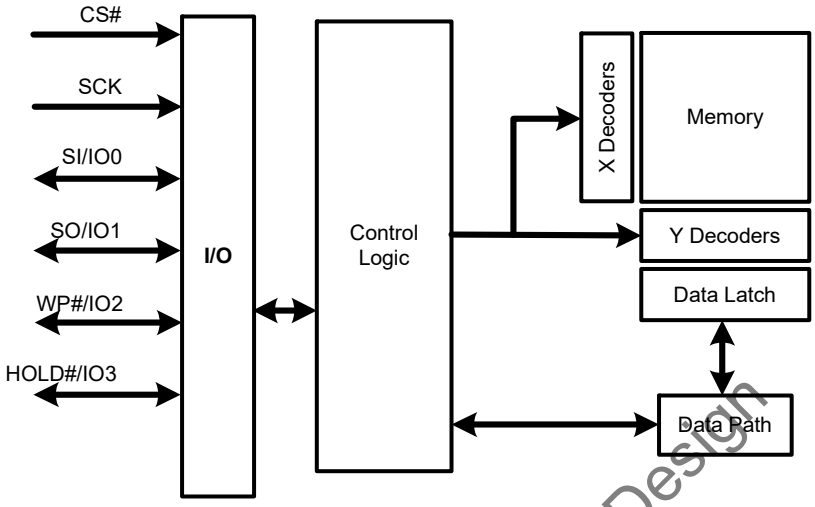
This product family has been retired and is not recommended for designs. For new and current designs, S25FL064L supersede the S25FL1-K family. These are the factory-recommended migration paths. Please refer to the S25FL-L Family datasheets for specifications and ordering information.

Features

- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Command subset and footprint compatible with S25FL-K
- Read
  - Normal Read (Serial):
    - 50 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Fast Read (Serial):
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Dual Read:
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Quad Read:
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - 54 MB/s maximum continuous data transfer rate (–40 °C to +85 °C/105 °C)
  - Efficient Execute-In-Place (XIP)
  - Continuous and wrapped read modes
  - Serial Flash Discoverable Parameters (SFDP)
- Program
  - Serial-input Page Program (up to 256 bytes)
  - Program Suspend and Resume
- Erase
  - Uniform sector erase (4 kB)
  - Uniform block erase (64 kB)
  - Chip erase
  - Erase Suspend and Resume
- Cycling Endurance
  - 100K Program-Erase cycles, minimum
- Data Retention
  - 20-year data retention, minimum
- Security
  - Three 256-byte Security Registers with OTP protection
  - Low supply voltage protection of the entire memory
  - Pointer-based security protection feature (**S25FL132K and S25FL164K**)
  - Top / Bottom relative Block Protection Range, 4 kB to all of memory
  - 8-Byte Unique ID for each device
  - Nonvolatile Status Register bits control protection modes
    - Software command protection
    - Hardware input signal protection
    - Lock-Down until power cycle protection
    - OTP protection of security registers
- 90 nm Floating Gate Technology
- Single Supply Voltage
  - 2.7 V to 3.6 V (Industrial, Industrial Plus, and Extended temperature range)
  - 2.6 V to 3.6 V (Extended temperature range)
- Temperature Ranges
  - Industrial (–40 °C to +85 °C)
  - Industrial Plus (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)
- Package Options
  - **S25FL116K**
    - 8-lead SOIC (150 mil) – SOA008
    - 8-lead SOIC (208 mil) – SOC008
    - 8-contact WSON 5 mm x 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024
    - KGD / KGW
  - **S25FL132K**
    - 8-lead SOIC (150 mil) – SOA008
    - 8-lead SOIC (208 mil) – SOC008
    - 8-contact USON 4 mm × 4 mm – UNF008
    - 8-contact WSON 5 mm × 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024
    - KGD / KGW
  - **S25FL164K**
    - 8-lead SOIC (208 mil) – SOC008
    - 16-lead SOIC (300 mil) – SO3016
    - 8-contact WSON 5 mm × 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024

Not Recommended for New Design

Logic Block Diagram



Performance Summary

Maximum Read Rates (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6.25
Fast Read	108	13.5
Dual Read	108	27
Quad Read	108	54

Typical Program and Erase Rates (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Operation	kbytes/s
Page Programming (256-byte page buffer)	365
4-kbyte Sector Erase	81
64-kbyte Sector Erase	131

Typical Current Consumption (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Operation	Current (mA)
Serial Read 50 MHz	7
Serial Read 108 MHz	12
Dual Read 108 MHz	14
Quad Read 108 MHz	16
Program	20
Erase	20
Standby	0.015
Deep-Power Down	0.002

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1. General Description

The S25FL1-K of nonvolatile flash memory devices connect to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial protocols. This multiple width interface is called SPI Multi-I/O or MIO.

The SPI-MIO protocols use only 4 to 6 signals:

- Chip Select (CS#)
- Serial Clock (SCK)
  - IO0 (SI)
  - IO1 (SO)
  - IO2 (WP#)
  - IO3 (HOLD#)
- Serial Data

The SIO protocol uses Serial Input (SI) and Serial Output (SO) for data transfer. The DIO protocols use IO0 and IO1 to input or output two bits of data in each clock cycle.

The Write Protect (WP#) input signal option allows hardware control over data protection. Software controlled commands can also manage data protection.

The HOLD# input signal option allows commands to be suspended and resumed on any clock cycle.

The QIO protocols use all of the data signals (IO0 to IO3) to transfer 4 bits in each clock cycle. When the QIO protocols are enabled the WP# and HOLD# inputs and features are disabled.

Clock frequency of up to 108 MHz is supported, allowing data transfer rates up to:

- Single bit data path = 13.5 Mbytes/s
- Dual bit data path = 27 Mbytes/s
- Quad bit data path = 54 Mbytes/s

Executing code directly from flash memory is often called Execute-in-Place or XIP. By using S25FL1-K devices at the higher clock rates supported, with QIO commands, the command read transfer rate can match or exceed traditional x8 or x16 parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically. The Continuous Read Mode allows for random memory access with as few as 8 clocks of overhead for each access, providing efficient XIP operation. The Wrapped Read mode provides efficient instruction or data cache refill via a fast read of the critical byte that causes a cache miss, followed by reading all other bytes in the same cache line in a single read command.

The S25FL1-K:

- Support JEDEC standard manufacturer and device type identification.
- Program pages of 256 bytes each. One to 256 bytes can be programmed in each Page Program operation. Pages can be erased in groups of 16 (4-kB aligned sector erase), groups of 256 (64-kB aligned block erase), or the entire chip (chip erase).
- The S25FL1-K devices operate on a single 2.6 V/2.7 V to 3.6 V power supply and all devices are offered in space-saving packages.
- Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

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1.1 Migration Notes

1.1.1 Features Comparison

The S25FL1-K is command set and footprint compatible with prior generation FL-K and FL-P families.

FL Generations Comparison

Parameter	S25FL1-K	S25FL-K	S25FL-P
Technology Node	90 nm	90 nm	90 nm
Architecture	Floating Gate	Floating Gate	MirrorBit®
Release Date	In Production	In Production	In Production
Density	16 Mbit - 64 Mbit	4 Mbit - 128 Mbit	32 Mbit - 256 Mbit
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.6 V / 2.7 V - 3.6 V	2.7 V - 3.6 V	2.7 V - 3.6 V
Normal Read Speed	6 MB/s (50 MHz)	6 MB/s (50 MHz)	5 MB/s (40 MHz)
Fast Read Speed	13.5 MB/s (108 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed	27 MB/s (108 MHz)	26 MB/s (104 MHz)	20 MB/s (80 MHz)
Quad Read Speed	54 MB/s (108 MHz at 85°C/105°C)	52 MB/s (104 MHz)	40 MB/s (80 MHz)
Program Buffer Size	256B	256B	256B
Page Programming Time (typ.)	700 µs (256B)	700 µs (256B)	1500 µs (256B)
Program Suspend / Resume	Yes	Yes	No
Erase Sector Size	4 kB / 64 kB	4 kB / 32 kB / 64 kB	64 kB / 256 kB
Parameter Sector Size	N/A	N/A	4 kB
Sector Erase Time (typ.)	50 ms (4 kB), 500 ms (64 kB)	30 ms (4 kB), 150 ms (64 kB)	500 ms (64 kB)
Erase Suspend / Resume	Yes	Yes	No
OTP Size	768B (3 x 256B)	768B (3 x 256B)	506B
Operating Temperature	-40°C to +85°C / +105°C	-40°C to +85°C	-40°C to +85°C / +105°C

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Notes:

1. *S25FL-K family devices can erase 4-kB sectors in groups of 32 kB or 64 kB.*
2. *S25FL1-K family devices can erase 4-kB sectors in groups of 64 kB.*
3. *S25FL-P has either 64-kB or 256-kB uniform sectors depending on an ordering option.*
4. *Refer to individual data sheets for further details.*

1.1.2 Known Feature Differences from Prior Generations

1.1.2.1 Secure Silicon Region (OTP)

The size and format (address map) of the OTP area is the same for the S25FL1-K and the S25FL-K but different for the S25FL-P.

1.1.2.2 Commands Not Supported

The following S25FL-K and S25FL-P commands are not supported:

- Quad Page PGM (32h)
- Half-Block Erase 32K (52h)
- Word read Quad I/O (E7)
- Octal Word Read Quad I/O (E3h)
- MFID dual I/O (92h)
- MFID quad I/O (94h)
- Read Unique ID (4Bh)

1.1.2.3 New Features

The S25FL1-K introduces new features to low density SPI category memories:

- Variable read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands
- Industrial Plus and Extended temperature range
- Volatile configuration option in addition to legacy nonvolatile configuration

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1.2 Glossary

- **Command.** All information transferred between the host system and memory during one period while CS# is low. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
- **Flash**. The name for a type of Electrical Erase Programmable Read Only Memory (EEPROM) that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
- **High**. A signal voltage level ≥ V_{IH} or a logic level representing a binary one (1).
- **Instruction**. The 8-bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
- **Low**. A signal voltage level ≤ V_{IL} or a logic level representing a binary zero (0).
- **LSB**. Least Significant Bit. Generally the right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
- **MSB**. Most Significant Bit. Generally the left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
- **nonvolatile**. No power is needed to maintain data stored in the memory.
- **OPN**. Ordering Part Number. The alphanumeric string specifying the memory device type, density, package, factory nonvolatile configuration, etc. used to select the desired device.
- **Page**. 256-byte aligned and length group of data.
- **PCB**. Printed Circuit Board.
- **Register Bit References**. Are in the format: Register_name[bit_number] or Register_name[bit_range_MSB: bit_range_LSB].
- **Sector**. Erase unit size; all sectors are physically 4-kbytes aligned and length. Depending on the erase command used, groups of physical sectors may be erased as a larger logical sector of 64 kbytes.
- **Write**. An operation that changes data within volatile or nonvolatile registers bits or nonvolatile flash memory. When changing nonvolatile data, an erase and reprogramming of any unchanged nonvolatile data is done, as part of the operation, such that the nonvolatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The nonvolatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

1.3 Other Resources

1.3.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

1.3.2 Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

1.3.3 Links to Application Notes

www.cypress.com/cypressappnotes

2. Hardware Interface

2.1 Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increases power consumption due to so many signals switching and the larger package increases cost.

The S25FL1-K reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FL1-K uses the industry standard single bit SPI and also supports commands for 2-bit (Dual) and 4-bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

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3. Signal Descriptions

3.1 Input / Output Summary

Table 1. Signal List

Signal Name	Type	Description
SCK	Input	**Serial Clock.**
CS#	Input	**Chip Select.**
SI (IO0)	I/O	**Serial Input** for single bit data commands. IO0 for Dual or Quad commands.
SO (IO1)	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# (IO2)	I/O	**Write Protect** in single bit or Dual data commands. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# (IO3)	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core and I/O Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Note

1. A signal name ending with the # symbol is active when low.

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3.2 Address and Data Configuration

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the SI signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Output commands send information from the host to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands send information from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK.

3.4 Chip Select (CS#)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the CS# input to logic low state enables the device, placing it in the Active Power mode. After Power-Up, a falling edge on CS# is required prior to the start of any command.

3.5 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.6 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1, an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.7 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC, and CMP bits in the status registers, are also hardware protected against data modification while WP# remains Low.

The WP# function is not available when the Quad mode is enabled (QE) in Status Register-2 (SR2[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode.

3.8 HOLD# / IO3

The HOLD# signal is used to pause any serial communications with the device without deselecting the device or stopping the serial clock.

To enter the Hold condition, the device must be selected by driving the CS# input to the logic low state. It is required that the user keep the CS# input low state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic low state. If the falling edge does not coincide with the SCK signal being at the logic low state, the Hold condition starts whenever the SCK signal reaches the logic low state. Taking the HOLD# signal to the logic low state does not terminate any Write, Program or Erase operation that is currently in progress.

During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care.

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic low state. If the rising edge does not coincide with the SCK signal being at the logic low state, the Hold condition ends whenever the SCK signal reaches the logic low state.

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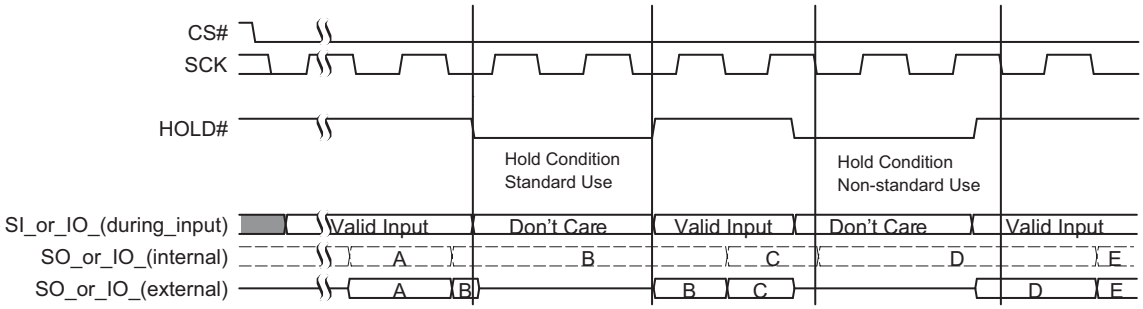
Figure 3.1 Hold Condition



3.9 Core and I/O Signal Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic and input / output signals. It is the single voltage used for all device functions including read, program, and erase.

3.10 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.11 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

3.12 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but is there potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.13 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

3.14 Block Diagrams

Figure 1. Bus Master and Memory Devices on the SPI Bus – Single Bit Data Path

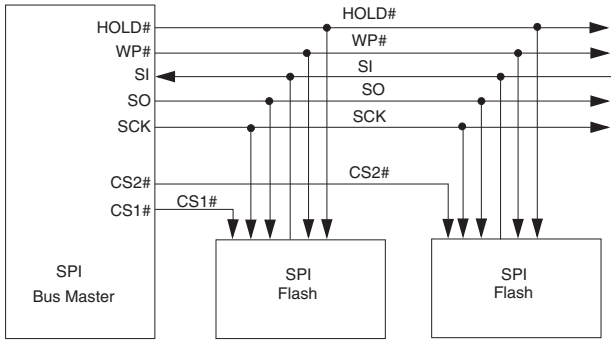


Figure 2. Bus Master and Memory Devices on the SPI Bus – Dual Bit Data Path

Not Recommended for New Design

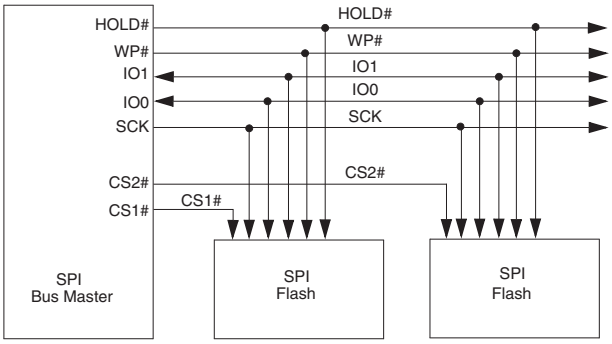
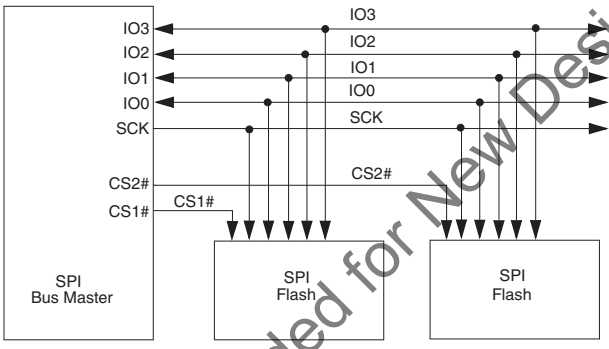


Figure 3. Bus Master and Memory Devices on the SPI Bus – Quad Bit Data Path



Not Recommended for New Design

4. Signal Protocols

4.1 SPI Clock Modes

The S25FL1-K can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

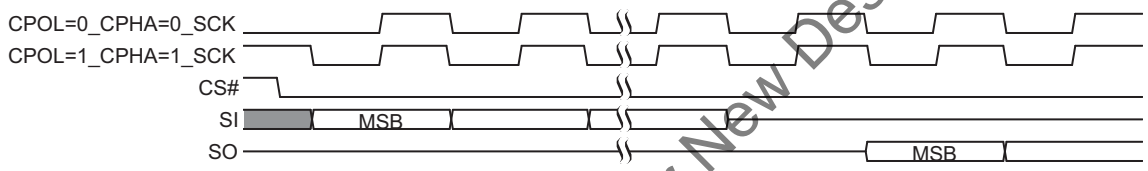
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 4. SPI Modes Supported



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Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with SCK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

4.2 Command Protocol

All communication between the host system and S25FL1-K memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier (mode), latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal.

Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal.

Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address is a 24-bit, byte boundary, address. The address transfers occur on SCK rising edge.
- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in 2-bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. SIngle bits or parallel bit groups are transferred in most to least significant bit order.
- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of clock cycles after CS# signal was driven low is an exact multiple of eight cycles. If the CS# signal does not go high exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the most significant bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

Not Recommended for New Design

4.2.1 Command Sequence Examples

Figure 5. Stand Alone Instruction Command

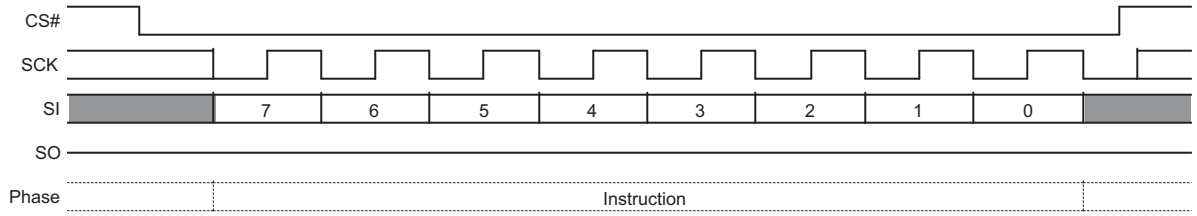
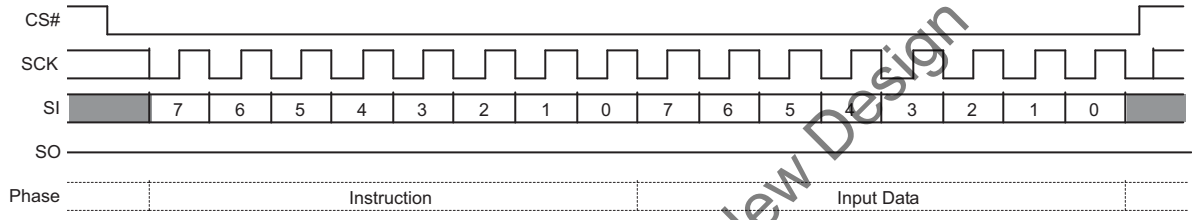


Figure 6. Single Bit Wide Input Command



Not Recommended for New Design

Figure 7. Single Bit Wide Output Command

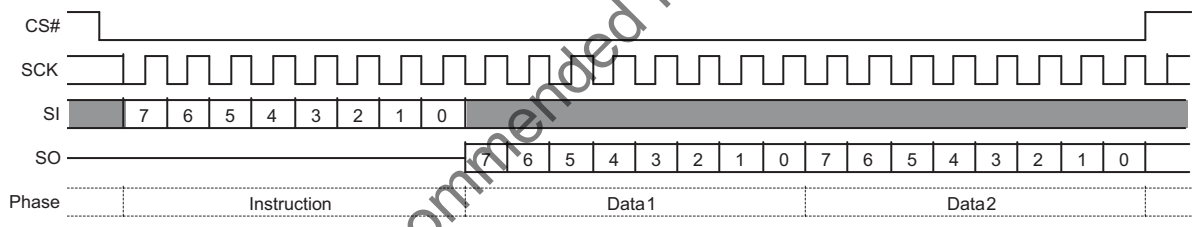


Figure 8. Single Bit Wide I/O Command without Latency

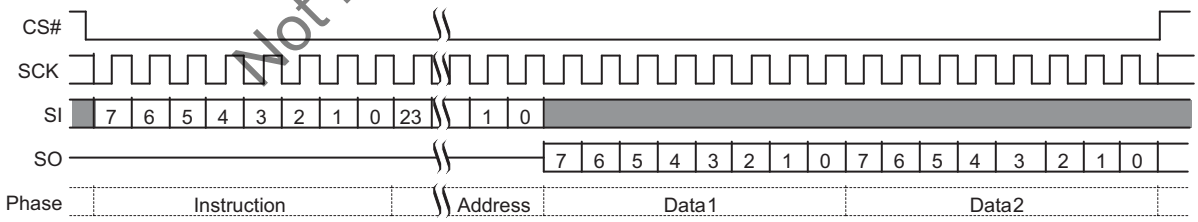


Figure 9. Single Bit Wide I/O Command with Latency

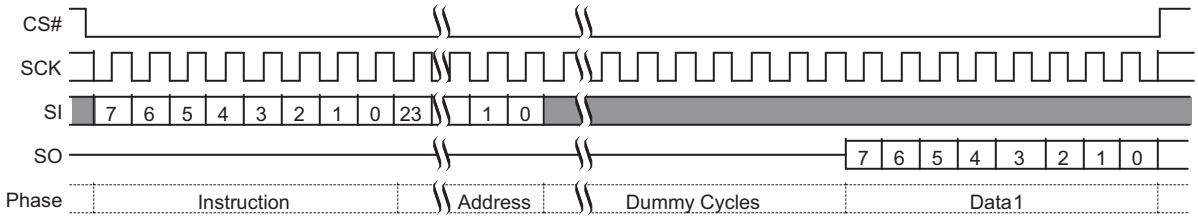


Figure 10. Dual Output Command

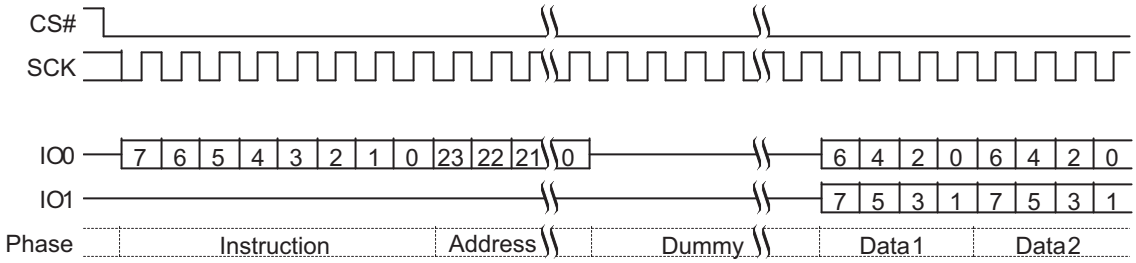
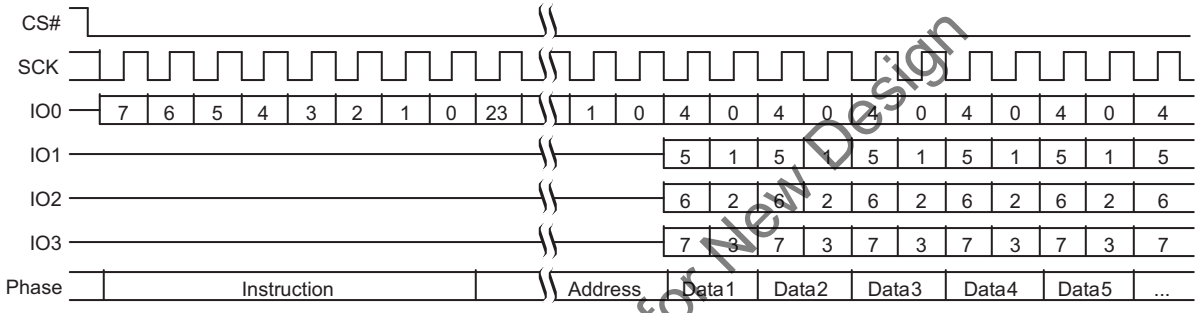


Figure 11. Quad Output Command without Latency



Not Recommended for New Design

Figure 12. Dual I/O Command

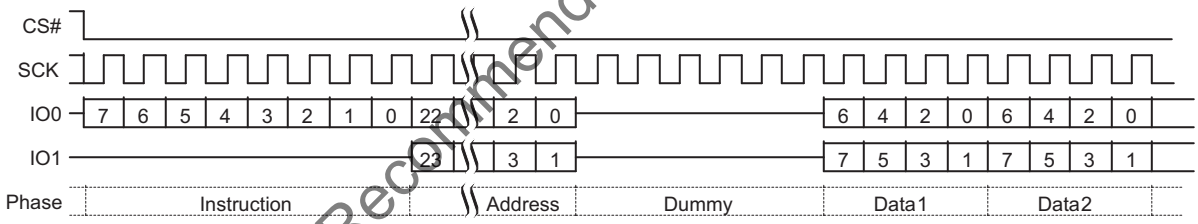
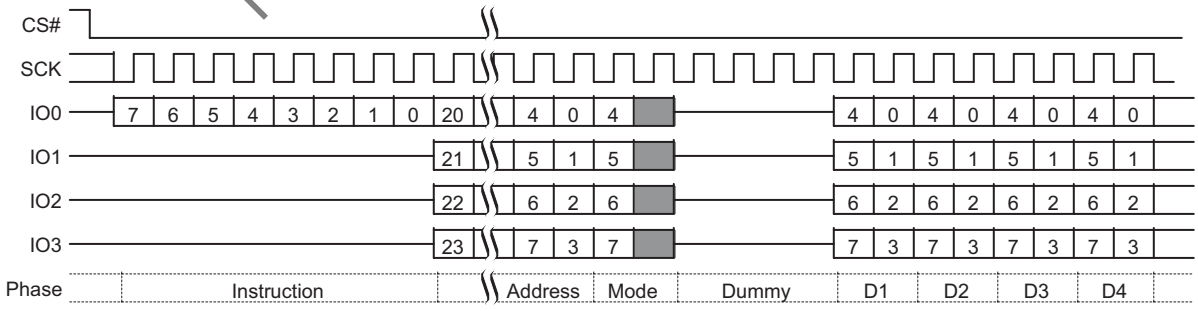


Figure 13. Quad I/O Command



Additional sequence diagrams, specific to each command, are provided in Section 10. Commands on page 63.

4.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 2. Interface States Summary

Interface State	V_{CC}	SCK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Low Power Hardware Data Protection	< V_{WI}	X	X	X	X	Z	X
Power-On (Cold) Reset	≥ V_{CC} (min)	X	HH	X	X	Z	X
Interface Standby	≥ V_{CC} (min)	X	X	X	X	Z	X
Instruction Cycle	≥ V_{CC} (min)	HT	HL	HH	HV	Z	HV
Hold Cycle	≥ V_{CC} (min)	HV or HT	HL	HL	X	X	X
Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	MV	MV	MV	MV

Legend:

Z = no driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = either HL or HH
X = HL or HH or Z
HT = toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = either ML or MH

Not Recommended for New Design

4.3.1 Low Power Hardware Data Protection

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.3.2 Power-On (Cold) Reset

When the core voltage supply remains at or below the $V_{CC\ (Low)}$ voltage for > t_{PD} time, then rises to ≥ V_{WI} the device will begin its Power-On-Reset (POR) process. POR continues until the end of t_{PUW}. During t_{PUW} the device does not react to write commands. Following the end of t_{PUW} the device transitions to the Interface Standby state and can accept write commands. For additional information on POR see Section 5.7 Power-On (Cold) Reset on page 25.

4.3.3 Interface Standby

When CS# is high the SPI interface is in standby state. Inputs are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

4.3.4 Instruction Cycle

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# low, HOLD# high, and drives Write Protect (WP#) signal as needed for the instruction. However, WP# is only relevant during instruction cycles of a Write Status Registers command and is otherwise ignored.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual output, Quad output, Dual I/O, or Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

4.3.5 Hold

When Quad mode is not enabled (SR2[1]=0) the HOLD# / IO3 signal is used as the HOLD# input. The host keeps HOLD# low, SCK may be at a valid level or continue toggling, and CS# is low. When HOLD# is low a command is paused, as though SCK were held low. SI / IO0 and SO / IO1 ignore the input level when acting as inputs and are high impedance when acting as outputs during hold state. Whether these signals are input or output depends on the command and the point in the command sequence when HOLD# is asserted low.

When HOLD# returns high the next state is the same state the interface was in just before HOLD# was asserted low.

4.3.6 Single Input Cycle — Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The dual output, and quad output commands send address to the memory using only SI but return read data using the I/O signals. The host keeps CS# low, HOLD# high, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output.

4.3.7 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. In dual or quad read commands, the host must stop driving the I/O signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving I/O signals during latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

4.3.8 Single Output Cycle — Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

Not Recommended for New Design

4.3.9 Dual Input Cycle — Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps CS# low, HOLD# high. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

4.3.10 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave
SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

4.3.11 Dual Output Cycle — Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

4.3.12 Quad Input Cycle — Host to Memory Transfer

The Read Quad I/O command transfers four address, mode, or data bits to the memory in each cycle. The host keeps CS# low, and drives the I/O signals.

For Read Quad I/O the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

4.3.13 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Control in the Status Register-3 (SR3[3:0]). During the latency cycles, the host keeps CS# low. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on I/O during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad output Cycle.

4.3.14 Quad Output Cycle — Memory to Host Transfer

The Read Quad Output and Read Quad I/O return data to the host four bits in each cycle. The host keeps CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

4.4 Status Register Effects on the Interface

The Status Register-2, bit 1 (SR2[1]), selects whether Quad mode is enabled to ignore HOLD# and WP# and allow Read Quad Output, and Read Quad I/O commands.

Not Recommended for New Design

4.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

4.5.1 Low Power

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.5.2 Power-Up

Program and erase operations continue to be prevented during the Power-Up to Write delay (t_{PUW}) because no write command is accepted until after t_{PUW}.

4.5.3 Deep Power-Down (DPD)

In DPD mode the device responds only to the Resume from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

4.5.4 Clock Pulse Count

The device verifies that all program, erase, and Write Status Registers commands consist of a clock pulse count that is a multiple of eight before executing them. A command not having a multiple of 8 clock pulse count is ignored and no error status is set for the command.

Not Recommended for New Design

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameters [2]	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}		–0.6 to +4.0	V
Voltage Applied to any Pin	V_{IO}	Relative to Ground	–0.6 to +4.0	V
Transient Voltage on any Pin	V_{IOT}	< 20 ns Transient Relative to Ground	–2.0 to 6.0	V
Storage Temperature	T_{STG}		–65 to +150	°C
Lead Temperature	T_{LEAD}		[3]	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model [4]	–2000 to +2000	V

Notes

2. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
4. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

5.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to negative V_{IOT} or overshoot to positive V_{IOT}, for periods up to 20 ns.

Figure 14. Maximum Negative Overshoot Waveform

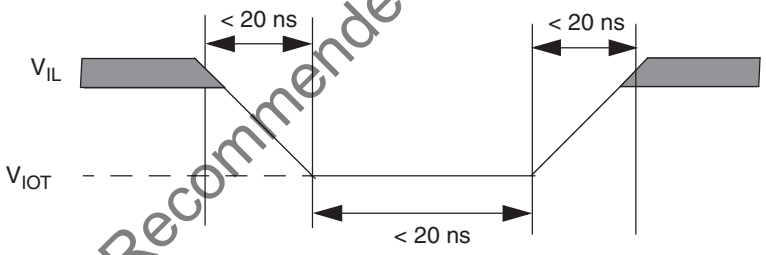
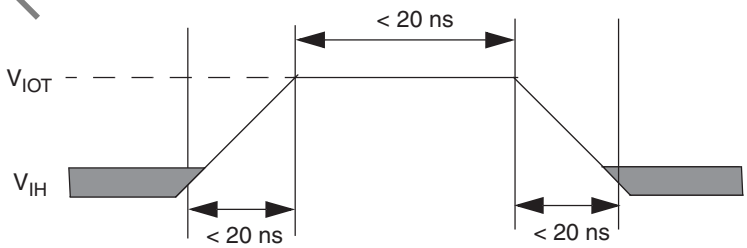


Figure 15. Maximum Positive Overshoot Waveform



Not Recommended for New Design

5.1.2 Latchup Characteristics

Table 4. Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	–1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	–1.0	V_{CC} + 1.0	V
V_{CC} Current	–100	+100	mA

Note

5. Excludes power supply V_{CC}. Test conditions: V_{CC} = 3.0V, one connection at a time tested, connections not being tested are at V_{SS}.

5.2 Thermal Resistance

Table 5. Thermal Resistance

Parameter	Description	SOA008	SOC008	FAB024	FAC024	WSON	Unit
Theta JA	Thermal resistance (junction to ambient)	75	75	39	39	18	°C/W

5.3 Operating Ranges

Operating ranges define those limits between which functionality of the device is guaranteed.

Table 6. Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial	-40	+85	°C
		Industrial Plus	-40	+105	
Supply Voltage	V_{CC}	Industrial and Industrial Plus Temp	2.7	3.6	V

Note

6. V_{CC} voltage during read can operate across the min and max range but should not exceed ± 10% of the voltage used during programming or erase of the data being read.

Not Recommended for New Design

5.4 DC Electrical Characteristics

DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max		Unit
					-40 to 85°C	-40 to 105°C	
Input Leakage	I_{LI}				±2		µA
I/O Leakage	I_{LO}				±2		µA
Standby Current	I_{CC1}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		15	25	25	µA
Deep Power-Down Current **(S25FL116K)**	I_{CC2}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		2	5	5	µA
Deep Power-Down Current **(S25FL132K / S25FL164K)**	I_{CC2}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		2	8	10	µA
Current: Read Single / Dual / Quad 1 MHz [5.4.1]	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		4 / 5 / 6	6 / 7.5 / 9	6 / 7.5 / 9	mA
Current: Read Single / Dual / Quad 33 MHz [5.4.1]	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		6 / 7 / 8	9 / 10.5 / 12	9 / 10.5 / 12	mA
Current: Read Single / Dual / Quad 50 MHz [5.4.1]	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		7 / 8 / 9	10 / 12 / 13.5	10 / 12 / 13.5	mA
Current: Read Single / Dual / Quad 108 MHz [5.4.1]	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		12 / 14 / 16	18 / 22 / 25	18 / 22 / 25	mA
Current: Write Status Registers	I_{CC4}	CS# = V_{CC}		8	12	12	mA
Current Page Program	I_{CC5}	CS# = V_{CC}		20	25	25	mA
Current Sector / Block Erase	I_{CC6}	CS# = V_{CC}		20	25	25	mA
Current Chip Erase	I_{CC7}	CS# = V_{CC}		20	25	25	mA
Input Low Voltage **(S25FL116K)**	V_{IL}		-0.5		V_{CC} x 0.2	V_{CC} x 0.2	V
Input Low Voltage **(S25FL132K / S25FL164K)**	V_{IL}		-0.5		V_{CC} x 0.3	V_{CC} x 0.3	V
Input High Voltage	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.4	V_{CC} + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA	V_{SS}		0.2	0.2	V
		I_{OL} = 1.6 mA	V_{SS}		0.4	0.4	
Output High Voltage	V_{OH}	I_{OH} = –100 µA	V_{CC} – 0.2		V_{CC}	V_{CC}	V

Not Recommended for New Design

Note

7. Tested on sample basis and specified through design and characterization data. T_A = 25°C, V_{CC} = 3V.

5.4.1 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

5.5 AC Measurement Conditions

Figure 16. Test Setup

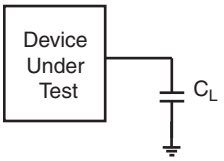


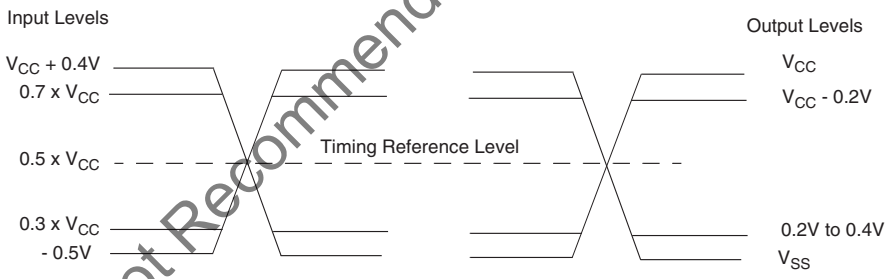
Table 7. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		2.4	ns
	Input Pulse Voltage	0.2 x V_{CC} to 0.8 V_{CC}		V
	Input Timing Ref Voltage	0.5 V_{CC}		V
	Output Timing Ref Voltage	0.5 V_{CC}		V

Notes

8. Output High-Z is defined as the point where data is no longer driven.
9. Input slew rate: 1.5 V/ns.
10. AC characteristics tables assume clock and data signals have the same slew rate (slope).

Figure 17. Input, Output, and Timing Reference Levels



Not Recommended for New Design

5.5.1 Capacitance Characteristics

Table 8. Capacitance

	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#)	1 MHz	–	8	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz	–	8	pF

Notes

11. Sampled, not 100% tested.
12. Test conditions TA = 25°C, f = 1.0 MHz.

5.6 Power-Up Timing

Table 9. Power-Up Timing and Voltage Levels

Parameter	Symbol	Spec		Unit
		Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	10	–	µs
Power-Up to Write — Time Delay Before Write Command	t_{PUW}	10	–	ms
Write Inhibit Threshold Voltage	V_{WI}	2.4	–	V
Power-Down Time	t_{PD}	10.0	–	µs
V_{CC} Power-Down Reset Threshold Voltage	V_{CC} Low	1.0	–	V

Note:
1. These parameters are characterized only.

Not Recommended for New Design

Figure 18. Power-Up Timing and Voltage Levels

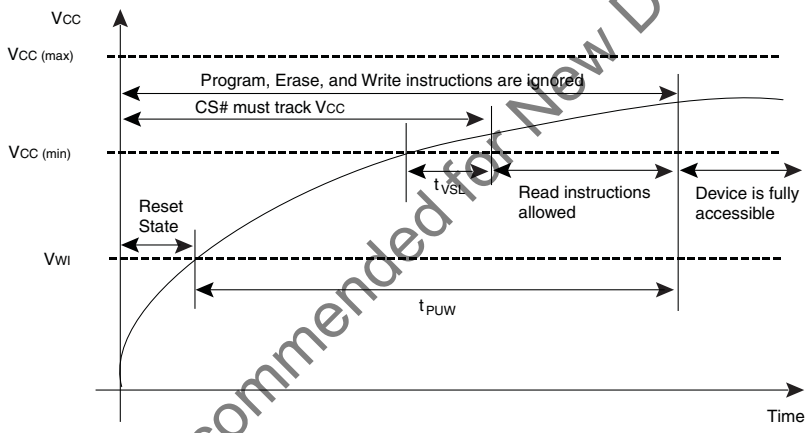
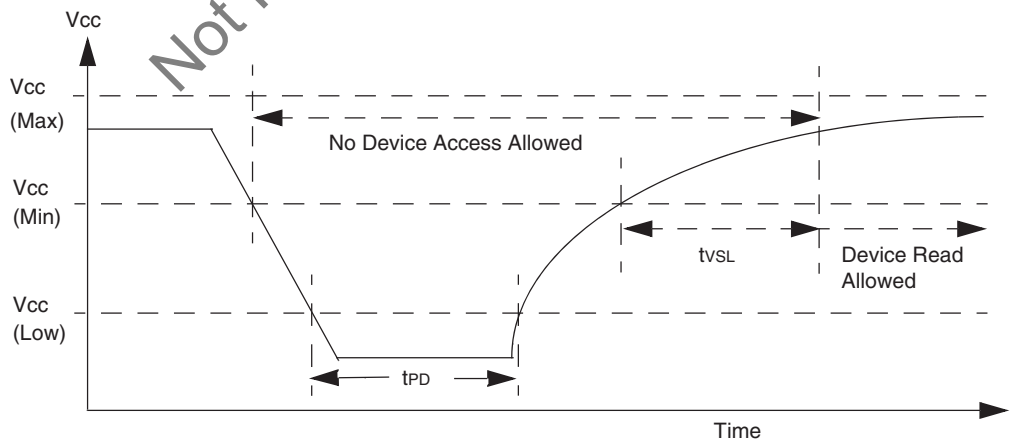


Figure 19. Power-Down and Voltage Drop



5.7 Power-On (Cold) Reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. See Figure 18 on page 24, Figure 19 on page 24, and Table on page 24. The device must not be selected (CS# to go high with V_{CC}) until after (t_{VSL}), i.e. no commands may be sent to the device until the end of t_{VSL}.

5.8 AC Electrical Characteristics

Table 10. AC Electrical Characteristics: –40°C to +85°C/105°C at 2.7V to 3.6V

Description	Symbol	Alt	Spec			Unit
			Min	Typ	Max	
Clock frequency for all SPI commands except for Read Data command (03h) and Fast Read command (0Bh) 2.7 V - 3.6V V_{CC}	F_R	f_C	D.C.	–	108	MHz
Clock frequency for Read Data command (03h)	f_R		D.C.	–	50	MHz
Clock frequency for all Fast Read commands SIO and MIO	f_{FR}		D.C.	–	108	MHz
Clock Period	P_{SCK}		9.25	–	–	ns
Clock High, Low Time for f_{FR}	t_{CLH}, t_{CLL} [13]	t_{CH}, t_{CL}	3.3	–	–	ns
Clock High, Low Time for F_R	t_{CLH}, t_{CLL} [13]	t_{CH}, t_{CL}	4.3	–	–	ns
Clock High, Low Time for f_R	t_{CRLH}, t_{CRLL} [13]	t_{CH}, t_{CL}	6	–	–	ns
Clock Rise Time	t_{CLCH} [14]	t_{CRT}	0.1	–	–	V/ns
Clock Fall Time	t_{CHCL} [14]	t_{CFT}	0.1	–	–	V/ns
CS# Active Setup Time relative to SCK	t_{SLCH}	t_{CSS}	5	–	–	ns
CS# Not Active Hold Time relative to SCK	t_{CHSL}	t_{CSH}	5	–	–	ns
Data In Setup Time	t_{DVCH}	t_{SU}	2	–	–	ns
Data In Hold Time	t_{CHDX}	t_{HD}	5	–	–	ns
CS# Active Hold Time relative to SCK	t_{CHSH}	t_{CSS}	5	–	–	ns
CS# Not Active Setup Time relative to SCK	t_{SHCH}	t_{CSH}	5	–	–	ns
CS# High Time		t_{CS}	10	–	–	ns
CS# Deselect Time (for Array Read -> Array Read)	t_{SHSL1}	t_{CS1}	7	–	–	ns
CS# Deselect Time (for Erase or Program -> Read Status Registers)	t_{SHSL2}	t_{CS2}	40	–	–	ns
Volatile Status Register Write Time			40	–	–	
CS# Deselect Time (for Erase or Program -> Suspend command)	t_{SHSL3}	t_{CS3}	130	–	–	ns
Output Disable Time	t_{SHQZ} [14]	t_{DIS}	–	–	7	ns
Clock Low to Output Valid, 30 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}	–	–	7	ns
Clock Low to Output Valid, 15 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}	–	–	6	ns
Clock Low to Output Valid (for Read ID commands) 2.7V - 3.6V	t_{CLQV2}	t_{V2}	–	–	8.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	2	–	–	ns
HOLD# Active Setup Time relative to SCK	t_{HLCH}	–	5	–	–	ns
HOLD# Active Hold Time relative to SCK	t_{CHHH}	–	5	–	–	ns
HOLD# Not Active Setup Time relative to SCK	t_{HHCH}	–	5	–	–	ns

Not Recommended for New Design

Table 10. AC Electrical Characteristics: –40°C to +85°C/105°C at 2.7V to 3.6V (Continued)

Description	Symbol	Alt	Spec			Unit
			Min	Typ	Max	
HOLD# Not Active Hold Time relative to SCK	t_{CHHL}	–	5	–	–	ns
HOLD# to Output Low-Z	t_{HHQX} [14]	t_{LZ}	–	–	7	ns
HOLD# to Output High-Z	t_{HLQZ} [14]	t_{HZ}	–	–	12	ns
Write Protect Setup Time Before CS# Low	t_{WHSL} [15]	t_{WPS}	20	–	–	ns
Write Protect Hold Time After CS# High	t_{SHWL} [15]	t_{WPH}	100	–	–	ns
CS# High to Power-down Mode	t_{DP} [14]	–	–	–	3	µs
CS# High to Standby Mode without Electronic Signature Read	t_{RES1} [14]	–	–	–	3	µs
CS# High to Standby Mode with Electronic Signature Read	t_{RES2} [14]	–	–	–	1.8	µs
CS# High to next Command after Suspend	t_{SUS} [14]	–	–	–	20	µs
Write Status Registers Time	t_W	–	–	2	30 [18]	ms
Byte Program Time (First Byte) [16][17]	t_{BP1}	–	–	15	50	µs
Additional Byte Program Time (After First Byte) [16][17]	t_{BP2}	–	–	2.5	12	µs
Page Program Time (105°C) [17]	t_{PP}	–	–	0.7	3	ms
Sector Erase Time (4 kB) [17]	t_{SE}	–	–	50	450	ms
Block Erase Time (64 kB) [17]	t_{BE2}	–	–	500	2000	ms
Chip Erase Time 16 Mb / 32 Mb / 64 Mb [17]	t_{CE}	–	–	11.2 / 32 / 64	64 / 128 / 256	s
End of Reset Instruction to CE# High	t_{RCH} [14]	–	40	–	–	ns
CE# High to next Instruction after Reset	t_{RST} [14]	–	1.5	–	–	µs

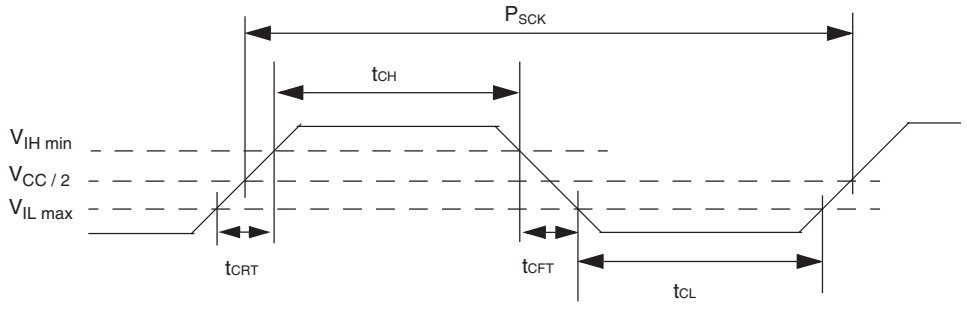
Not Recommended for New Design

Notes

13. Clock high + Clock low must be less than or equal to $1/f_C$.
14. Value guaranteed by design and / or characterization, not 100% tested in production.
15. Only applicable as a constraint for a Write Status Registers command when Status Register Protect 0 (SRP0) bit is set to 1. Or WPSEL bit = 1.
16. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.
17. All program and erase times are tested using a random data pattern.
18. For 10K Cycles. 85 ms at 100K cycles.

5.8.1 Clock Timing

Figure 20. Clock Timing



5.8.2 Input / Output Timing

Figure 21. SPI Single Bit Input Timing

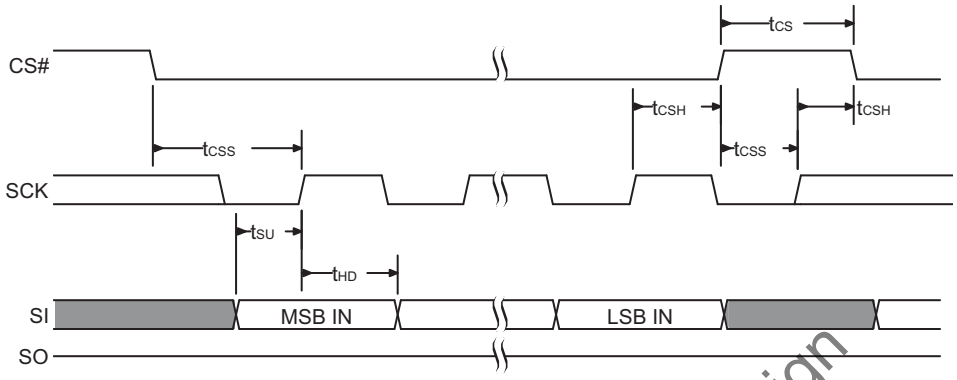


Figure 22. PI Single Bit Output Timing

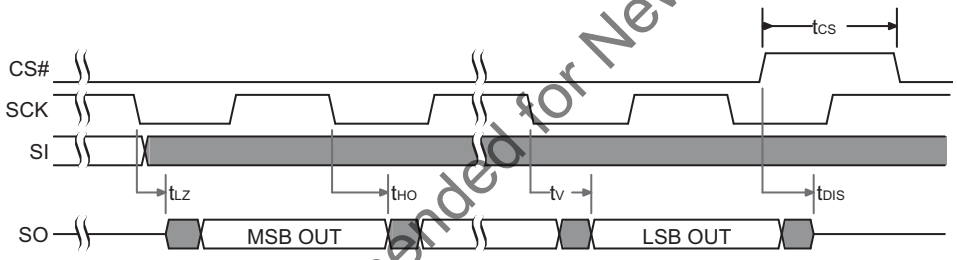
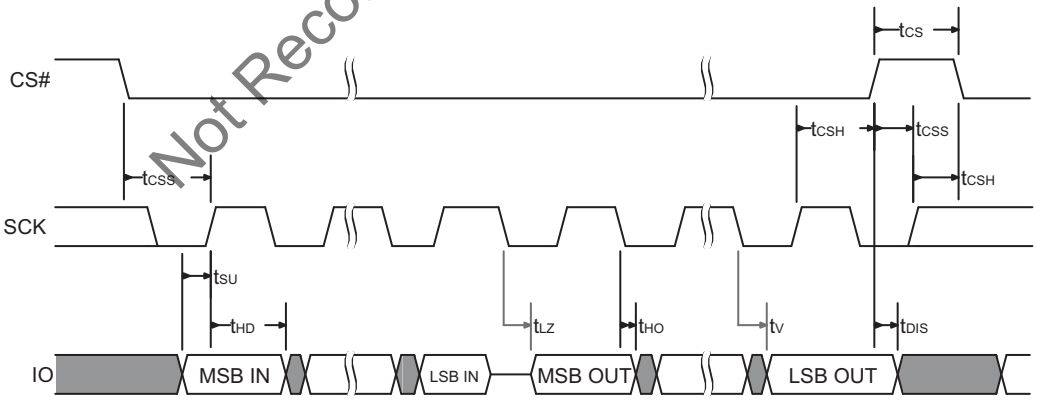


Figure 23. SPI MIO Timing



Not Recommended for New Design

Figure 24. Hold Timing

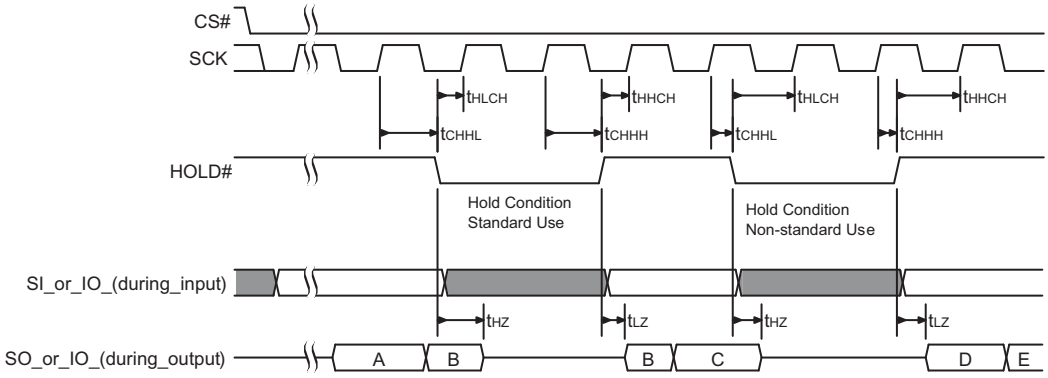
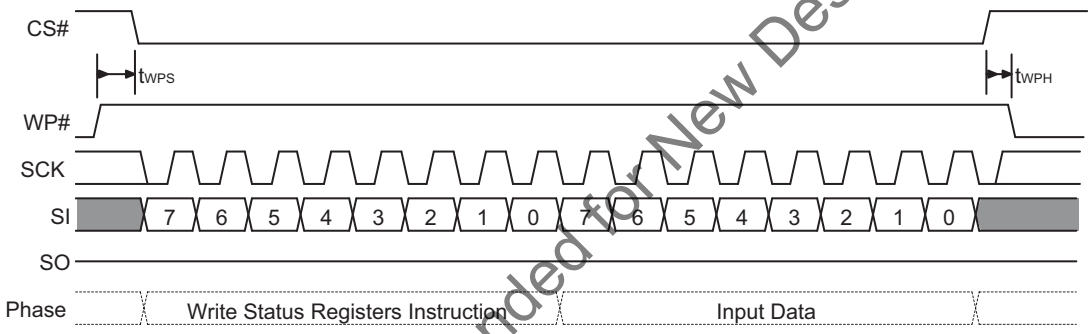
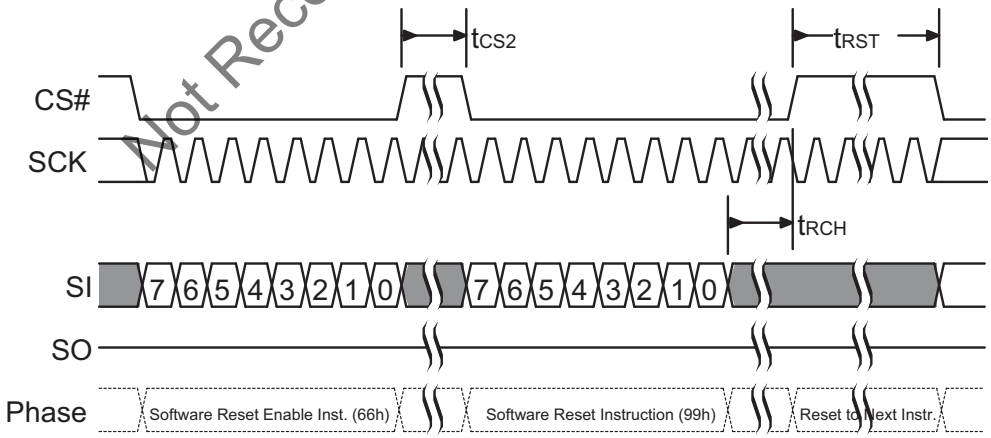


Figure 25. WP# Input Timing



Not Recommended for New Design

Figure 26. Software Reset Input Timing

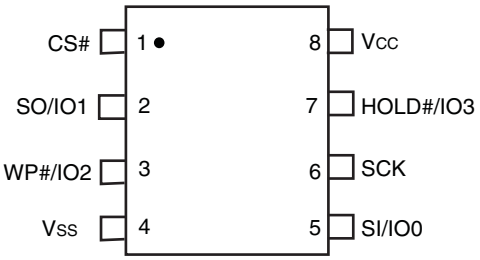


6. Physical Interface

6.1 Connection Diagrams

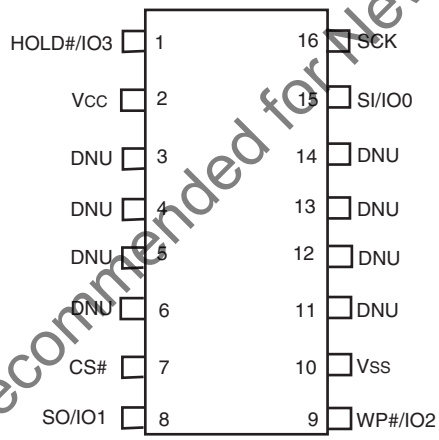
6.1.1 SOIC 8

Figure 27. 8-Pin Plastic Small Outline Package (SO)



6.1.2 SOIC 16 — S25FL164K

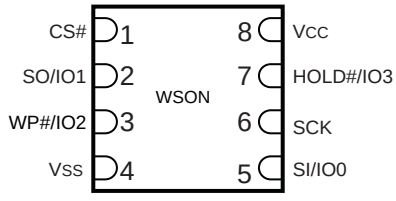
Figure 28. 16-Pin Plastic Small Outline Package (SO)



Not Recommended for New Design

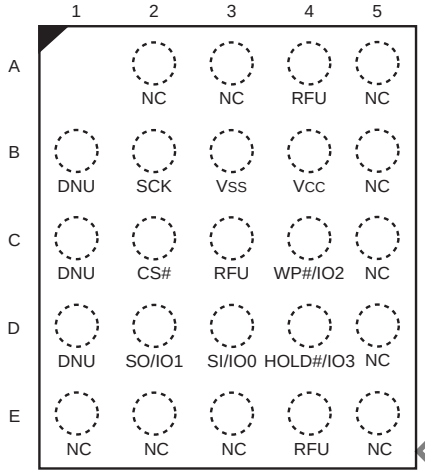
6.1.3 WSON 8

Figure 29. 8-Contact WSON (5 mm x 6 mm) Package / 8-Contact USON (4 mm x 4 mm) Package



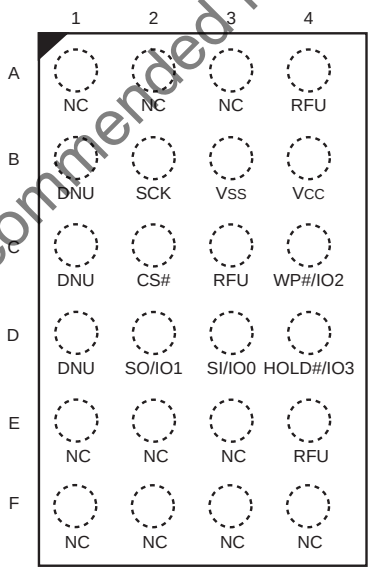
6.1.4 FAB024 24-Ball BGA

Figure 6.1 24-Ball BGA Package, 5x5 Ball Configuration, Top View



6.1.5 FAC024 24-Ball BGA Package

Figure 6.2 24-Ball BGA Package, 6x4 Ball Configuration, Top View



Not Recommended for New Design

Note

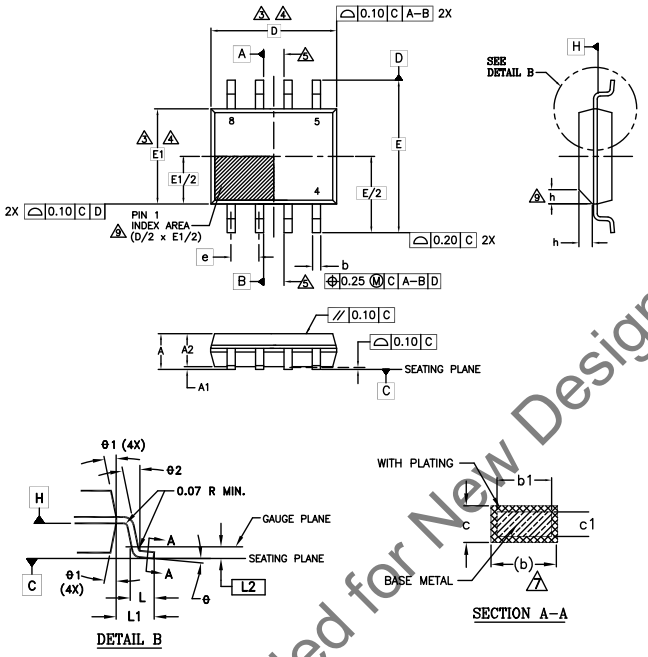
19. Signal connections are in the same relative positions as FAB024 BGA, allowing a single PCB footprint to use either package.

6.1.6 Special Handling Instructions for FBGA Packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and / or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

6.2 Physical Diagrams

6.2.1 SOA008 — 8-Lead Plastic Small Outline Package (150-mils Body Width)

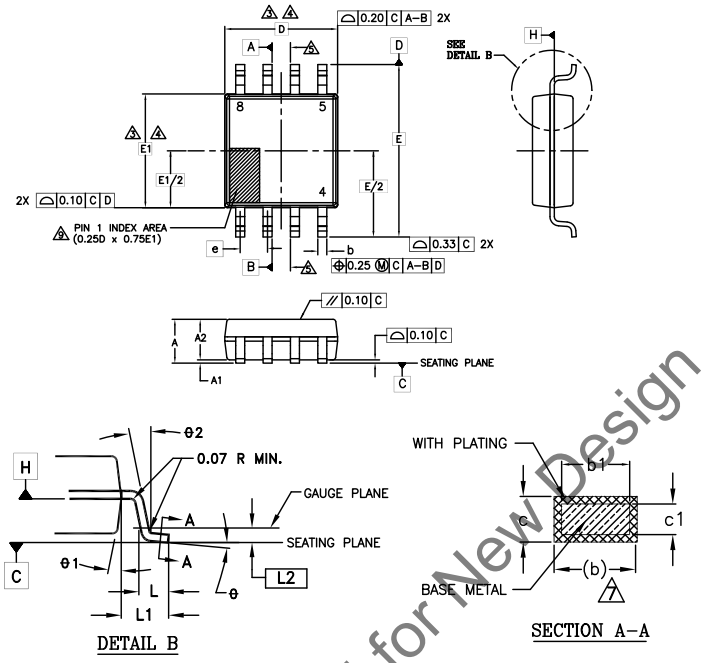


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.32	-	
b	0.31	-	0.51
b1	0.28		0.48
c	0.17		0.25
c1	0.17	-	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	0.89
L1	1.04 REF		
L2	0.25 BSC		
N	8		
h	0.25	-	0.50
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0° REF		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

Not Recommended for New Design

6.2.2 SOC008 — 8-Lead Plastic Small Outline Package (208-mils Body Width)



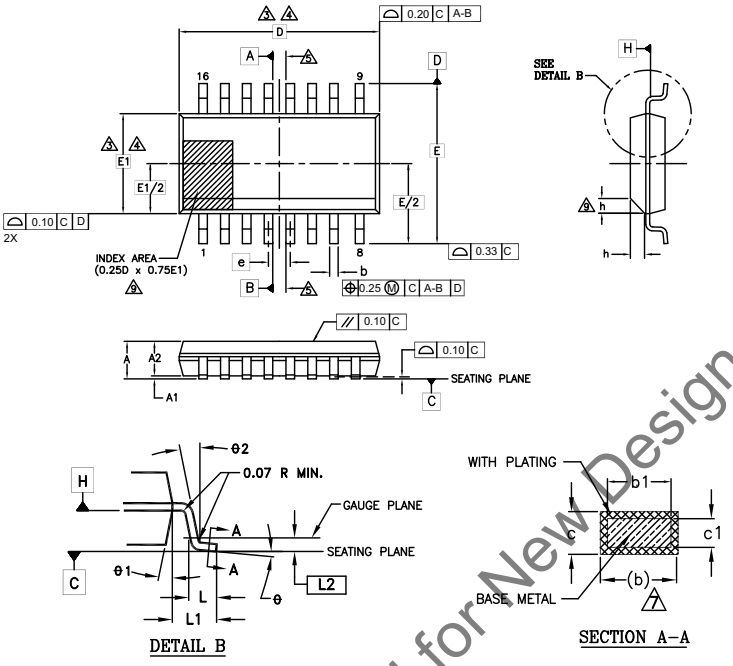
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.75	-	2.16
A1	0.05	-	0.25
A2	1.70	-	1.90
b	0.36	-	0.48
b1	0.33	-	0.46
c	0.19	-	0.24
c1	0.15	-	0.20
D	5.28 BSC		
E	8.00 BSC		
E1	5.28 BSC		
e	1.27 BSC		
L	0.51	-	0.76
L1	1.36 REF		
L2	0.25 BSC		
N	8		
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0-8° REF		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

Not Recommended for New Design

6.2.3 SO3016 — 16-Lead Plastic Wide Outline Package (300-mils Body Width)



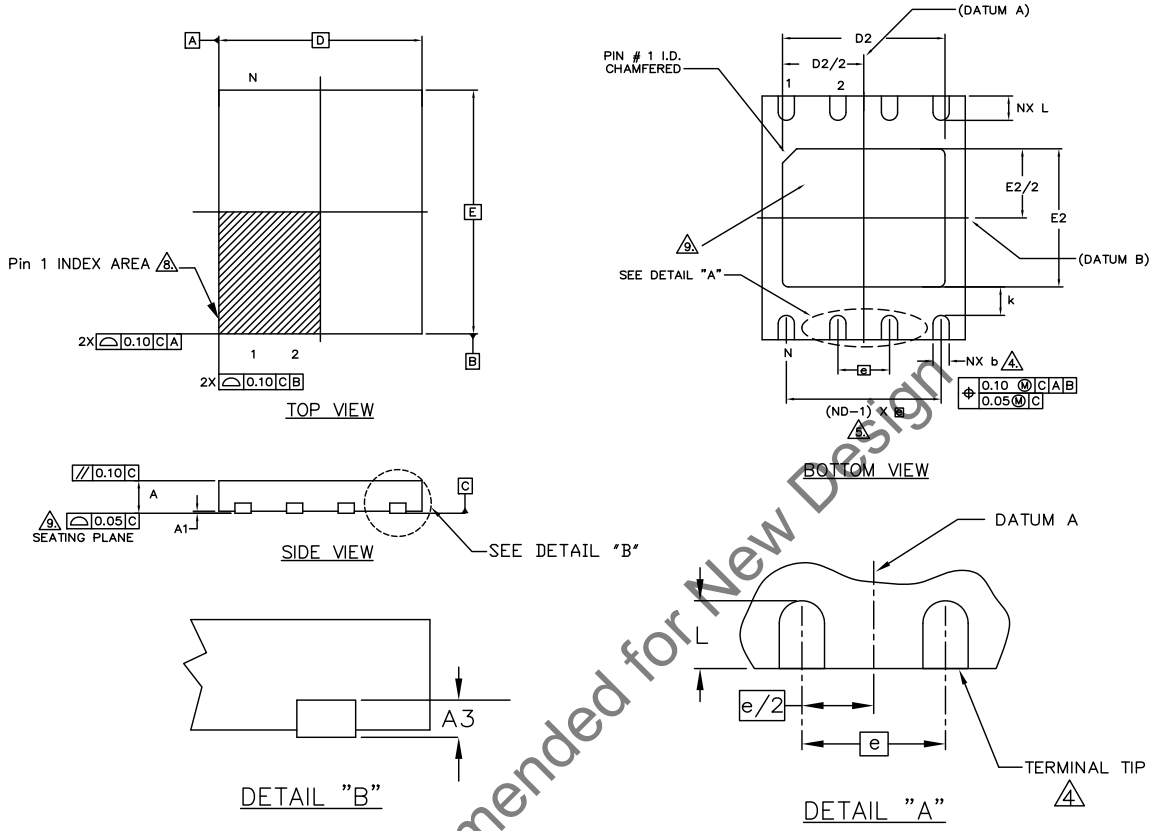
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

Not Recommended for New Design

6.2.4 WND008 — 8-Contact WSON 5 mm × 6 mm



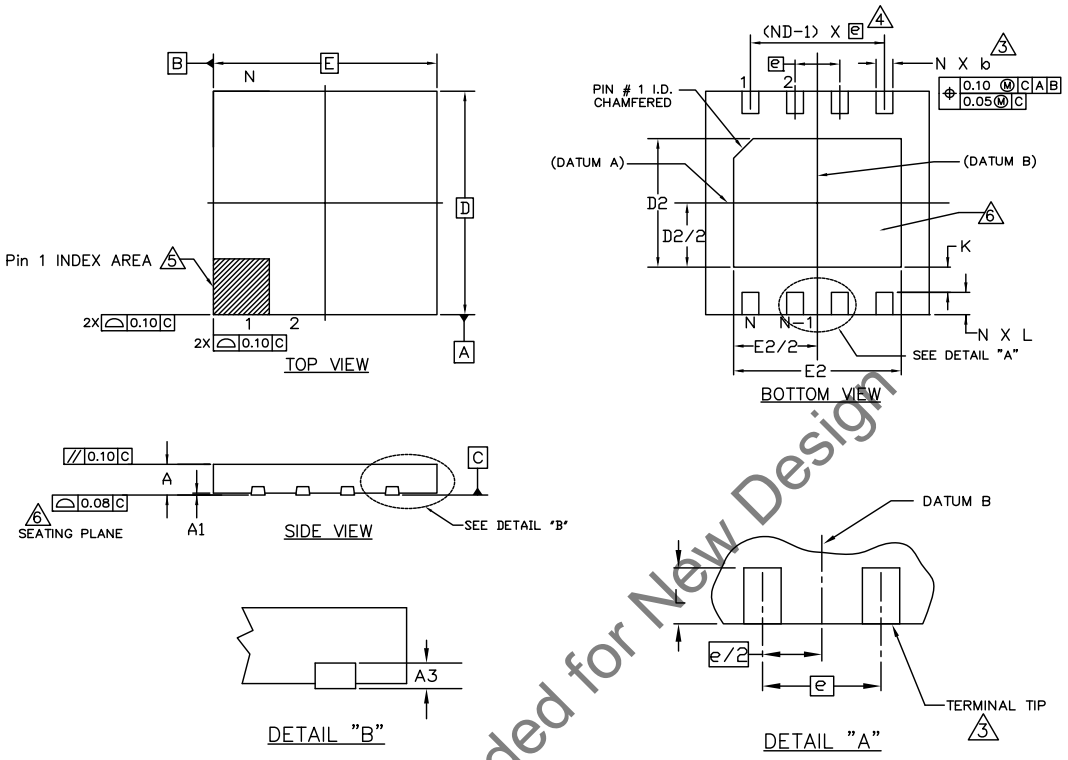
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.55	0.60	0.65
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		5.00 BSC	
E		6.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

Not Recommended for New Design

6.2.5 UNF008 — 8-Contact USON 4 mm x 4 mm



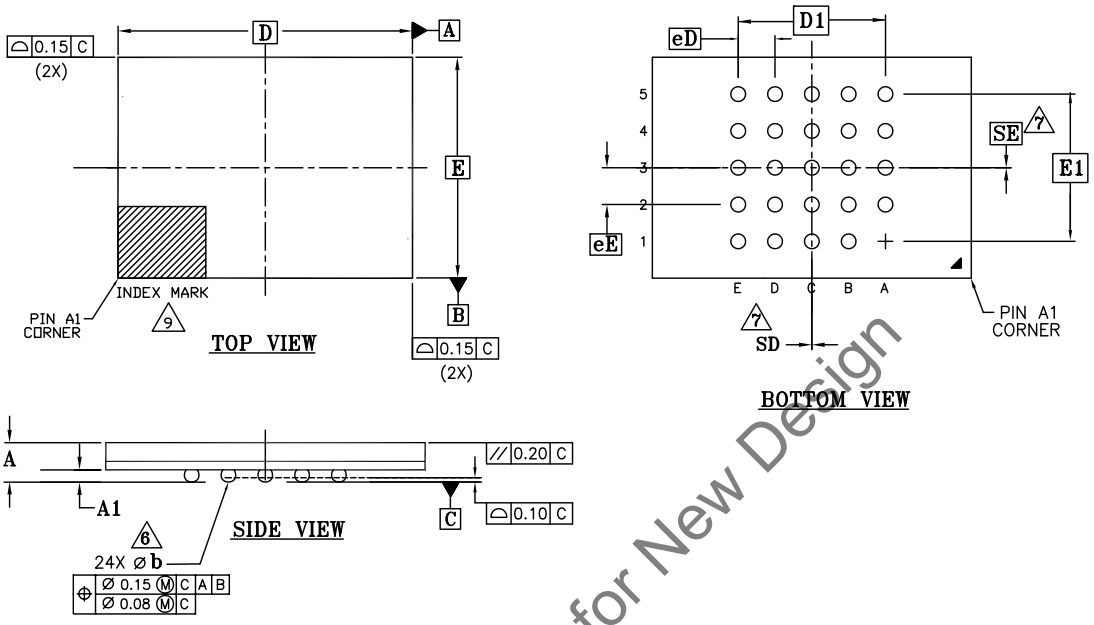
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.80 BSC.	
N		8	
ND		4	
L	0.35	0.40	0.45
b	0.25	0.30	0.35
D2	2.20	2.30	2.40
E2	2.90	3.00	3.10
D		4.00 BSC	
E		4.00 BSC	
A	0.50	0.55	0.60
A1	0.00	0.035	0.05
A3		0.152 REF	
K	0.20	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF: N/A

Not Recommended for New Design

6.2.6 FAB024 — 24-Ball Ball Grid Array (8 mm × 6 mm) Package



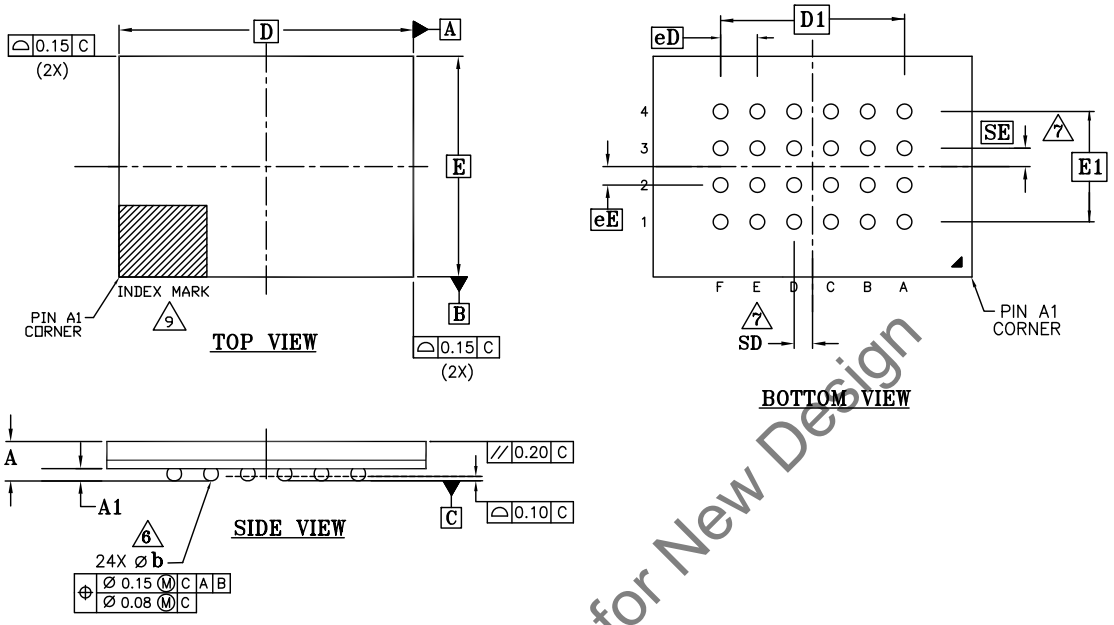
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

Not Recommended for New Design

6.2.7 FAC024 — 24-Ball Ball Grid Array (8 mm × 6 mm) Package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		5.00 BSC	
E1		3.00 BSC	
MD		6	
ME		4	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.50 BSC	
SE		0.50 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

Not Recommended for New Design

7. Software Interface

This section discusses the features and behaviors most relevant to host system software that interacts with S25FL1-K memory devices.

8. Address Space Maps

8.1 Overview

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main flash array. Each separate address space uses the full 24-bit address but may only define a small portion of the available address space.

8.2 Flash Memory Array

The main flash array is divided into erase units called sectors. The sectors are uniform 4 kbytes in size.

S25FL116K Main Memory Address Map

Sector Size (kbyte)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	512	SA0	000000h-000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA511	1FF000h-1FFFFFh	

S25FL132K Main Memory Address Map

Sector Size (kbyte)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	1024	SA0	000000h-000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA1023	3FF000h-3FFFFFh	

S25FL164K Main Memory Address Map

Sector Size (kbyte)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	2048	SA0	000000h-000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA2047	7FF000h-7FFFFFh	

Note: These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-kB sectors have the pattern XXX000h-XXXFFFh.

Not Recommended for New Design

8.3 Security Registers

The S25FL1-K provides four 256-byte Security Registers. Each register can be used to store information that can be permanently protected by programming One Time Programmable (OTP) lock bits in Status Register-2.

Register 0 is used by Cypress to store and protect the Serial Flash Discoverable Parameters (SFDP) information that is also accessed by the Read SFDP command. See Section 8.4.

The three additional Security Registers can be erased, programmed, and protected individually. These registers may be used by system manufacturers to store and permanently protect security or other important information separate from the main memory array.

Table 11. Security Register Addresses

Security Register	Address
0 (SFDP)	000000h - 0000FF
1	001000h - 0010FF
2	002000h - 0020FF
3	003000h - 0030FF

8.4 Security Register 0 — Serial Flash Discoverable Parameters (SFDP — JEDEC JESD216B)

This document defines the Serial Flash Discoverable Parameters (SFDP) revision B data structure for S25FL1-K family.

These data structure values are an update to the earlier revision SFDP data structure in the S25FL1-K family devices.

The Read SFDP (RSFDP) command (5Ah) reads information from a separate flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216B standard for Serial Flash Discoverable Parameters.

The SFDP data structure consists of a header table that identifies the revision of the JESD216 header format that is supported and provides a revision number and pointer for each of the SFDP parameter tables that are provided. The parameter tables follow the SFDP header. However, the parameter tables may be placed in any physical location and order within the SFDP address space. The tables are not necessarily adjacent nor in the same order as their header table entries.

The SFDP header points to the following parameter tables:

- Basic Flash
  - This is the original SFDP table. It has a few modified fields and new additional field added at the end of the table.
- Sector Map
  - This is the original SFDP table. It has a few modified fields and new additional field added at the end of the table.

The physical order of the tables in the SFDP address space is: SFDP Header, Cypress Vendor Specific, Basic Flash, and Sector Map.

The SFDP address space is programmed by Cypress and read-only for the host system.

Not Recommended for New Design

8.4.1 Serial Flash Discoverable Parameters (SFDP) Address Map

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One Basic Flash parameter is mandated by the JEDEC JESD216B standard.

Table 12. SFDP Overview Map — Security Register 0

Byte Address	Description
0000h	Location zero within JEDEC JESD216B SFDP space – start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
0080h	Start of SFDP parameter
...	Remainder of SFDP JEDEC parameter followed by undefined space
00BFh	End of SFDP space
00C0h to 00F7h	Reserved space
00F8h to 00FFh	Unique ID

8.4.2 SFDP Header Field Definitions

Not Recommended for New Design

Table 13. SFDP Header

SFDP Byte Address	SFDP Dword Name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space ASCII “S”
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h	SFDP Header 2nd DWORD	06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B) – This revision is backward compatible with all prior minor revisions. Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields. Increments of the minor revision value indicate that previously reserved parameter fields may have been assigned a new definition or entire Dwords may have been added to the parameter table. However, the definition of previously existing fields is unchanged and therefore remain backward compatible with earlier SFDP parameter table revisions. Software can safely ignore increments of the minor revision number, as long as only those parameters the software was designed to support are used i.e. previously reserved fields and additional Dwords must be masked or ignored. Do not do a simple compare on the minor revision number, looking only for a match with the revision number that the software is designed to handle. There is no problem with using a higher number minor revision.
05h		01h	SFDP Major Revision – This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		03h	Number of Parameter Headers (zero based, 03h = 4 parameters)
07h		FFh	Unused
08h	Parameter Header 0 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		00h	Parameter Minor Revision (00h = JESD216) – This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 0 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a higher numbered minor revision that contains additional parameters for that software revision.
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		09h	Parameter Table Length (in double words = Dwords = 4-byte units) 09h = 9 Dwords
0Ch	Parameter Header 0 2nd DWORD	80h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 80h
0Dh		00h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)

Not Recommended for New Design

Table 13. SFDP Header (Continued)

SFDP Byte Address	SFDP Dword Name	Data	Description
10h	Parameter Header 1 1st DWORD	EFh	Parameter ID LSB (EFh = Winbond Legacy SPI Flash Parameter)
11h		00h	Parameter Minor Revision (00h = JESD216) – This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 0 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a later minor revision that contains additional parameters.
12h		01h	Parameter Major Revision (01h = The original major revision – all SFDP software is compatible with this major revision.
13h		04h	Parameter Table Length (in double words = Dwords = 4-byte units) 04h = 4 Dwords
14h	Parameter Header 1 2nd DWORD	80h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0080h address
15h		00h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18h	Parameter Header 2 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
19h		06h	Parameter Minor Revision (06h = JESD216 Revision B)
1Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
1Bh		10h	Parameter Table Length (in double words = Dwords = 4-byte units) 10h = 16 Dwords
1Ch	Parameter Header 2 2nd DWORD	80h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0080h address
1Dh		00h	Parameter Table Pointer Byte 1
1Eh		00h	Parameter Table Pointer Byte 2
1Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
20h	Parameter Header 3 1st DWORD	01h	Parameter ID LSB (Cypress Vendor Specific ID parameter) Legacy Manufacturer ID 01h = AMD / Cypress
21h		01h	Parameter Minor Revision (01h = ID updated with SFDP Rev B table)
22h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
23h		00h	Parameter Table Length (in double words = Dwords = 4-byte units) 00h not implemented
24h	Parameter Header 3 2nd DWORD	00h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned)
25h		00h	Parameter Table Pointer Byte 1
26h		00h	Parameter Table Pointer Byte 2
27h		01h	Parameter ID MSB (01h = JEDEC JEP106 Bank Number 1)

Not Recommended for New Design

8.4.3 JEDEC SFDP Basic SPI Flash Parameter

Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
00h	JEDEC Basic Flash Parameter Dword-1	E5h	Start of SFDP JEDEC parameter Bits 7:5 = unused = 111b Bit 4:3 = 05h is volatile status register write instruction and status register is default non-volatile= 00b Bit 2 = Program Buffer > 64 bytes = 1 Bits 1:0 = Uniform 4-kB erase is supported through out the device = 01b
01h		20h	Bits 15:8 = Uniform 4-kB erase instruction = 20h
02h		F1h	Bit 23 = Unused = 1b Bit 22 = Supports QOR Read (1-1-4), Yes = 1b Bit 21 = Supports QIO Read (1-4-4),Yes =1b Bit 20 = Supports DIO Read (1-2-2), Yes = 1b Bit19 = Supports DDR, No= 0 b Bit 18:17 = Number of Address Bytes 3 only = 00b Bit 16 = Supports SIO and DIO Yes = 1b Binary Field: 1-1-1-1-0-00-1 Nibble Format: 1111 0001 Hex Format: F1
03h		FFh	Bits 31:24 = Unused = FFh
04h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 16 Mb = 00FFFFFFh 32 Mb = 01FFFFFFh 64 Mb = 03FFFFFFh
05h		FFh	
06h		FFh	
07h		00h 16Mb 01h 32Mb 03h 64Mb	
08h	JEDEC Basic Flash Parameter Dword-3	44h	Bits 7:5 = number of QIO (1-4-4)Mode cycles = 010b Bits 4:0 = number of Fast Read QIO Dummy cycles = 00100b for default latency code
09h		EBh	Fast Read QIO (1-4-4)instruction code
0Ah		08h	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b for default latency code
0Bh		6Bh	Quad Out (1-1-4)instruction code
0Ch	JEDEC Basic Flash Parameter Dword-4	08h	Bits 7:5 = number of Dual Out (1-1-2)Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 01000b for default latency code
0Dh		3Bh	Dual Out (1-1-2) instruction code
0Eh		80h	Bits 23:21 = number of Dual I/O Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 00000b for default latency code
0Fh		BBh	Dual I/O instruction code

Not Recommended for New Design

Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
10h	JEDEC Basic Flash Parameter Dword-5	EEh	Bits 7:5 RFU = 111b Bit 4 = QPI (4-4-4) fast read commands not supported = 0b Bits 3:1 RFU = 111b Bit 0 = Dual All not supported = 0b
11h		FFh	Bits 15:8 = RFU = FFh
12h		FFh	Bits 23:16 = RFU = FFh
13h		FFh	Bits 31:24 = RFU = FFh
14h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
15h		FFh	Bits 15:8 = RFU = FFh
16h		FFh	Bits 23:21 = number of Dual All Mode cycles = 111b Bits 20:16 = number of Dual All Dummy cycles = 11111b
17h		FFh	Dual All instruction code
18h	JEDEC Basic Flash Parameter Dword-7	FFh	Bits 7:0 = RFU = FFh
19h		FFh	Bits 15:8 = RFU = FFh
1Ah		FFh	Bits 23:21 = number of QPI Mode cycles = 111b not supported Bits 20:16 = number of QPI Dummy cycles = 11111b for default latency code
1Bh		FFh	QPI instruction code “Not supported FF”
1Ch	JEDEC Basic Flash Parameter Dword-8	0Ch	Sector type 1 size 2^N Bytes = 4 kB = 0Ch (for Uniform 4 kB)
1Dh		20h	Sector type 1 instruction
1Eh		10h	Sector type 2 size 2^N Bytes = 64 kB = 0Fh (for Uniform 64 kB)
1Fh		D8h	Sector type 2 instruction
20h	JEDEC Basic Flash Parameter Dword-9	00h	Sector type 3 size 2^N Bytes = not supported = 00h
21h		FFh	Sector type 3 instruction = not supported = FFh
22h		00h	Sector type 4 size 2^N Bytes = not supported = 00h
23h		FFh	Sector type 4 instruction = not supported = FFh

Not Recommended for New Design

Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
24h	JEDEC Basic Flash Parameter Dword-10	42h	Bits 31:30 = Sector Type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = RFU = 11b Bits 29:25 = Sector Type 4 Erase, Typical time count = RFU = 11111b (typ erase time = (count +1) * units) = RFU =11111 Bits 24:23 = Sector Type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = RFU = 11b Bits 22:18 = Sector Type 3 Erase, Typical time count = 00100b (typ erase time = (count +1) * units) = RFU =11111 Bits 17:16 = Sector Type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16 ms = 01b Bits 15:11 = Sector Type 2 Erase, Typical time count = 11110b (typ erase time = (count +1) * units) = 31*16 ms = 496 ms Bits 10:9 = Sector Type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b Bits 8:4 = Sector Type 1 Erase, Typical time count = 00100b (typ erase time = (count +1) * units) = 5*16 ms = 80 ms Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time))- 1 = 0010b Multiplier from typical erase time to maximum erase time = 6x multiplier Max Erase time = 2*(Count +1)*Typ Erase time Binary Fields: 11-11111-11-11111-01-11110-01-00100-0010 Nibble Format: 1111_1111_1111_1101_1111_0010_0100_0010 Hex Format: FF_FD_F2_42
25h		F2h	–
26h		FDh	–
27h		FFh	–

Not Recommended for New Design

Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
28h	JEDEC Basic Flash Parameter Dword-11	81h	Bits 23 = Byte Program Typical time, additional byte units (0b:1 µs, 1b:8 µs) = 1 µs = 0b Bits 22:19 = Byte Program Typical time, additional byte count, (count+1)*units, count = 0010b, (typ Program time = (count +1) * units) = 3*1 µs =3 µs Bits 18 = Byte Program Typical time, first byte units (0b:1 µs, 1b:8 µs) = 8 µs = 1b Bits 17:14 = Byte Program Typical time, first byte count, (count+1)*units, count = 0001b, (typ Program time = (count +1) * units) = 2*8 µs = 16 µs Bits 13 = Page Program Typical time units (0b:8 µs, 1b:64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical time count, (count+1)*units, count = 01010b, (typ Program time = (count +1) * units) = 11*64 µs = 704 µs Bits 7:4 = N = 1000b, Page size= 2^N = 256B page Bits 3:0 = Count = 0001b = (Max Page Program time / (2 * Typ Page Program time))- 1 Multiplier from typical Page Program time to maximum Page Program time = 4x multiplier Max Page Program time = 2*(Count +1)*Typ Page Program time Binary Fields: 0-0010-1-0001-1-01010-1000-0001 Nibble Format: 0001_0100_0110_1010_1000_0001 Hex Format: 14_6A_81
29h		6Ah	
2Ah		14h	
2Bh		C2h 16Mb C7h 32Mb CFh 64Mb	16 Mb = 1100_0010b = C2h Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 4s = 10b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, count = 00010b, (typ Program time = (count +1) * units) = 3*4s = 12S 32 Mb = 1100_0111b = C7h Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 4s = 10b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, count = 00111b, (typ Program time = (count +1) * units) = 8*4s = 32s 64 Mb = 1100_1111b = CFh Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 4s = 10b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, count = 01111b, (typ Program time = (count +1) * units) = 16*4S = 64S

Not Recommended for New Design

Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
2Ch	JEDEC Basic Flash Parameter Dword-12	CCh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1us, 10b: 8 µs, 11b: 64 µs) = 1 µs= 01b Bits 28:24 = Suspend in-progress erase max latency count = 10011b, max erase suspend latency = (count +1) * units = 20*1 µs = 20 µs Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = (count +1) * 64 µs = 2 * 64 µs = 128 µs Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1us, 10b: 8 µs, 11b: 64 µs) = 1 µs= 01b Bits 17:13 = Suspend in-progress program max latency count = 10011b, max erase suspend latency = (count +1) * units = 20*1 µs = 20 µs Bits 12:9 = Program resume to suspend interval count = 0001b, interval = (count +1) * 64 µs = 2 * 64 µs = 128 µs Bit 8 = RFU = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a page program anywhere + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1100b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b Binary Fields: 0-01-10011-0001-01-10011-0001-1-1100-1100 Nibble Format: 0011_0011_0001_0110_0110_0011_1100_1100 Hex Format: 33_16_63_CC
2Dh		63h	
2Eh		16h	
2Fh		33h	
30h	JEDEC Basic Flash Parameter Dword-13	7Ah	Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = 75h Bits 7:0 = Program Resume Instruction = 7Ah
31h		75h	
32h		7Ah	
33h		75h	
34h	JEDEC Basic Flash Parameter Dword-14	F7h	Bit 31 = Deep Power-Down Supported = 0 Bits 30:23 = Enter Deep Power-Down Instruction = B9h Bits 22:15 = Exit Deep Power-Down Instruction = ABh Bits 14:13 = Exit Deep Power-Down to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 1 µs = 01b Bits 12:8 = Exit Deep Power-Down to next operation delay count = 00010b, Exit Deep Power-Down to next operation delay = (count+1)*units = 3*1 µs=3 µs Bits 7:4 = RFU = 1111b Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy). Bits 1:0 = RFU = 11b Binary Fields: 0-10111001-10101011-01-00010-1111-01-11 Nibble Format: 0101_1100_1101_0101_1010_0010_1111_0111 Hex Format: 5C_D5_A2_F7
35h		A2h	
36h		D5h	
37h		5Ch	

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Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
38h	JEDEC Basic Flash Parameter Dword-15	00h	Bits 31:24 = RFU = FFh Bit 23 = Hold and WP Disable = not supported = 0b Bits 22:20 = Quad Enable Requirements = 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x0xxb: Mode Bits[7:0] = Axh + 1xxxb: RFU = 1001b Bits 15:10 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + 11_x1xx: RFU = 111101 Bit 9 = 0-4-4 mode supported = 1 Bits 8:4 = 4-4-4 mode enable sequences = 0_0000b: not supported Bits 3:0 = 4-4-4 mode disable sequences = 0000b: not supported Binary Fields: 11111111-0-101-1001-111101-1-00000-0000 Nibble Format: 1111_1111_0101_1001_1111_0110_0000_0000 Hex Format: FF_59_F6_00
39h		F6h	
3Ah		59h	
3Bh		FFh	

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Table 14. Basic SPI Flash Parameter, JEDEC SFDP Rev B (Continued)

SFDP Parameter Relative Byte Address	SFDP Dword Name	Data	Description
3Ch	JEDEC Basic Flash Parameter Dword-16	E8h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b:issue instruction B7 (preceding write enable not required + xx1x_xxxxb: Supports dedicated 4-byte address instruction set. Consult vendor data sheet for the instruction set definition or look for 4-byte Address Parameter Table. + 1xxx_xxxxb: Reserved = 10000000b not supported Bits 23:14 = Exit 4-byte Addressing = xx_xxxx_xxx1b:issue instruction E9h to exit 4-byte address mode (Write enable instruction 06h is not required) + xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_0000_0000b not supported Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1,2, or 4 wires depending on the device operating mode = 01_0000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or nonvolatile Register and Write Enable Instruction for Status Register 1 = xxx_1xxxb: nonvolatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to nonvolatile status register. Volatile status register may be activated after power-up to override the nonvolatile status register, use instruction 50h to enable write and activate the volatile status register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1101000b Binary Fields: 10000000-1100000000-010000-1-1101000 Nibble Format: 1000_0000_1100_0000_0001_0000_1110_1000 Hex Format: 80_C0_10_E8
3Dh		10h	
3Eh		C0h	
3Fh		80h	

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8.5 Status Registers

Status Register-1 (SR1) and Status Register-2 (SR2) can be used to provide status on the availability of the flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, and Erase / Program Suspend status.

SR1 and SR2 contain nonvolatile bits in locations SR1[7:2] and SR2[6:0] that control sector protection, OTP Register Protection, Status Register Protection, and Quad mode. Bit locations SR2[7], SR1[1], and SR1[0] are read only volatile bits for suspend, write enable, and busy status; these are updated by the memory control logic. The SR1[1] write enable bit is set only by the Write Enable (06h) command and cleared by the memory control logic when an embedded operation is completed.

Write access to the nonvolatile Status Register bits is controlled by the state of the nonvolatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable command (06h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

A volatile version of bits SR2[6], SR2[1], and SR1[7:2] that control sector protection and Quad Mode are used to control the behavior of these features after power up. During power up or software reset, these volatile bits are loaded from the nonvolatile version of the Status Register bits. The Write Enable for Volatile Status Register (50h) command can be used to write these volatile bits when the command is followed by a Write Status Registers (01h) command. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical nonvolatile bit write cycles or affecting the endurance of the Status Register nonvolatile bits.

Write access to the volatile SR1 and SR2 Status Register bits is controlled by the state of the nonvolatile Status Register Protect bits SR1[7] and SR2[0] (SRP0, SRP1), the Write Enable for Volatile Status Register command (50h) preceding a Write Status Registers command, and while Quad mode is not enabled, the WP# pin.

Status Register-3 (SR3) is used to configure and provide status on the variable read latency, and Quad IO wrapped read features.

Write access to the volatile SR3 Status Register bits is controlled by Write Enable for Volatile Status Register command (50h) preceding a Write Status Register command. The SRP bits do not protect SR3.

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Table 15. Status Register-1 (SR1)

Bits	Field Name	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Nonvolatile and Volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down See Table on page 58.
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors See Table 20 on page 54 and Table 21 on page 55 for protection ranges.
5	TB	Top / Bottom Protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up See Table 20 on page 54 and Table 21 on page 55 for protection ranges.
4	BP2	Block Protect Bits		0	000b = No protection See Table 20 on page 54 and Table 21 on page 55 for protection ranges.
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 16. Status Register-2 (SR2)

Bits	Field Name	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	nonvolatile and Volatile versions	0	0 = Normal Protection Map 1 = Inverted Protection Map See Table 20 on page 54 and Table 21 on page 55 for protection ranges.
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected Security register 0 contains the Serial Flash Discoverable Parameters and is always programmed and locked by Cypress.
4	LB2			0	
3	LB1			0	
2	LB0			1	
1	QE	Quad Enable	nonvolatile and Volatile versions	0 (For all model numbers except 'Q1')	0 = Quad Mode Not Enabled, the WP# pin and HOLD# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled
				1 (For model number 'Q1')	1 = Quad Mode Enabled and **can not** be changed, the IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled
0	SRP1	Status Register Protect 1		0	0 = SRP1 selects whether WP# input has effect on protection of the status register 1 = SRP1 selects Power Supply Lock Down or OTP Lock Down mode See Table on page 58.

Note

20. LB0 value should be considered don't care for read. This bit is set to 1.

Table 17. Status Register-3 (SR3)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved		0	Reserved for Future Use
6	W6	Burst Wrap Length	Volatile	1	00 = 8-byte wrap. Data read starts at the initial address and wraps within an aligned 8-byte boundary. 01 = 16-byte wrap. Data read starts at the initial address and wraps within an aligned 16-byte boundary. 10 = 32-byte wrap. Data read starts at the initial address and wraps within an aligned 32-byte boundary. 11 = 64-byte wrap. Data read starts at the initial address and wraps within an aligned 64-byte boundary.
5	W5			1	
4	W4	Burst Wrap Enable		1	0 = Wrap Enabled 1 = Wrap Disabled
3	Latency Control (LC)	Variable Read Latency Control		0	Defines the number of read latency cycles in Fast Read, Dual Out, Quad Out, Dual IO, and Quad IO commands. Binary values for 1 to 15 latency cycles. A value of zero disables the variable latency mode.
2				0	
1				0	
0				0	

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8.5.1 BUSY

BUSY is a read only bit in the Status Register (SR1[0]) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers or Erase / Program Security Register command. During this time the device will ignore further commands except for the Software Reset, Read Status Register and Erase / Program Suspend commands (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in Section 5.8 AC Electrical Characteristics on page 25). When the program, erase or write status / security register command has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further commands.

8.5.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the Status Register (SR1[1]) that is set to 1 after executing a Write Enable Command. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers, Erase Security Register and Program Security Register. The WEL status bit is cleared to 0 even when a program or erase operation is prevented by the block protection bits. The WEL status bit is also cleared to 0 when a program or erase operation is suspended. The WEL status bit is set to 1 when a program or erase operation is resumed.

8.5.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are nonvolatile read / write bits in the Status Register (SR1[4:2]) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Registers Command (see t_W in Section 5.8 AC Electrical Characteristics on page 25). All, none or a portion of the memory array can be protected from Program and Erase commands (see Section 8.5.7 Block Protection Maps on page 53). The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

8.5.4 Top / Bottom Block Protect (TB)

The nonvolatile Top / Bottom bit (TB SR1[5]) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Section 8.5.7 Block Protection Maps on page 53. The factory default setting is TB=0. The TB bit can be set with the Write Status Registers Command depending on the state of the SRP0, SRP1 and WEL bits.

8.5.5 Sector / Block Protect (SEC)

The nonvolatile Sector / Block Protect bit (SEC SR1[6]) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Section 8.5.7 Block Protection Maps on page 53. The default setting is SEC=0.

8.5.6 Complement Protect (CMP)

The Complement Protect bit (CMP SR2[6]) is a nonvolatile read / write bit in the Status Register (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4-kB sector can be protected while the rest of the array is not; when CMP=1, the top 4-kB sector will become unprotected while the rest of the array become read-only. Refer to Section 8.5.7 Block Protection Maps on page 53 for details. The default setting is CMP=0.

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8.5.7 Block Protection Maps

Table 18. FL116K Block Protection (CMP = 0)

Status Register [21]					S25FL1-K (16 Mbit) Block Protection (CMP=0) [22]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	31	1F0000h – 1FFFFFh	64 kB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128 kB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h – 1FFFFFh	256 kB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h – 1FFFFFh	512 kB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h – 1FFFFFh	1 MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2 MB	All
1	0	0	0	1	31	1FF000h – 1FFFFFh	4 kB	Upper 1/512
1	0	0	1	0	31	1FE000h – 1FFFFFh	8 kB	Upper 1/256
1	0	0	1	1	31	1FC000h – 1FFFFFh	16 kB	Upper 1/128
1	0	1	0	X	31	1F8000h – 1FFFFFh	32 kB	Upper 1/64
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/512
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/256
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/128
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/64

Notes

21. X = don't care.
22. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Table 19. FL116K Block Protection (CMP = 1)

Status Register [23]					S25FL1-K (16 Mbit) Block Protection (CMP=1) [24]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	0 thru 31	000000h – 1FFFFFh	All	All
0	0	0	0	1	0 thru 30	000000h – 1EFFFFh	1,984 kB	Lower 31/32
0	0	0	1	0	0 thru 29	000000h – 1DFFFFh	1,920 kB	Lower 15/16
0	0	0	1	1	0 thru 27	000000h – 1BFFFFh	1,792 kB	Lower 7/8
0	0	1	0	0	0 thru 23	000000h – 17FFFFh	1,536 kB	Lower 3/4
0	0	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/2
0	1	0	0	1	1 thru 31	010000h – 1FFFFFh	1,984 kB	Upper 31/32
0	1	0	1	0	2 and 31	020000h – 1FFFFFh	1,920 kB	Upper 15/16
0	1	0	1	1	4 thru 31	040000h – 1FFFFFh	1,792 kB	Upper 7/8
0	1	1	0	0	8 thru 31	080000h – 1FFFFFh	1,536 kB	Upper 3/4
0	1	1	0	1	16 thru 31	100000h – 1FFFFFh	1 MB	Upper 1/2
X	X	1	1	X	None	None	None	None
1	0	0	0	1	0 thru 31	000000h – 1FEFFFh	2,044 kB	Lower 511/512

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Table 19. FL116K Block Protection (CMP = 1) (Continued)

Status Register [23]					S25FL1-K (16 Mbit) Block Protection (CMP=1) [24]			
1	0	0	1	0	0 thru 31	000000h – 1FDFFFh	2,040 kB	Lower 255/256
1	0	0	1	1	0 thru 31	000000h – 1FBFFFh	2,032 kB	Lower 127/128
1	0	1	0	X	0 thru 31	000000h – 1F7FFFh	2,016 kB	Lower 63/64
1	1	0	0	1	0 thru 31	001000h – 1FFFFFh	2,044 kB	Upper 511/512
1	1	0	1	0	0 thru 31	002000h – 1FFFFFh	2,040 kB	Upper 255/256
1	1	0	1	1	0 thru 31	004000h – 1FFFFFh	2,032 kB	Upper 127/128
1	1	1	0	X	0 thru 31	008000h – 1FFFFFh	2,016 kB	Upper 63/64

Notes

23. X = don't care.
24. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Table 20. FL132K Block Protection (CMP = 0)

Status Register [25]					S25FL132K (32-Mbit) Block Protection (CMP=0) [26]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	63	3F0000h – 3FFFFFh	64 kB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h – 3FFFFFh	128 kB	Upper 1/32
0	0	0	1	1	60 thru 63	3C0000h – 3FFFFFh	256 kB	Upper 1/16
0	0	1	0	0	56 thru 63	380000h – 3FFFFFh	512 kB	Upper 1/8
0	0	1	0	1	48 thru 63	300000h – 3FFFFFh	1 MB	Upper 1/4
0	0	1	1	0	32 thru 63	200000h – 3FFFFFh	2 MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/64
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/32
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/16
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/8
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/4
0	1	1	1	0	0 thru 31	000000h – 1FFFFFh	2 MB	Lower 1/2
X	X	1	1	1	0 thru 63	000000h – 3FFFFFh	4 MB	All
1	0	0	0	1	63	3FF000h – 3FFFFFh	4 kB	Upper 1/1024
1	0	0	1	0	63	3FE000h – 3FFFFFh	8 kB	Upper 1/512
1	0	0	1	1	63	3FC000h – 3FFFFFh	16 kB	Upper 1/256
1	0	1	0	X	63	3F8000h – 3FFFFFh	32 kB	Upper 1/128
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/1024
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/512
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/256
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/128

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Notes

25. X = don't care.
26. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Table 21. FL132K Block Protection (CMP = 1)

Status Register [27]					S25FL132K (32-Mbit) Block Protection (CMP=1) [28]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	0 thru 63	000000h – 3FFFFFh	4 MB	All
0	0	0	0	1	0 thru 62	000000h – 3EFFFFh	4,032 kB	Lower 63/64
0	0	0	1	0	0 and 61	000000h – 3DFFFFh	3,968 kB	Lower 31/32
0	0	0	1	1	0 thru 59	000000h – 3BFFFFh	3,840 kB	Lower 15/16
0	0	1	0	0	0 thru 55	000000h – 37FFFFh	3,584 kB	Lower 7/8
0	0	1	0	1	0 thru 47	000000h – 2FFFFFh	3 MB	Lower 3/4
0	0	1	1	0	0 thru 31	000000h – 1FFFFFh	2 MB	Lower 1/2
0	1	0	0	1	1 thru 63	010000h – 3FFFFFh	4,032 kB	Upper 63/64
0	1	0	1	0	2 and 63	020000h – 3FFFFFh	3,968 kB	Upper 31/32
0	1	0	1	1	4 thru 63	040000h – 3FFFFFh	3,840 kB	Upper 15/16
0	1	1	0	0	8 thru 63	080000h – 3FFFFFh	3,584 kB	Upper 7/8
0	1	1	0	1	16 thru 63	100000h – 3FFFFFh	3 MB	Upper 3/4
0	1	1	1	0	32 thru 63	200000h – 3FFFFFh	2 MB	Upper 1/2
X	X	1	1	1	None	None	None	None
1	0	0	0	1	0 thru 63	000000h – 3FEFFFh	4,092 kB	Lower 1023/1024
1	0	0	1	0	0 thru 63	000000h – 3FDFFFh	4,088 kB	Lower 511/512
1	0	0	1	1	0 thru 63	000000h – 3FBFFFh	4,080 kB	Lower 255/256
1	0	1	0	X	0 thru 63	000000h – 3F7FFFh	4,064 kB	Lower 127/128
1	1	0	0	1	0 thru 63	001000h – 3FFFFFh	4,092 kB	Upper 1023/1024
1	1	0	1	0	0 thru 63	002000h – 3FFFFFh	4,088 kB	Upper 511/512
1	1	0	1	1	0 thru 63	004000h – 3FFFFFh	4,080 kB	Upper 255/256
1	1	1	0	X	0 thru 63	008000h – 3FFFFFh	4,064 kB	Upper 127/128

Notes

27. X = don't care.
28. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

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Table 22. FL164K Block Protection (CMP = 0)

Status Register [29]					S25FL164K (64-Mbit) Block Protection (CMP=0) [30]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	126 and 127	7E0000h – 7FFFFFh	128 kB	Upper 1/64
0	0	0	1	0	124 thru 127	7C0000h – 7FFFFFh	256 kB	Upper 1/32
0	0	0	1	1	120 thru 127	780000h – 7FFFFFh	512 kB	Upper 1/16
0	0	1	0	0	112 thru 127	700000h – 7FFFFFh	1 MB	Upper 1/8
0	0	1	0	1	96 thru 127	600000h – 7FFFFFh	2 MB	Upper 1/4
0	0	1	1	0	64 thru 127	400000h – 7FFFFFh	4 MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/64
0	1	0	1	0	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/32
0	1	0	1	1	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/16

Table 22. FL164K Block Protection (CMP = 0) (Continued)

Status Register [29]					S25FL164K (64-Mbit) Block Protection (CMP=0) [30]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
0	1	1	0	0	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/8
0	1	1	0	1	0 thru 31	000000h – 1FFFFFh	2 MB	Lower 1/4
0	1	1	1	0	0 thru 63	000000h – 3FFFFFh	4 MB	Lower 1/2
X	X	1	1	1	0 thru 127	000000h – 7FFFFFh	8 MB	ALL
1	0	0	0	1	127	7FF000h – 7FFFFFh	4 kB	Upper 1/2048
1	0	0	1	0	127	7FE000h – 7FFFFFh	8 kB	Upper 1/1024
1	0	0	1	1	127	7FC000h – 7FFFFFh	16 kB	Upper 1/512
1	0	1	0	X	127	7F8000h – 7FFFFFh	32 kB	Upper 1/256
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower1/2048
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/1024
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/512
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/256

Notes

29. X = don't care.
30. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Not Recommended for New Design

Table 23. FL164K Block Protection (CMP = 1)

Status Register [31]					S25FL164K (64-Mbit) Block Protection (CMP=1) [32]			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
X	X	0	0	0	0 thru 127	000000h – 7FFFFFh	8 MB	ALL
0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064 kB	Lower 63/64
0	0	0	1	0	0 thru 123	000000h – 7BFFFFh	7,936 kB	Lower 31/32
0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680 kB	Lower 15/16
0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7 MB	Lower 7/8
0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	5 MB	Lower 3/4
0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4 MB	Lower 1/2
0	1	0	0	1	2 thru 127	020000h – 7FFFFFh	8,064 kB	Upper 63/64
0	1	0	1	0	4 thru 127	040000h – 7FFFFFh	7,936 kB	Upper 31/32
0	1	0	1	1	8 thru 127	080000h – 7FFFFFh	7,680 kB	Upper 15/16
0	1	1	0	0	16 thru 127	100000h – 7FFFFFh	7 MB	Upper 7/8
0	1	1	0	1	32 thru 127	200000h – 7FFFFFh	5 MB	Upper 3/4
0	1	1	1	0	64 thru 127	400000h – 7FFFFFh	4 MB	Upper 1/2
X	X	1	1	1	None	None	None	None
1	0	0	0	1	0 thru 127	000000h – 7FEFFFh	8,188 kB	Lower 2047/2048
1	0	0	1	0	0 thru 127	000000h – 7FDFFFh	8,184 kB	Lower 1023/1024
1	0	0	1	1	0 thru 127	000000h – 7FBFFFh	8,176 kB	Lower 511/512
1	0	1	0	X	0 thru 127	000000h – 7F7FFFh	8,160 kB	Lower 255/256
1	1	0	0	1	0 thru 127	001000h – 7FFFFFh	8,188 kB	Lower 2047/2048
1	1	0	1	0	0 thru 127	002000h – 7FFFFFh	8,184 kB	Lower 1023/1024
1	1	0	1	1	0 thru 127	004000h – 7FFFFFh	8,176 kB	Lower 511/512
1	1	1	0	X	0 thru 127	008000h – 7FFFFFh	8,160 kB	Lower 255/256

Not Recommended for New Design

Notes

31. X = don't care.
32. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8.5.8 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are nonvolatile read / write bits in the Status Register (SR2[0] and SR1[7]). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down, or one time programmable (OTP) protection.

Status Register Protection Bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. SR1 and SR2 can be written to after a Write Enable command, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When WP# pin is low the SR1 and SR2 are locked and can not be written.
0	1	1	Hardware Unprotected	When WP# pin is high SR1 and SR2 are unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	SR1 and SR2 are protected and can not be written to again until the next power-down, power-up cycle. [33]
1	1	X	One Time Program [34]	SR1 and SR2 are permanently protected and can not be written.

Notes

33. When SRP1, SRP0 = (1, 0), a power-down, power-up, or Software Reset cycle will change SRP1, SRP0 to (0, 0) state.
34. The One-Time Program feature is available upon special order. Contact Cypress for details.
35. Busy, WEL, and SUS (SR1[1:0] and SR2[7]) are volatile read only status bits that are never affected by the Write Status Registers command.
36. The nonvolatile version of CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR2[6,1,0] and SR1[6:2]) bits and the OTP LB3-LB0 bits are not writable when protected by the SRP bits and WP# as shown in the table. The nonvolatile version of these Status Register bits are selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command.
37. The volatile version of CMP, QE, SRP1, SRP0, SEC, TB, and BP2-BP0 (SR2[6,1,0] and SR1[6:2]) bits are not writable when protected by the SRP bits and WP# as shown in the table. The volatile version of these Status Register bits are selected for writing when the Write Enable for volatile Status Register (50h) command precedes the Write Status Registers (01h) command. There is no volatile version of the LB3-LB0 bits and these bits are not affected by a volatile Write Status Registers command.
38. The volatile SR3 bits are not protected by the SRP bits and may be written at any time by volatile (50h) Write Enable command preceding the Write Status Registers (01h) command.

8.5.9 Erase / Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (SR2[7]) that is set to 1 after executing an Erase / Program Suspend (75h) command. The SUS status bit is cleared to 0 by Erase / Program Resume (7Ah) command as well as a power-down, power-up cycle.

8.5.10 Security Register Lock Bits (LB3, LB2, LB1, LB0)

The Security Register Lock Bits (LB3, LB2, LB1, LB0) are nonvolatile One Time Program (OTP) bits in Status Register (SR2[5:2]) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers 1 to 3 are unlocked. LB[3:1] can be set to 1 individually using the Write Status Registers command. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-byte Security Register will become read-only permanently.

Security Register 0 is programmed with the SFDP parameters and LB0 is programmed to 1 by Cypress.

8.5.11 Quad Enable (QE)

The Quad Enable (QE) bit is a nonvolatile read / write bit in the Status Register (SR2[1]) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled.

Note: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

Not Recommended for New Design

8.5.12 Latency Control (LC)

Status Register-3 provides bits (SR3[3:0]) to select the number of read latency cycles used in each Fast Read command. The Read Data command is not affected by the latency code. The binary value of this field selects from 1 to 15 latency cycles. The zero value selects the legacy number of latency cycles used in prior generation FL-K family devices. The default is 0 cycles to provide backward compatibility to legacy devices. The Latency Control bits may be set to select a number of read cycles optimized for the frequency in use. If the number of latency cycles is not sufficient for the operating frequency, invalid data will be read.

Table 24. Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V

Latency Control	Read Command Maximum Frequency (MHz)				
	Fast Read	Dual Output	Dual I/O	Quad Output	Quad I/O
0 (legacy read latency)	108 (8 dummy)	108 (8 dummy)	88 (4 mode, 0 dummy)	108 (8 dummy)	78 (2 mode, 4 dummy)
1	50	50	94	43	49
2	95	85	105	56	59
3	105	95	108	70	69
4	108	105	108	83	78
5	108	108	108	94	86
6	108	108	108	105	95
7	108	108	108	108	105
8	108	108	108	108	108
9	108	108	108	108	108
10	108	108	108	108	108
11	108	108	108	108	108
12	108	108	108	108	108
13	108	108	108	108	108
14	108	108	108	108	108
15	108	108	108	108	108

Not Recommended for New Design

Notes

39. SCK frequency > 108 MHz SIO, 108 MHz DIO, or 108 MHz QIO is not supported by this family of devices.
40. The Dual I/O and Quad I/O command protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Dual I/O command has four Continuous Read Mode bits following the address and no additional dummy cycles. Therefore, the legacy Dual I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of zero cycles. By increasing the variable read latency the frequency of the Dual I/O command can be increased to allow operation up to the maximum supported 108 MHz DIO frequency.

8.5.13 Burst Wrap Enable (W4)

Status Register-3 provides a bit (SR3[4]) to enable a read with wrap option for the Quad I/O Read command. When SR3[4]=1, the wrap mode is not enabled and unlimited length sequential read is performed. When SR3[4]=0, the wrap mode is enabled and a fixed length and aligned group of 8, 16, 32, or 64 bytes will be read starting at the byte address provided by the Quad I/O Read command and wrapping around at the group alignment boundary.

8.5.14 Burst Wrap Length (W6, W5)

Status Register-3 provides bits (SR3[1:0]) to select the alignment boundary at which reading will wrap to perform a cache line fill. Reading begins at the initial byte address of a Fast Read Quad IO command, then sequential bytes are read until the selected boundary is reached. Reading then wraps to the beginning of the selected boundary. This enables critical word first cache line refills. The wrap point can be aligned on 8-, 16-, 32-, or 64-byte boundaries.

8.6 Device Identification

8.6.1 Legacy Device Identification Commands

Three legacy commands are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in Table 25.

Table 25. Device Identification

Device OPN	Instruction	Data 1	Data 2	Data 3
S25FL116K	ABh[41]	Device ID = 14h	—	—
	90h[42]	Manufacturer ID = 01h	Device ID = 14h	—
	9Fh[43]	Manufacturer ID = 01h	Device Type = 40h	Capacity = 15h
S25FL132K	ABh[41]	Device ID = 15h	—	—
	90h[42]	Manufacturer ID = 01h	Device ID = 15h	—
	9Fh[43]	Manufacturer ID = 01h	Device Type = 40h	Capacity = 16h
S25FL164K	ABh[41]	Device ID = 16h	—	—
	90h[42]	Manufacturer ID = 01h	Device ID = 16h	—
	9Fh[43]	Manufacturer ID = 01h	Device Type = 40h	Capacity = 17h

Notes

41. The ABh instruction is followed by three dummy address bytes then the output of Device ID byte. See Section 29 Command Set (ID, Security Commands) on page 65 and Section 10.5.2 Release from Deep-Power-Down / Device ID (ABh) on page 78.
42. The 90h instruction is followed by three address bytes with (Address = 0) followed by the output of Manufacturer ID byte then the Device ID byte See Section 29 Command Set (ID, Security Commands) on page 65. and Section 10.5.3 Read Manufacturer / Device ID (90h) on page 79.
43. The 9Fh instruction is followed by the output of the Manufacturer ID byte then Device ID byte then the Capacity byte. See Section 29 Command Set (ID, Security Commands) on page 65 and Section 10.5.4 Read JEDEC ID (9Fh) on page 79.

8.6.2 Serial Flash Discoverable Parameters (SFDP)

A Read SFDP (5Ah) command to read a JEDEC standard JESD216) defined device information structure is supported. The information is stored in Security Register 0 and described in Section 8.4 Security Register 0 — Serial Flash Discoverable Parameters (SFDP — JEDEC JESD216B) on page 39.

Not Recommended for New Design

9. Functional Description

9.1 SPI Operations

9.1.1 Standard SPI Commands

The S25FL1-K is accessed through an SPI compatible bus consisting of four signals: Serial Clock (SCK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI commands use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge SCK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the serial flash. For Mode 0, the SCK signal is normally low on the falling and rising edges of CS#. For Mode 3, the SCK signal is normally high on the falling and rising edges of CS#.

9.1.2 Dual SPI Commands

The S25FL1-K supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” commands. These commands allow data to be transferred to or from the device at two to three times the rate of ordinary serial flash devices. The Dual SPI Read commands are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

9.1.3 Quad SPI Commands

The S25FL1-K supports Quad SPI operation when using the “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)” commands. These commands allow data to be transferred to or from the device four to six times the rate of ordinary serial flash. The Quad Read commands offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI commands the SI and SO pins become bidirectional IO0 and IO1, and the WP# and HOLD# pins become IO2 and IO3 respectively. Quad SPI commands require the nonvolatile or volatile Quad Enable bit (QE) in Status Register-2 to be set.

9.1.4 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# (IO3) signal allows the device interface operation to be paused while it is actively selected (when CS# is low). The Hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, if the page buffer is only partially written when a priority interrupt requires use of the SPI bus, the Hold function can save the state of the interface and the data in the buffer so programming command can resume where it left off once the bus is available again. The Hold function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a Hold condition, the device must be selected with CS# low. A Hold condition will activate on the falling edge of the HOLD# signal if the SCK signal is already low. If the SCK is not already low the Hold condition will activate after the next falling edge of SCK. The Hold condition will terminate on the rising edge of the HOLD# signal if the SCK signal is already low. If the SCK is not already low the Hold condition will terminate after the next falling edge of SCK. During a Hold condition, the Serial Data Output, (SO) or IO0 and IO1, are high impedance and Serial Data Input, (SI) or IO0 and IO1, and Serial Clock (SCK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the Hold operation to avoid resetting the internal logic state of the device.

Not Recommended for New Design

9.2 Write Protection

Applications that use nonvolatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the S25FL1-K provides several means to protect the data from inadvertent program or erase.

9.2.1 Write Protect Features

- Device resets when V_{CC} is below threshold
- Time delay write disable after Power-Up
- Write enable / disable commands and automatic write disable after erase or program
- Command length protection
  - All commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored
- Software and Hardware write protection using Status Register control
  - WP# input protection
  - Lock Down write protection until next power-up or Software Reset
  - One-Time Program (OTP) write protection
- Write Protection using the Deep Power-Down command

Upon power-up or at power-down, the S25FL1-K will maintain a reset condition while V_{CC} is below the threshold value of VWI, (see Figure 18. Power-Up Timing and Voltage Levels on page 24). While reset, all operations are disabled and no commands are recognized. During power-up and after the V_{CC} voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Registers commands. Note that the chip select pin (CS#) must track the V_{CC} supply level at power-up until the V_{CC}-min level and t_{VSL} time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Registers command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled main flash array write protection is facilitated using the Write Status Registers command to write the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits.

The BP method allows a portion as small as 4-kB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. SeeStatus Registers on page 50. for further information.

Additionally, the Deep Power-Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep-Power-Down (RES ABh) command. Thus, preventing any program or erase during the DPD state.

Not Recommended for New Design

9.3 Status Registers

The Read and Write Status Registers commands can be used to provide status and control of the flash memory device.

10. Commands

The command set of the S25FL1-K is fully controlled through the SPI bus (see Table 26 to Table 29 on page 65). Commands are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the SI input provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Commands vary in length from a single byte to several bytes. Each command begins with an instruction code and may be followed by address bytes, a mode byte, read latency (dummy / don't care) cycles, or data bytes. Commands are completed with the rising edge of edge CS#. Clock relative sequence diagrams for each command are included in the command descriptions. All read commands can be completed after any data bit. However, all commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, all commands except for Read Status Register and Suspend commands will be ignored until the program or erase cycle has completed. When the Status Register is being written, all commands except for Read Status Register will be ignored until the Status Register write operation has completed.

Table 26. Command Set (Configuration, Status, Erase, Program Commands [44])

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Status Register-1	05h	SR1[7:0] [45] [47]				
Read Status Register-2	35h	SR2[7:0] [45] [47]				
Read Status Register-3	33h	SR3[7:0] [45]				
Write Enable	06h					
Write Enable for Volatile Status Register	50h					
Write Disable	04h					
Write Status Registers	01h	SR1[7:0]	SR2[7:0]	SR3[7:0]		
Set Burst with Wrap	77h	xxh	xxh	xxh	SR3[7:0] [46]	
Set Block / Pointer Protection **(S25FL132K / S25FL164K)**	39h	A23–A16	A15–A10, x, x	xxh		
Page Program	02h	A23–A16	A15–A8	A7–A0	D7–D0	
Sector Erase (4 kB)	20h	A23–A16	A15–A8	A7–A0		
Block Erase (64 kB)	D8h	A23–A16	A15–A8	A7–A0		
Chip Erase	C7h / 60h					
Erase / Program Suspend	75h					
Erase / Program Resume	7Ah					

Not Recommended for New Design

Notes

44. Data bytes are shifted with Most Significant Bit First. Byte fields with data in brackets '[]' indicate data being read from the device on the SO pin.
45. Status Register contents will repeat continuously until CS# terminates the command.
46. Set Burst with Wrap Input format to load SR3. See Table 17 on page 51.
    IO0 = x, x, x, x, x, W4, x]
    IO1 = x, x, x, x, x, W5, x]
    IO2 = x, x, x, x, x, W6 x]
    IO3 = x, x, x, x, x, x,x
47. When changing the value of any single bit, read all other bits and rewrite the same value to them.

Table 27. Command Set (Read Commands)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0, …)	
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)
Fast Read Dual Output	3Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …) [48]
Fast Read Quad Output	6Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …) [50]
Fast Read Dual I/O	BBh	A23–A8 [49]	A7–A0, M7–M0 [49]	(D7–D0, …) [48]		
Fast Read Quad I/O	EBh	A23–A0, M7–M0 [51]	(x,x,x,x, D7–D0, …) [52]	(D7–D0, …) [50]		
Continuous Read Mode Reset [53]	FFh	FFh				

Notes

48. Dual Output data
    IO0 = (D6, D4, D2, D0)
    IO1 = (D7, D5, D3, D1)
49. Dual Input Address
    IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
    IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
50. Quad Output Data
    IO0 = (D4, D0, …..)
    IO1 = (D5, D1, …..)
    IO2 = (D6, D2, …..)
    IO3 = (D7, D3, …..)
51. Quad Input Address
    IO0 = A20, A16, A12, A8, A4, A0, M4, M0
    IO1 = A21, A17, A13, A9, A5, A1, M5, M1
    IO2 = A22, A18, A14, A10, A6, A2, M6, M2
    IO3 = A23, A19, A15, A11, A7, A3, M7, M3
52. Fast Read Quad I/O Data
    IO0 = (x, x, x, x, D4, D0, …..)
    IO1 = (x, x, x, x, D5, D1, …..)
    IO2 = (x, x, x, x, D6, D2, …..)
    IO3 = (x, x, x, x, D7, D3, …..)
53. This command is recommended when using the Dual or Quad "Continuous Read Mode" feature. See Section 10.4.3 and Section 10.4.3 on page 76 for more information.

Table 28. Command Set (Reset Commands)

Command Name	Byte 1 (Instruction)	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Software Reset Enable	66h					
Software Reset	99h					
Continuous Read Mode Reset [54]	FFh	FFh				

Note

54. This command is recommended when using the Dual or Quad "Continuous Read Mode" feature. See Section 10.4.3 and Section 10.4.3 on page 76 for more information.

Not Recommended for New Design

Table 29. Command Set (ID, Security Commands)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Deep Power-down	B9h					
Release Power down / Device ID	ABh	dummy	dummy	dummy	Device ID [55]	
Manufacturer / Device ID [56]	90h	A23–A16	A15–A8	A7–A0	Manufacturer	Device ID
JEDEC ID	9Fh	Manufacturer	Memory Type	Capacity		
Read SFDP Register / Read Unique ID Number	5Ah	00h	00h	A7–A0	dummy	(D7–D0, …)
Read Security Registers [57]	48h	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)
Erase Security Registers [57]	44h	A23–A16	A15–A8	A7–A0		
Program Security Registers [57]	42h	A23–A16	A15–A8	A7–A0	D7–D0, …	

Notes

55. The Device ID will repeat continuously until CS# terminates the command.
56. See Section 8.6.1 Legacy Device Identification Commands on page 60 for Device ID information. The 90h instruction is followed by an address. Address = 0 selects Manufacturer ID as the first returned data as shown in the table. Address = 1 selects Device ID as the first returned data followed by Manufacturer ID.
57. Security Register Address:
    Security Register 0: A23-16 = 00h; A15-8 = 00h; A7-0 = byte address
    Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
    Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
    Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

    Security Register 0 is used to store the SFDP parameters and is always programmed and locked by Cypress.

Not Recommended for New Design

10.1 Configuration and Status Commands

10.1.1 Read Status Registers (05h), (35h), (33h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by driving CS# low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2, or 33h for Status Register-3, into the SI pin on the rising edge of SCK. The Status Register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first as shown in Figure 30. The Status Register bits are shown in Section 8.5 Status Registers on page 50.

The Read Status Register-1 (05h) command may be used at any time, even while a Program, Erase, or Write Status Registers cycle is in progress. This allows the BUSY status bit to be checked to determine when the operation is complete and if the device can accept another command. The Read Status Register-2 (35h), and Read Status Registers (33h) may be used only when the device is in standby, not busy with an embedded operation.

Status Registers can be read continuously as each repeated data output delivers the updated current value of each status register. Example: using the instruction code “05h” for Read Status Register-1, the first output of eight bits may show the device is busy, SR1[0]=1. By continuing to hold CS# low, the updated value of SR1 will be shown in the next byte output. This repeated reading of SR1can continue until the system detects the Busy bit has changed back to ready status in one of the status bytes being read out. The Read Status Register commands are completed by driving CS# high.

Figure 30. Read Status Register Command Sequence Diagram for 05h and 35h

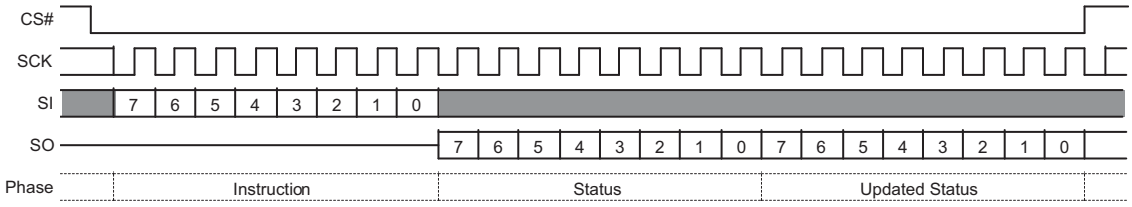
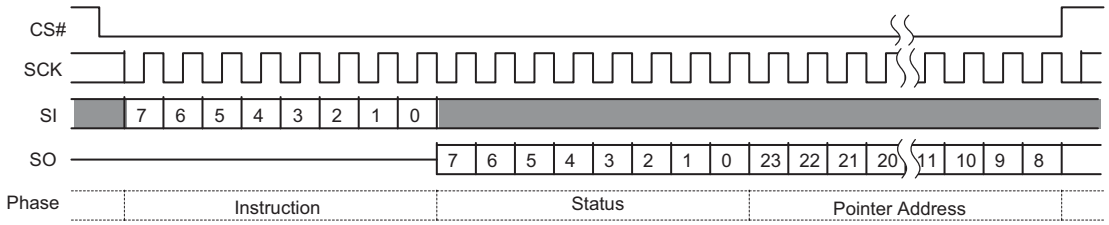


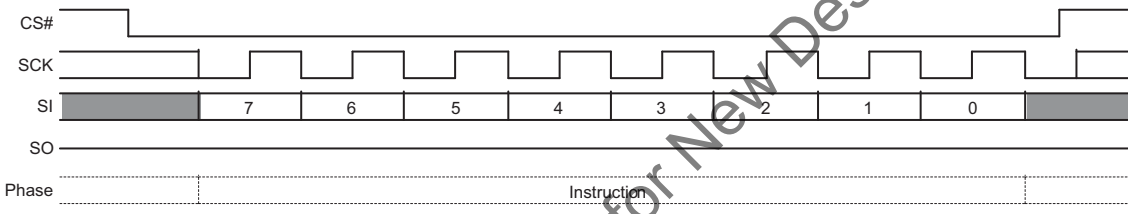
Figure 31. Read Status Register-3 Command Sequence Diagram for 33h — S25FL132K / S25FL164K



10.1.2 Write Enable (06h)

The Write Enable command (Figure 32) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Registers and Erase / Program Security Registers command. The Write Enable command is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (SI) pin on the rising edge of SCK, and then driving CS# high.

Figure 32. Write Enable (WREN 06h) Command Sequence

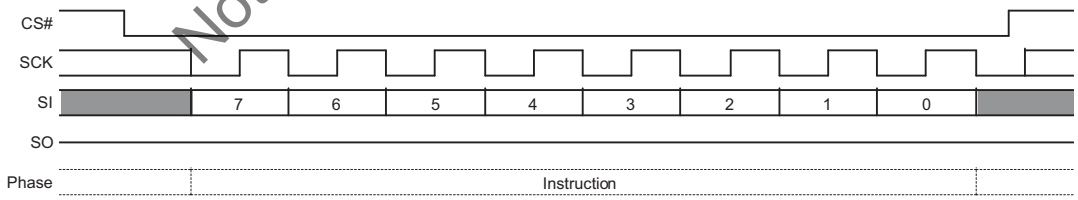


Not Recommended for New Design

10.1.3 Write Enable for Volatile Status Register (50h)

The nonvolatile Status Register bits described in Section 8.5 Status Registers on page 50 can also be written to as volatile bits. During power up reset, the nonvolatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical nonvolatile bit write cycles or affecting the endurance of the Status Register nonvolatile bits. To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued and immediately followed by the Write Status Registers (01h) command. Write Enable for Volatile Status Register command (Figure 33) will not set the Write Enable Latch (WEL) bit, it is only valid for the next following Write Status Registers command, to change the volatile Status Register bit values.

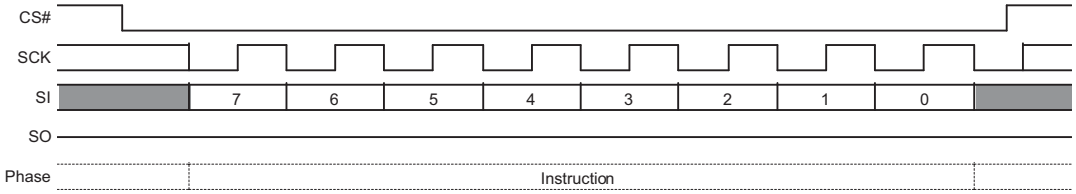
Figure 33. Write Enable for Volatile Status Register Command Sequence



10.1.4 Write Disable (04h)

The Write Disable command resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable command is entered by driving CS# low, shifting the instruction code “04h” into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Registers, Erase / Program Security Registers, Page Program, Sector Erase, Block Erase and Chip Erase commands.

Figure 34. Write Disable (WRDI 04h) Command Sequence



10.1.5 Write Status Registers (01h)

The Write Status Registers command allows the Status Registers to be written. Only nonvolatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (SR1[7:2]) CMP, LB3, LB2, LB1, QE, SRP1 (SR2[6:0]), and the volatile bits SR3[6:0] can be written. All other Status Register bit locations are read-only and will not be affected by the Write Status Registers command. LB3-0 are nonvolatile OTP bits; once each is set to 1, it can not be cleared to 0. The Status Register bits are shown in Section 8.5 Status Registers on page 50. Any reserved bits should only be written to their default value.

To write nonvolatile Status Register bits, a standard Write Enable (06h) command must previously have been executed for the device to accept the Write Status Registers Command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CS# low, sending the instruction code “01h”, and then writing the Status Register data bytes as illustrated in Figure 35.

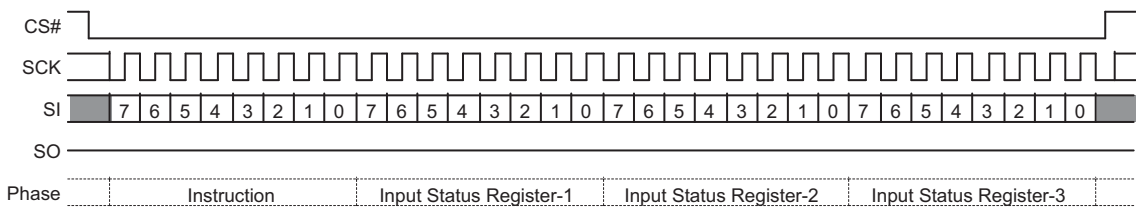
To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) command must have been executed prior to the Write Status Registers command (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1, LB0 can not be changed because of the OTP protection for these bits. Upon power-off, the volatile Status Register bit values will be lost, and the nonvolatile Status Register bit values will be restored when power on again.

To complete the Write Status Registers command, the CS# pin must be driven high after the eighth bit of a data value is clocked in (CS# must be driven high on an 8-bit boundary). If this is not done the Write Status Registers command will not be executed. If CS# is driven high after the eighth clock the CMP and QE bits will be cleared to 0 if the SRP1 bit is 0. The SR2 bits are unaffected if SRP1 is 1. If CS# is driven high after the eighth or sixteenth clock, the SR3 bits will not be affected.

During nonvolatile Status Register write operation (06h combined with 01h), after CS# is driven high at the end of the Write Status Registers command, the self-timed Write Status Registers operation will commence for a time duration of t_W (see Section 5.8 AC Electrical Characteristics on page 25). While the Write Status Registers operation is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Registers operation and a 0 when the operation is finished and ready to accept other commands again. After the Write Status Registers operation has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high at the end of the Write Status Registers command, the Status Register bits will be updated to the new values within the time period of t_{SHSL2} (see Section 5.8 AC Electrical Characteristics on page 25). BUSY bit will remain 0 during the Status Register bit refresh period. Refer to Section 8.5 Status Registers on page 50 for detailed Status Register bit descriptions.

Figure 35. Write Status Registers Command Sequence Diagram



Not Recommended for New Design

10.2 Program and Erase Commands

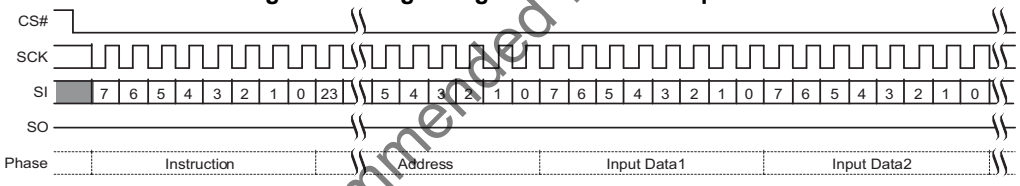
10.2.1 Page Program (02h)

The Page Program command allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Page Program Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 36. Page Program Command Sequence on page 68.

If an entire 256-byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After CS# is driven high, the self-timed Page Program command will commence for a time duration of t_{PP} (Section 5.8 AC Electrical Characteristics on page 25). While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 36. Page Program Command Sequence



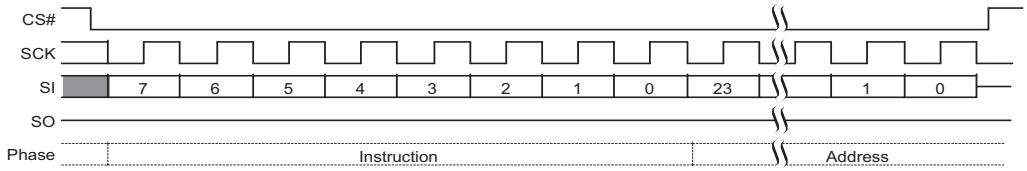
Not Recommended for New Design

10.2.2 Sector Erase (20h)

The Sector Erase command sets all memory within a specified sector (4 kbytes) to the erased state of all 1’s (FFh). A Write Enable command must be executed before the device will accept the Sector Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) SeeSupply and Signal Ground (V_{SS}) on page 10. The Sector Erase command sequence is shown in Figure 37 on page 69.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase command will not be executed. After CS# is driven high, the self-timed Sector Erase command will commence for a time duration of t_{SE}. Section 5.8 AC Electrical Characteristics on page 25 While the Sector Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase command will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (Table 20, FL132K Block Protection (CMP = 0) on page 54).

Figure 37. Sector Erase Command Sequence

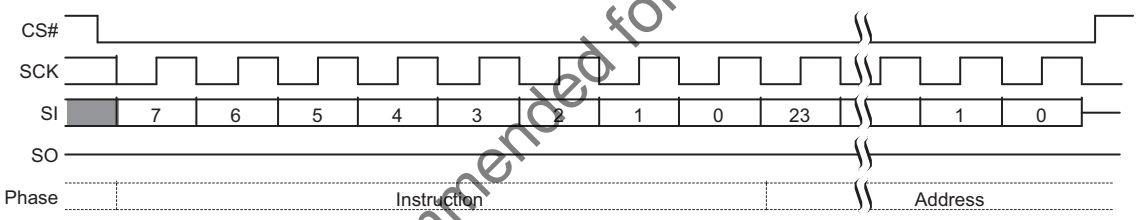


10.2.3 64-kB Block Erase (D8h)

The Block Erase command sets all memory within a specified block (64 kbytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0) SeeSupply and Signal Ground (V_{SS}) on page 10. The Block Erase command sequence is shown in Figure 38.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After CS# is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE} (see Section 5.8 AC Electrical Characteristics on page 25). While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Section 8.5 Status Registers on page 50).

Figure 38. 64-kB Block Erase Command Sequence



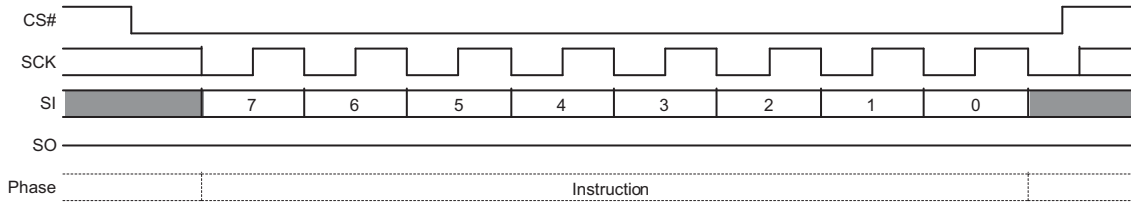
Not Recommended for New Design

10.2.4 Chip Erase (C7h / 60h)

The Chip Erase command sets all memory within the device to the erased state of all 1’s (FFh). A Write Enable command must be executed before the device will accept the Chip Erase command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase command sequence is shown in Figure 39.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command will not be executed. After CS# is driven high, the self-timed Chip Erase command will commence for a time duration of t_{CE} (Section 5.8 AC Electrical Characteristics on page 25). While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Section 8.5 Status Registers on page 50).

Figure 39. Chip Erase Command Sequence



10.2.5 Erase / Program Suspend (75h)

The Erase / Program Suspend command allows the system to interrupt a Sector or Block Erase operation, then read from or program data to any other sector. The Erase / Program Suspend command also allows the system to interrupt a Page Program operation and then read from any other page or erase any other sector or block. The Erase / Program Suspend command sequence is shown in Figure 40. Erase / Program Suspend Command Sequence on page 71.

The Write Status Registers command (01h), Program Security Registers (42h), and Erase commands (20h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend command is ignored. The Write Status Registers command (01h), Erase Security Registers (44h), and Program commands (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program operation.

Table 30. Commands Accepted During Suspend

Operation Suspended	Command Allowed	Instruction
Program or Erase	Read Data	03h
Program or Erase	Fast Read	0Bh
Program or Erase	Fast Read Dual Output	3Bh
Program or Erase	Fast Read Quad Output	6Bh
Program or Erase	Fast Read Dual I/O	BBh
Program or Erase	Fast Read Quad I/O	EBh
Program or Erase	Continuous Read Mode Reset	FFh
Program or Erase	Read Status Register-1	05h
Program or Erase	Read Status Register-2	35h
Program or Erase	Write Enable	06h
Erase	Page Program	02h
Program	Sector Erase	20h
Program	Block Erase	D8h
Program or Erase	Erase / Program Resume	7Ah

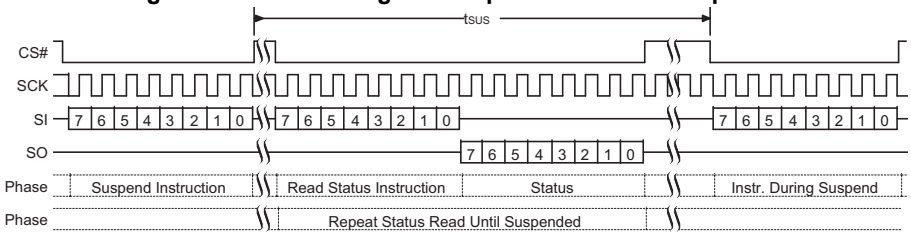
Not Recommended for New Design

The Erase / Program Suspend command 75h will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend command will be ignored by the device. Program or Erase command for the sector that is being suspended will be ignored.

A maximum of time of t_{SUS} (Section 5.8 AC Electrical Characteristics on page 25) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within t_{SUS} and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase / Program Suspend. For a previously resumed Erase / Program operation, it is also required that the Suspend command 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume command 7Ah.

Unexpected power off during the Erase / Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques to prevent accidental power interruption, provide nonvolatile tracking of in process program or erase commands, and preserve data integrity by evaluating the nonvolatile program or erase tracking information during each system power up in order to identify and repair (re-erase and re-program) any improperly terminated program or erase operations.

Figure 40. Erase / Program Suspend Command Sequence

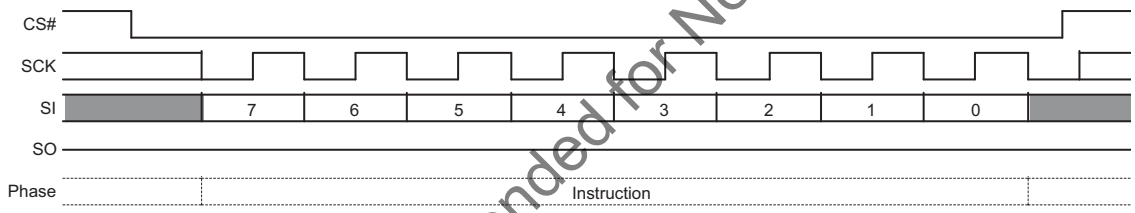


10.2.6 Erase / Program Resume (7Ah)

The Erase / Program Resume command “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase / Program Suspend. The Resume command “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After the Resume command is issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume command “7Ah” will be ignored by the device. The Erase / Program Resume command sequence is shown in Figure 41.

It is required that a subsequent Erase / Program Suspend command not to be issued within a minimum of time of “t_{SUS}” following a Resume command.

Figure 41. Erase / Program Resume Command Sequence



Not Recommended for New Design

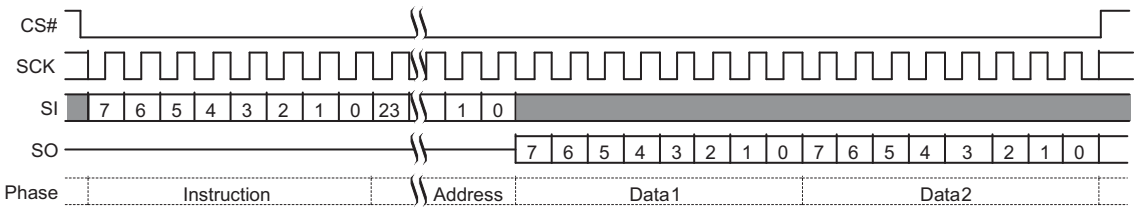
10.3 Read Commands

10.3.1 Read Data (03h)

The Read Data command allows one or more data bytes to be sequentially read from the memory. The command is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the SI pin. The code and address bits are latched on the rising edge of the SCK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving CS# high.

The Read Data command sequence is shown in Figure 42. If a Read Data command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle. The Read Data command allows clock rates from DC to a maximum of f_R (see Section 5.8 AC Electrical Characteristics on page 25).

Figure 42. Read Data Command Sequence

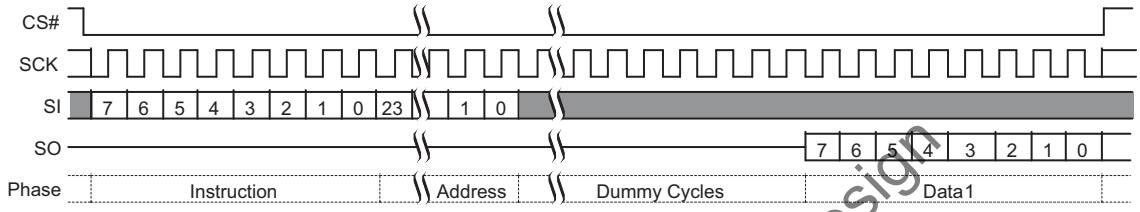


10.3.2 Fast Read (0Bh)

The Fast Read command is similar to the Read Data command except that it can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 43. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SI pin is a “don’t care.”

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 24, Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V on page 59.

Figure 43. Fast Read Command Sequence



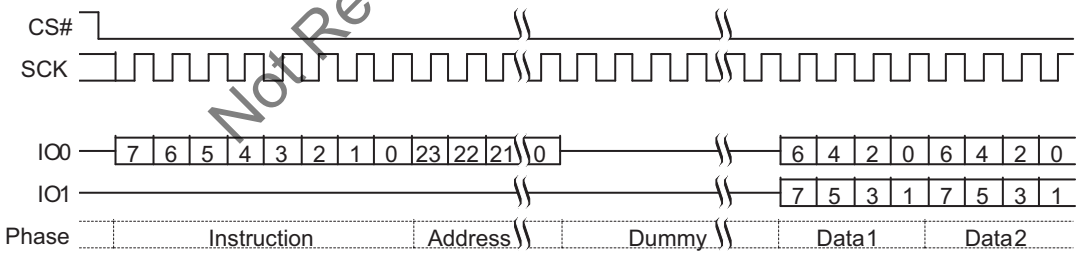
10.3.3 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) command is similar to the standard Fast Read (0Bh) command except that data is output on two pins; IO0 and IO1. This allows data to be transferred from the S25FL1-K at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read command, the Fast Read Dual Output command can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 44. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care.” However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 24, Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V on page 59.

Figure 44. Fast Read Dual Output Command Sequence



Not Recommended for New Design

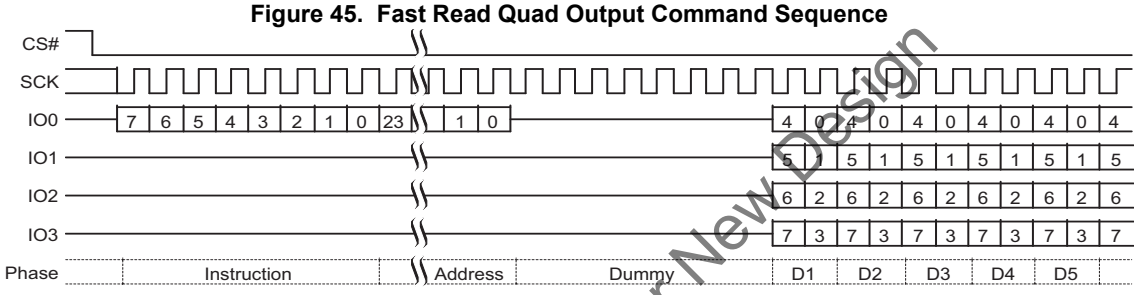
10.3.4 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) command is similar to the Fast Read Dual Output (3Bh) command except that data is output on four pins, IO0, IO1, IO2, and IO3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Command (Status Register bit QE must equal 1). The Fast Read Quad Output Command allows data to be transferred from the S25FL1-K at four times the rate of standard SPI devices.

The Fast Read Quad Output command can operate at higher frequency than the traditional Read Data command. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 45. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care.” However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

When variable read latency is enabled, the number of dummy cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 24, Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V on page 59.

Figure 45. Fast Read Quad Output Command Sequence



Not Recommended for New Design

10.3.5 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) command allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) command but with the capability to input the Address bits (A23-0) two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

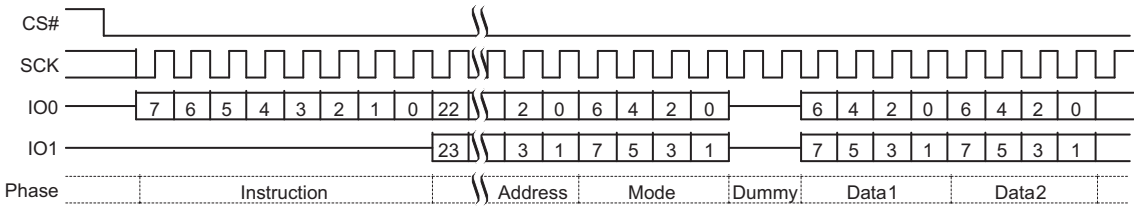
Fast Read Dual I/O with “Continuous Read Mode”

The Fast Read Dual I/O command can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 46. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O command (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 47. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset command can also be used to reset (M7-0) before issuing normal commands (see SeeContinuous Read Mode Reset (FFh or FFFFh) on page 76.).

When variable read latency is enabled, the number of latency (Mode + Dummy) cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See Table 24, Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V on page 59. Note that the legacy Read Dual I/O command has four Mode cycles and no Dummy cycles for a total of four latency cycles, Enabling the variable read latency allows for the addition of more read latency to enable higher frequency operation of the Dual I/O command.

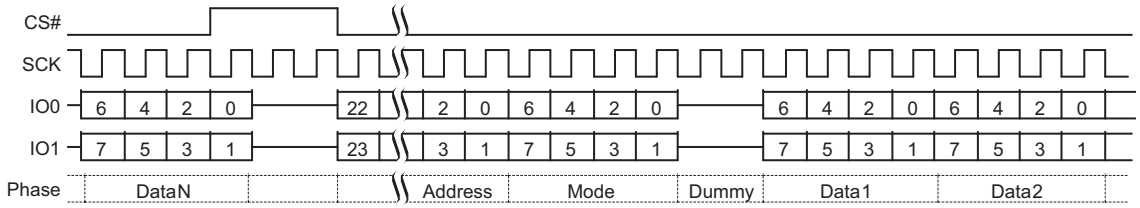
Figure 46. Fast Read Dual I/O Command Sequence (Initial command or previous M5-4 ≠ 10)



Note

58. Least significant 4 bits of Mode are don't care and it is optional for the host to drive these bits. The host may turn off drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.

Figure 47. Fast Read Dual I/O Command Sequence (Previous command set M5-4 = 10)



10.3.6 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Command.

Fast Read Quad I/O with "Continuous Read Mode"

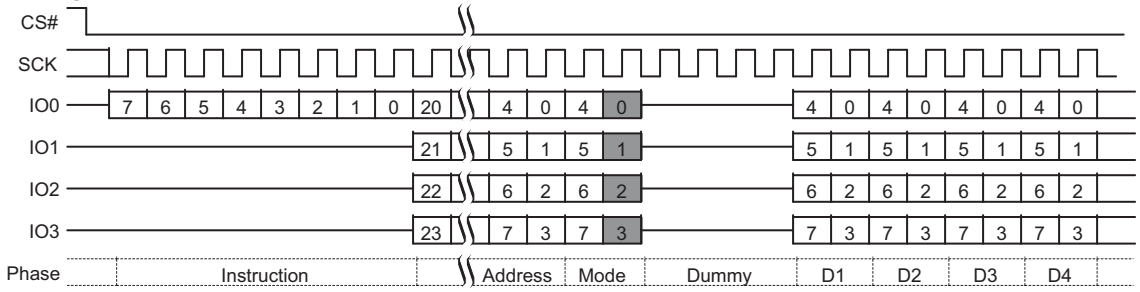
The Fast Read Quad I/O command can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 48. Fast Read Quad I/O Command Sequence (Initial command or previous M5-4 ≠10) on page 74. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 49. Fast Read Quad I/O Command Sequence (Previous command set M5-4 = 10) on page 75. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset command can also be used to reset (M7-0) before issuing normal commands (see Section 10.4.3 Continuous Read Mode Reset (FFh or FFFFh) on page 76).

When variable read latency is enabled, the number of latency (Mode + Dummy) cycles is set by the Latency Control value in SR3 to optimize the latency for the frequency in use. See. Table 24, Latency Cycles Versus Frequency for -40°C to 85°C/105°C at 2.7V to 3.6V on page 59. Note that the legacy Read Quad I/O command has two Mode cycles plus four Dummy cycles for a total of six latency cycles, Enabling the variable read latency allows for the addition of more read latency to enable higher frequency operation of the Quad I/O command.

Not Recommended for New Design

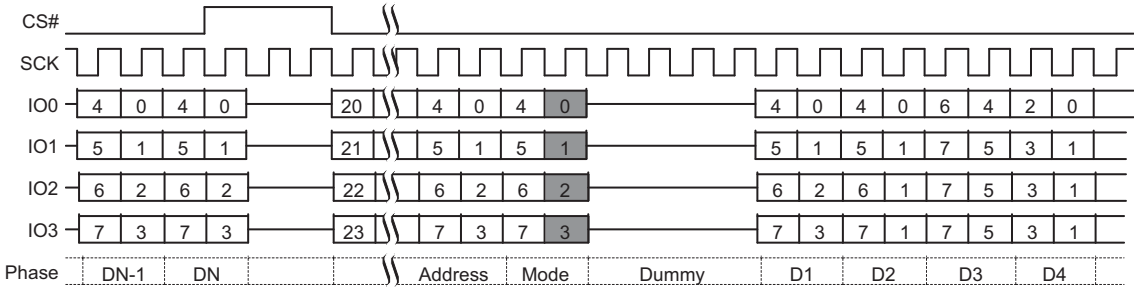
Figure 48. Fast Read Quad I/O Command Sequence (Initial command or previous M5-4 ≠10)



Note

59. Least significant 4 bits of Mode are don't care and it is optional for the host to drive these bits. The host may turn off drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.

Figure 49. Fast Read Quad I/O Command Sequence (Previous command set M5-4 = 10)



Fast Read Quad I/O with "16 / 32 / 64-Byte Wrap Around"

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" command prior to EBh. The "Set Burst with Wrap" command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 16 / 32 / 64-byte section of data. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 16 / 32 / 64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16 / 32 / 64-bytes) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See Section 10.3.7 Set Burst with Wrap (77h) on page 75.

Not Recommended for New Design

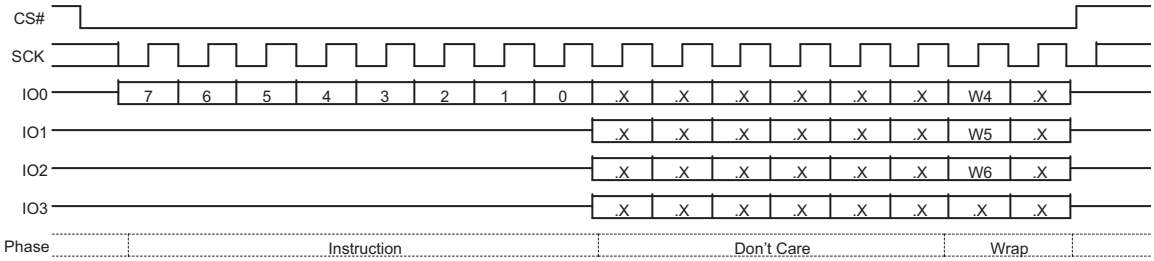
10.3.7 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) command is used in conjunction with "Fast Read Quad I/O" commands to access a fixed length and alignment of 8 / 16 / 32 / 64-bytes of data. Certain applications can benefit from this feature and improve the overall system code execution performance. This command loads the SR3 bits.

Similar to a Quad I/O command, the Set Burst with Wrap command is initiated by driving the CS# pin low and then shifting the instruction code "77h" followed by 24-dummy bits and 8 "Wrap Bits", W7-0. The command sequence is shown in Figure 50. Set Burst with Wrap Command Sequence on page 75. Wrap bit W7 and the lower nibble W3-0 are not used. See Status Register-3 (SR3[6:4]) for the encoding of W6-W4 in Section 8.5 Status Registers on page 50.

Once W6-4 is set by a Set Burst with Wrap command, all the following "Fast Read Quad I/O" commands will use the W6-4 setting to access the 8 / 16 / 32 / 64-byte section of data. Note, Status Register-2 QE bit (SR2[1]) must be set to 1 in order to use the Fast Read Quad I/O and Set Burst with Wrap commands. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Software Reset command or a Set Burst with Wrap command to reset W4 = 1 prior to any normal Read commands since S25FL1-K does not have a hardware Reset Pin.

Figure 50. Set Burst with Wrap Command Sequence



10.4 Reset Commands

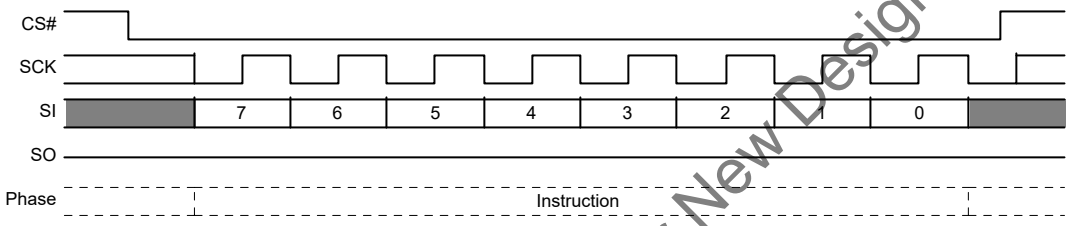
Software controlled Reset commands restore the device to its initial power up state, by reloading volatile registers from nonvolatile default values. If a software reset is initiated during a Erase, Program or writing of a Register operation the data in that Sector, Page or Register is not stable, the operation that was interrupted needs to be initiated again.

When the device is in Deep Power-Down mode it is protected from a software reset, the software reset commands are ignored and have no effect. To reset the device send the Release Power down command (ABh) and after time duration of t_{RES1} the device will resume normal operation and the Software reset commands will be accepted.

A software reset is initiated by the Software Reset Enable command (66h) followed by Software Reset command (99h) and then executed when CS# is brought high after t_{RCH} time at the end of the Software Reset instruction and requires t_{RST} time before executing the next Instruction after the Software Reset. See Figure 26. Software Reset Input Timing on page 28

Note: The t_{RCH} is a Cypress specific parameter and CS# must be brought high after t_{RCH} time, if not the Software Reset will not be executed.

Figure 51. Software Reset Command Sequence



Not Recommended for New Design

10.4.1 Software Reset Enable (66h)

The Reset Enable (66h) command is required immediately before a software reset command (99h) such that a software reset is a sequence of the two commands. Any command other than Reset (99h) following the Reset Enable (66h) command, will clear the reset enable condition and prevent a later RST command from being recognized.

10.4.2 Software Reset (99h)

The Reset (99h) command immediately following a Reset Enable (66h) command, initiates the software reset process. Any command other than Reset (99h) following the Reset Enable (66h) command, will clear the reset enable condition and prevent a later Reset (99h) command from being recognized.

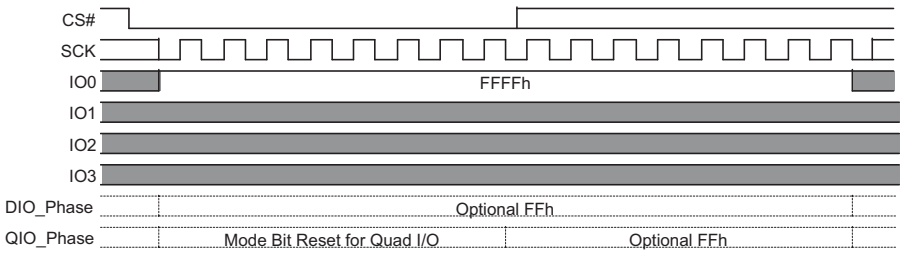
10.4.3 Continuous Read Mode Reset (FFh or FFFFh)

The “Continuous Read Mode” bits are used in conjunction with “Fast Read Dual I/O” and “Fast Read Quad I/O” commands to provide the highest random Flash memory access rate with minimum SPI instruction overhead, thus allowing more efficient XIP (execute in place) with this device family. A device that is in a continuous high performance read mode may not recognize any normal SPI command or the software reset command may not be recognized by the device. It is recommended to use the Continuous Read Mode Reset command after a system Power on Reset or, before sending a software reset, to ensure the device is released from continuous high performance read mode.

The “Continuous Read Mode” bits M7-0 are set by the Dual/Quad I/O Read commands. M5-4 are used to control whether the 8-bit SPI instruction code (BBh or EBh) is needed or not for the next command. When M5-4 = (1,0), the next command will be treated the same as the current Dual/Quad I/O Read command without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI command mode, in which all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

The Continuous Read Mode Reset command (FFh or FFFFh) can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in Figure 52.

Figure 52. Continuous Read Mode Reset for Fast Read Dual or Quad I/O



Notes

60. To reset “Continuous Read Mode” during Quad I/O operation, only eight clocks are needed. The instruction is “FFh”.
61. To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFh”.

10.4.4 Host System Reset Commands

Since S25FL1-K does not have a hardware Reset pin, if the host system memory controller resets, without a complete power-down and power-up sequence, while an S25FL1-K device is set to Continuous Mode Read, the S25FL1-K device will not recognize any initial standard SPI commands from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset (FFFFh) command as the first command after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI commands to be recognized. See Section 10.4.3 Continuous Read Mode Reset (FFh or FFFFh) on page 76.

If Burst Wrap Mode is used, it is also recommended to issue a Set Burst with Wrap (77h) command that sets the W4 bit to one as the second command after a system Reset. Doing so will release the device from the Burst Wrap Mode and allow standard sequential read SPI command operation. See Section 10.3.7 Set Burst with Wrap (77h) on page 75.

Issuing these commands immediately after a non-power-cycle (warm) system reset, ensures the device operation is consistent with the power-on default device operation. The same commands may also be issued after device power-on (cold) reset so that system reset code is the same for warm or cold reset.

Not Recommended for New Design

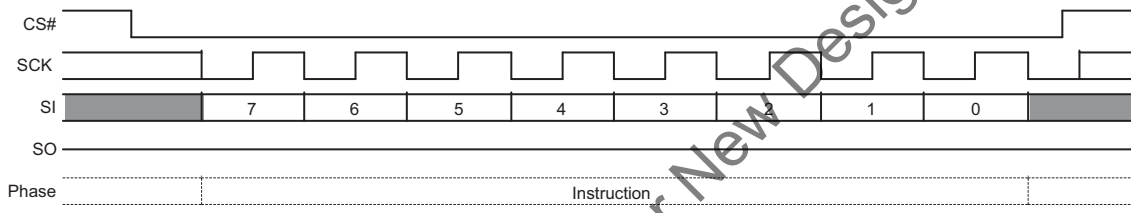
10.5 ID and Security Commands

10.5.1 Deep-Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep-Power-Down command. The lower power consumption makes the Deep-Power-Down (DPD) command especially useful for battery powered applications (see I_{CC1} and I_{CC2} in Section 5.8 AC Electrical Characteristics on page 25). The command is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 53.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep-Power-Down command will not be executed. After CS# is driven high, the power-down state will entered within the time duration of t_{DP} (Section 5.8 AC Electrical Characteristics on page 25). While in the power-down state only the Release from Deep-Power-Down / Device ID command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

Figure 53. Deep Power-Down Command Sequence



Not Recommended for New Design

10.5.2 Release from Deep-Power-Down / Device ID (ABh)

The Release from Deep-Power-Down / Device ID command is a multi-purpose command. It can be used to release the device from the deep-power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the deep-power-down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 54. Release from deep-power-down will take the time duration of t_{RES1} (Section 5.8 AC Electrical Characteristics on page 25) before the device will resume normal operation and other commands are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the deep power-down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCK with most significant bit (MSB) first. The Device ID values for the S25FL1-K is listed in Section 8.6.1 Legacy Device Identification Commands on page 60. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the deep-power-down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 55, except that after CS# is driven high it must remain high for a time duration of t_{RES2}. After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Deep-Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 54. Release from Deep-Power-Down Command Sequence

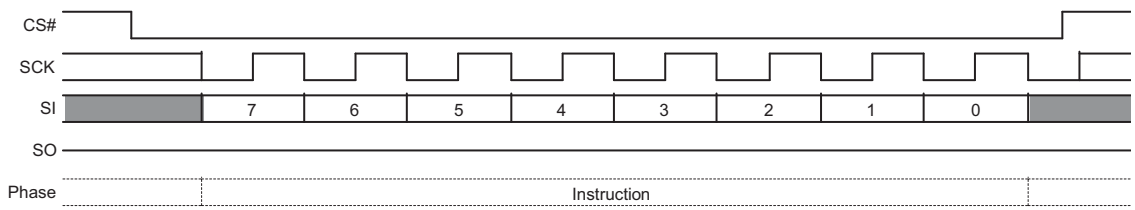
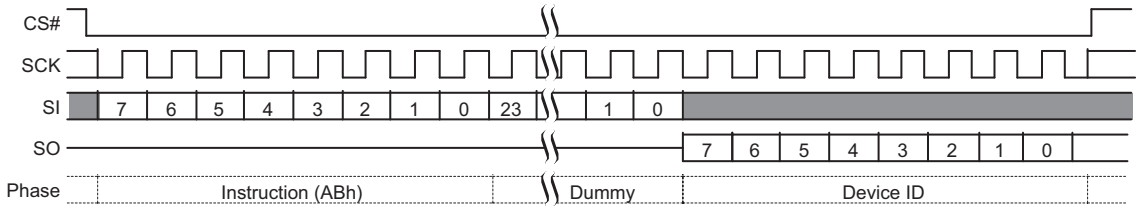


Figure 55. Read Electronic Signature (RES ABh) Command Sequence

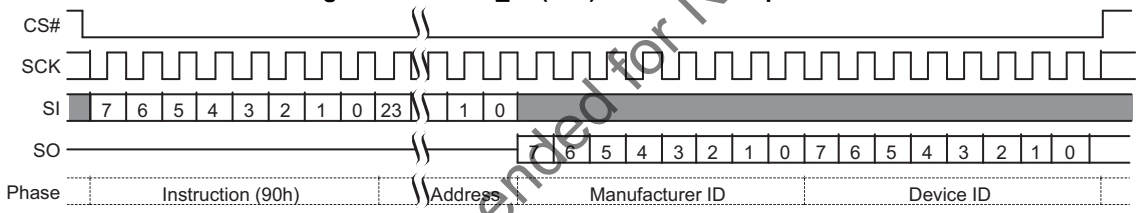


10.5.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer / Device ID command is an alternative to the Release from Deep-Power-Down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer / Device ID command is very similar to the Release from Deep-Power-Down / Device ID command. The command is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 56. The Device ID values for the S25FL1-K is listed in Section 8.6.1 Legacy Device Identification Commands on page 60. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

Figure 56. READ_ID (90h) Command Sequence

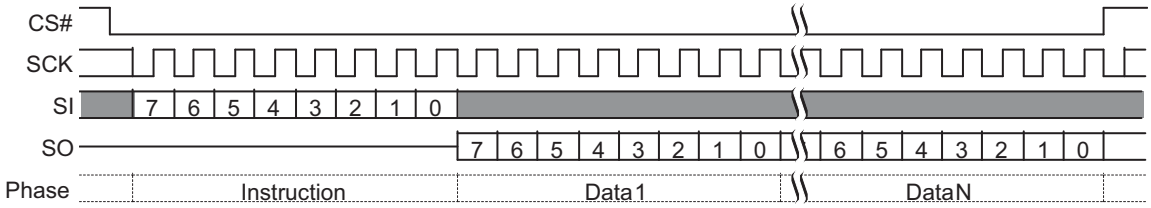


Not Recommended for New Design

10.5.4 Read JEDEC ID (9Fh)

For compatibility reasons, the S25FL1-K provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The command is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 57. For memory type and capacity values refer to Section 8.6.1 Legacy Device Identification Commands on page 60.

Figure 57. Read JEDEC ID Command Sequence



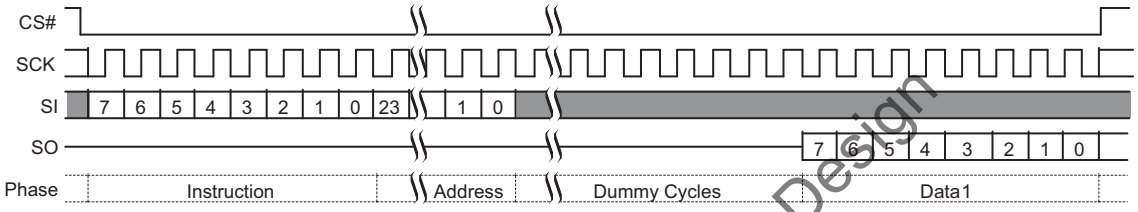
10.5.5 Read SFDP Register / Read Unique ID Number (5Ah)

The Read SFDP command is initiated by driving the CS# pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) into the SI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th SCK with most significant bit (MSB) first as shown in Figure 58. For SFDP register values and descriptions, refer to Table 8.6.2, Serial Flash Discoverable Parameters (SFDP) on page 60.

Note: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-byte SFDP Register.

The 5Ah command can also be used to access the Read Unique ID Number. This is a factory-set read-only 8-byte number that is unique to each S25FL1-K device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

Figure 58. Read SFDP Register Command Sequence



Not Recommended for New Design

10.5.6 Erase Security Registers (44h)

The Erase Security Register command is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept the Erase Security Register Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the security registers.

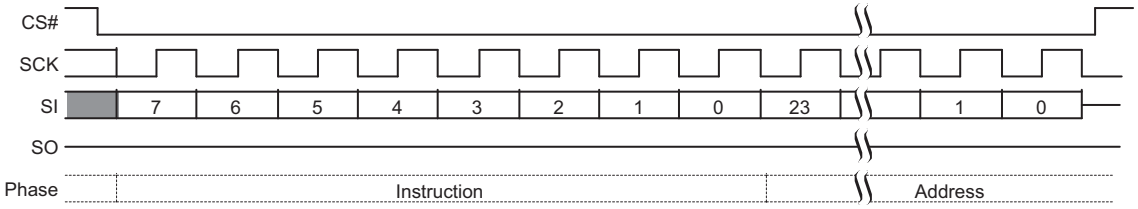
Address	A23-16	A15-8	A7-0
Security Register-1	00h	10h	xxh
Security Register-2	00h	20h	xxh
Security Register-3	00h	30h	xxh

Note

62. Addresses outside the ranges in the table have undefined results.

The Erase Security Register command sequence is shown in Figure 59. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the command will not be executed. After CS# is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (see Section 5.8 AC Electrical Characteristics on page 25). While the Erase Security Register cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and an Erase Security Register command to that register will be ignored (see Section 8.5.10 Security Register Lock Bits (LB3, LB2, LB1, LB0) on page 58).

Figure 59. Erase Security Registers Command Sequence



10.5.7 Program Security Registers (42h)

The Program Security Register command is similar to the Page Program command. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Program Security Register Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

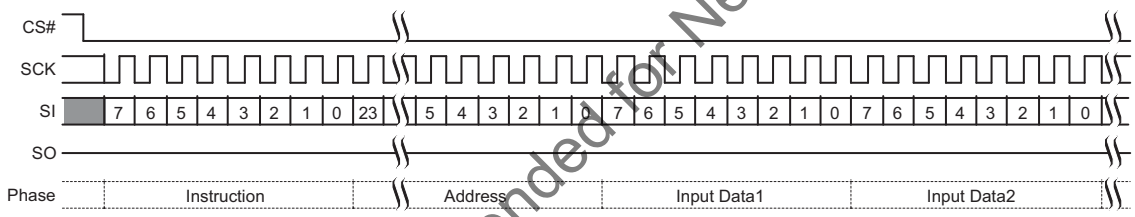
Address	A23-16	A15-8	A7-0
Security Register-1	00h	10h	Byte Address
Security Register-2	00h	20h	Byte Address
Security Register-3	00h	30h	Byte Address

Note

63. Addresses outside the ranges in the table have undefined results.

The Program Security Register command sequence is shown in Figure 60. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and a Program Security Register command to that register will be ignored (see Section 8.5.10 Security Register Lock Bits (LB3, LB2, LB1, LB0) on page 58 and Section 10.2.1 Page Program (02h) on page 68 for detail descriptions).

Figure 60. Program Security Registers Command Sequence



Not Recommended for New Design

10.5.8 Read Security Registers (48h)

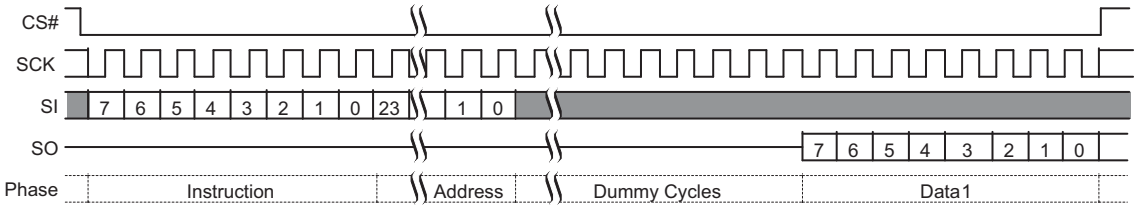
The Read Security Register command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCK pin. After the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. Locations with address bits A23-A16 not equal to zero, have undefined data. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The command is completed by driving CS# high. The Read Security Register command sequence is shown in Figure 61. If a Read Security Register command is issued while an Erase, Program, or Write cycle is in process (BUSY=1), the command is ignored and will not have any effects on the current cycle. The Read Security Register command allows clock rates from DC to a maximum of F_R (see Section 5.8 AC Electrical Characteristics on page 25).

Address	A23-16	A15-8	A7-0
Security Register-0 (SFDP)	00h	00h	Byte Address
Security Register-1	00h	10h	Byte Address
Security Register-2	00h	20h	Byte Address
Security Register-3	00h	30h	Byte Address

Note

64. Addresses outside the ranges in the table have undefined results.

Figure 61. Read Security Registers Command Sequence



10.6 Set Block / Pointer Protection (39h) — S25FL132K and S25FL164K

The user has a choice to enable one of two protection mechanisms: block protection or pointer protection. Only one protection mechanism can be enabled at one time.

The Set Block / Pointer Protection (39h) is a new command (see Figure 62) and is used to determine which one of the two protection mechanisms is enabled, and if the pointer protection mechanism is enabled, determines the pointer address. The Write Enable command must precede the Set Block / Pointer command.

After the Set Block / Pointer Protection command is given, the value of A10 in byte 3 selects whether the block protection or the pointer protection mechanism will be enabled. If A10 = 1, then the block protection mode is enabled. This is the default state, and the rest of pointer values are don't care. If A10=0, then the pointer protection is enabled, and the block protection feature is disabled. The pointer address values A9 to A0 are don't care.

If the pointer protection mechanism is enabled, a pointer address determines the boundary between the protected and the unprotected regions in the memory. The format of the Set Pointer command is the 39h instruction followed by three address bytes. For the S25FL132K, ten address bits (A21-A12) after the 39h command are used to program the nonvolatile pointer address. For the 32M, A23 – A22 are don't care. For the S25FL164K, eleven address bits (A22-A12) after the 39h command are used to program the nonvolatile pointer address. For the 64M, A23 is a don't care.

The A11 bit can be used to protect all sectors. If A11=1, then all sectors are protected, and A23 – A12 are don't cares. If A11=0, then the unprotected range will be determined by A22-A12 for the 64M and A21-A12 for the 32M. The area that is unprotected will be inclusive of the 4-kB sector selected by the pointer address.

Bit 5 (Top / Bottom) of SR1 is used to determine whether the region that will be unprotected will start from the top (highest address) or bottom (lowest address) of the memory array to the location of the pointer. If TB=0 and the 39h command is issued followed by a 24-bit address, then the 4-kB sector which includes that address and all the sectors from the bottom up (zero to higher address) will be unprotected. If TB=1 and 39h command is issued followed by a 24-bit address then the 4-kB sector which includes that address and all the sectors from the Top down (max to lower address) will be unprotected.

The SRP1 (SR2 [0]) and SRP0 (SR1 [7]) bits are used to protect the pointer address in the same way they protect SR1 and SR2. When SRP1 and SRP0 protect SR1 and SR2, the 39h command is ignored. This effectively prevents changes to the protection scheme using the existing SRP1-SRP0 mechanism – including the OTP protection option.

The 39h command is ignored during a suspend operation because the pointer address cannot be erased and re-programmed during a suspend.

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The Read Status Register-3 command 33h (see Figure 31 for 33h timing diagram) reads the contents of SR3 followed by the contents of the pointer. This allows the contents of the pointer to be read out for test and verification. The read back order is SR3, A23-A16, A15-A8. If CS# remains low, the Bytes after A15-A8 are undefined.

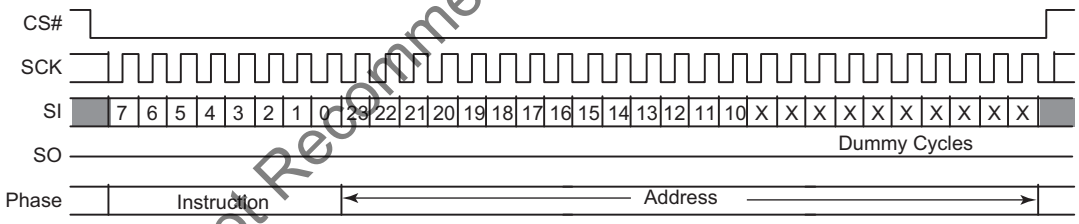
TB	A11	A10	Protect Address Range	Unprotect Address Range	Comment
x	x	1	See Block Protect Method	See Block Protect Method	A10 = 1 the block protect protection mode is enabled (this is the default state and the rest of pointer address is don't care).
0	0	0	Amax [65] to (A<22-12>+1)	A<22-12> [66] to 000000	If TB=0 and the 39h command is issued followed by a 24-bit address, then the 4-kB sector which includes that address and all the sectors from the bottom up (zero to higher address) will be unprotected.
1	0	0	(A<22-12>-1) to 000000	Amax [65] to A<22-12>	If TB=1 and 39h command is issued followed by a 24-bit address then the 4-kB sector which includes that address and all the sectors from the Top down (max to lower address) will be unprotected.
x	1	0	Amax [65] to 000000	Not Applicable	A10=0 and A11 =1 means protect all sectors and Amax-A12 are don't care.

Notes

65. Amax = 7FFFFFh for the FL164K, and 3FFFFFh for the FL132K.
66. A<21-12> for the FL132K.

Block Erase: In general, if the pointer protect scheme is active (A10=0), protect all sectors is not active (A11=0), and the pointer address points to anywhere within the block, the whole block will be protected from Block Erase even though part of the block is unprotected. The 2 exceptions where block erase goes through is if the pointer address points to the TOP sector of the block(A[15:12]=1111) if TB=0, and if the pointer points to the BOTTOM sector of the block (A[15:12]=0000) and TB=1.

Figure 62. Set Pointer Address (39h)



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11. Data Integrity

11.1 Erase Endurance

Erase Endurance

Parameter	Min	Unit
Program/Erase cycles main Flash array sector	100K	PE cycle
Program/Erase cycles Security Registers nonvolatile register array [67]	1K	PE cycle

Note

67. Each write command to a nonvolatile register causes a PE cycle on the entire nonvolatile register array. Re-writing registers with the same value doesn't cause a PE cycle. OTP bits in registers internally reside in a separate array that is not cycled.

11.2 Data Retention

Parameter	Test Conditions	Minimum Time	Unit
Data Retention Time	10K Program/Erase Cycles	20	Years
	100K Program/Erase Cycles	2	Years

11.3 Initial Delivery State

The device is shipped from Cypress with nonvolatile bits / default states set as follows:

- The entire memory array is erased: i.e. all bits are set to 1 (each byte contains FFh).
- The Unique Device ID is programmed to a random number seeded by the date and time of device test.
- The SFDP Security Register address space 0 contains the values as defined in Section 8.6.2 Serial Flash Discoverable Parameters (SFDP) on page 60. Security Register address spaces 1 to 3 are erased: i.e. all bits are set to 1 (each byte contains FFh).
- Status Register-1 contains 00h.
- Status Register-2 contains 04h.
- Status Register-3 contains 70h.

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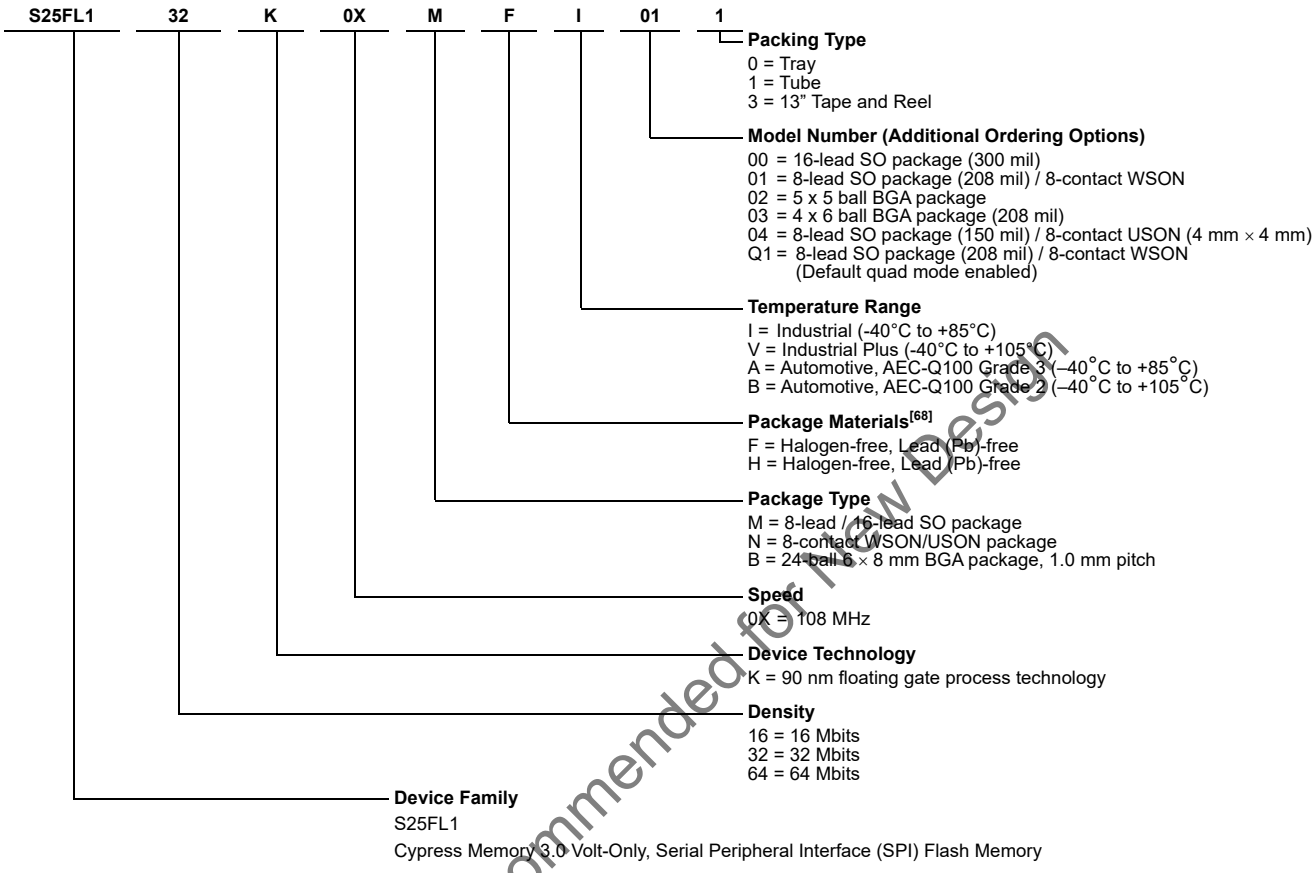
12. Ordering Information

The ordering part number is formed by a valid combination of the following:



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Note

68. Halogen free definition is in accordance with IEC 61249-2-21.

Valid Combinations — Standard

Table lists standard configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for Standard Part Numbers

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
FL116K	0X	MFI	01	0, 1, 3	FL116KIF01
			Q1		FL116KIFQ1
			04		FL116KIF4
		MFV	01		FL116KVF01
			04		FL116KVF4
		NFI	01		FL116KIF01
			Q1		FL116KIFQ1
		NFV	01		FL116KVF01
		BHI	02	0, 3	FL116KIH02
			03		FL116KIH03
		BHV	02		FL116KVH02
			03		FL116KVH03
FL132K	0X	MFI	01	0, 1, 3	FL132KIF01
			04		FL132KIF4
			Q1		FL132KIFQ1
		MFV	01		FL132KVF01
			04		FL132KVF4
		NFI	01		FL132KIF01
			04		FL132KIF04
			Q1		FL132KIFQ1
		NFV	01		FL132KVF01
			04		FL132KVF04
		BHI	02	0, 3	FL132KIH02
			03		FL132KIH03
		BHV	02		FL132KVH02
			03		FL132KVH03
FL164K	0X	MFI	00	0, 1, 3	FL164KIF00
			01		FL164KIF01
			Q1		FL164KIFQ1
		MFV	00		FL164KVF00
			01		FL164KVF01
		NFI	01		FL164KIF01
			Q1		FL164KIFQ1
		NFV	01		FL164KVF01
		BHI	02	0, 3	FL164KIH02
			03		FL164KIH03
		BHV	02		FL164KVH02
			03		FL164KVH03

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Valid Combinations — Automotive Grade / AEC-Q100

The table below lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Valid Combinations — Automotive Grade / AEC-Q100

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
FL116K	0X	MFA	01	0, 1, 3	FL116KAF01
			Q1		FL116KAFQ1
			04		FL116KAF4
		MFB	01		FL116KBF01
			04		FL116KBF4
		NFA	01		FL116KAF01
			Q1		FL116KAFQ1
		NFB	01		FL116KBF01
		BHA	02	0, 3	FL116KAH02
			03		FL116KAH03
		BHB	02		FL116KBH02
			03		FL116KBH03
FL132K	0X	MFB	01	0, 1, 3	FL132KBF01
			04		FL132KBF4
		NFA	01		FL132KAF01
			04		FL132KAF04
			Q1		FL132KAFQ1
		NFB	01		FL132KBF01
			04		FL132KBF04
		BHA	02	0, 3	FL132KAH02
			03		FL132KAH03
		BHB	02		FL132KBH02
			03		FL132KBH03
FL164K	0X	MFB	Q1	0, 1, 3	FL164KAFQ1
		BHA	02	0, 3	FL164KAH02
			03		FL164KAH03
		BHB	02		FL164KBH02
			03		FL164KBH03

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13. Revision History

Document History Page

Document Title: S25FL116K/S25FL132K/S25FL164K, 16-Mbit (2 Mbyte)/32-Mbit (4 Mbyte)/64-Mbit (8 Mbyte), 3.0 V, SPI Flash Memory Document Number: 002-00497				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	ASPA	04/14/2014	Initial release Combined S25FL116K_00_06 and S25FL132K_164K_00_05 Global: Promoted data sheet from Preliminary to Full Production Added 125°C option
*A	–	ASPA	10/10/2014	Migration Notes: FL Generations Comparison table: corrected Sector Erase Time (typ.) for S25FL1-K AC Electrical Characteristics: AC Electrical Characteristics — -40°C to +85°C/105°C at 2.7V to 3.6V table: added tRCH and tRST Input / Output Timing: added Software Reset Input Timing figure Physical Interface: Corrected figure: 8-Contact WSON (5 mm x 6 mm) Package Security Register 0 — Serial Flash Discoverable Parameters (SFDP — JEDEC JESD216B): Updated section based on revised JEDEC JESD216B spec Commands: Added Command Set (Reset Commands) table Reset Commands: Added sections: Reset Commands, Software Reset Enable (66h), Software Reset (99h) Updated section: Continuous Read Mode Reset (FFh or FFFFh)
*B	–	ASPA	12/04/2014	Power-Up Timing: Power-Up Timing and Voltage Levels table: corrected TPUW Valid Combinations: Valid Combinations table: corrected FL116K Model Number and Package Marking
*C	4891479	BWHA	09/18/2015	Updated to Cypress template.
*D	5044503	BWHA	12/18/2015	Added “USON 4 mm × 4 mm” package related information in all instances across the document. Updated This product family has been retired and is not recommended for designs. For new and current designs, S25FL064L supersede the S25FL1-K family. These are the factory-recommended migration paths. Please refer to the S25FL-L Family datasheets for specifications and ordering information.: Updated Package Options. Updated Physical Interface: Updated Connection Diagrams: Updated SOIC 8: Updated Figure 27. Updated SOIC 16 — S25FL164K: Updated Figure 28. Updated WSON 8: Updated Figure 29. Updated FAB024 24-Ball BGA: Updated Figure 6.1. Updated FAC024 24-Ball BGA Package: Updated Figure 6.2. Updated Physical Diagrams: Added UNF008 — 8-Contact USON 4 mm x 4 mm. Updated Ordering Information: Added “Halogen-free” for “F” under “Package Materials”. Added Note “GT grade is Cypress’s quality and reliability rating to indicate products that are tested to meet <10 ppm and intended for high reliability applications such as automotive.” and referred the same note in “A” under “Temperature Range”.

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Document Title: S25FL116K/S25FL132K/S25FL164K, 16-Mbit (2 Mbyte)/32-Mbit (4 Mbyte)/64-Mbit (8 Mbyte), 3.0 V, SPI Flash Memory Document Number: 002-00497				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	5270099	BWHA	06/29/2016	Added Logic Block Diagram. Updated Electrical Characteristics: Added Thermal Resistance. Updated Data Integrity: Removed “Endurance”. Added Data Retention. Updated Ordering Information: Updated Valid Combinations — Automotive Grade / AEC-Q100: Updated Table : Added a column “Model Number”. Added a row under “FL164K” and added “MFB” and its corresponding details. Updated to new template.
*F	5645494	BWHA	02/28/2017	Updated Signal Descriptions: Updated Input / Output Summary: Update Table 1: Updated details in “Description” column corresponding to “DNU”. Updated Electrical Characteristics: Updated Operating Ranges: Updated Table 6: Removed Extended Temperature range related information. Updated AC Electrical Characteristics: Updated Table 10: Added “t_{CS}” parameter and its details. Updated Physical Interface: Updated Physical Diagrams: Updated SOA008 — 8-Lead Plastic Small Outline Package (150-mils Body Width) (Updated Package Drawing to Cypress format). Updated SOC008 — 8-Lead Plastic Small Outline Package (208-mils Body Width) (Updated Package Drawing to Cypress format). Updated SO3016 — 16-Lead Plastic Wide Outline Package (300-mils Body Width) (Updated Package Drawing to Cypress format). Updated WND008 — 8-Contact WSON 5 mm ´ 6 mm (Updated Package Drawing to Cypress format). Updated UNF008 — 8-Contact USON 4 mm x 4 mm (Updated Package Drawing to Cypress format). Updated FAB024 — 24-Ball Ball Grid Array (8 mm ´ 6 mm) Package (Updated Package Drawing to Cypress format). Updated FAC024 — 24-Ball Ball Grid Array (8 mm ´ 6 mm) Package (Updated Package Drawing to Cypress format). Updated Address Space Maps: Updated Device Identification: Updated Table 25: Added Note 41 and referred the same note in “ABh” in “Instruction” column. Added Note 42 and referred the same note in “90h” in “Instruction” column. Added Note 43 and referred the same note in “9Fh” in “Instruction” column.

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Document History Page (Continued)

Document Title: S25FL116K/S25FL132K/S25FL164K, 16-Mbit (2 Mbyte)/32-Mbit (4 Mbyte)/64-Mbit (8 Mbyte), 3.0 V, SPI Flash Memory Document Number: 002-00497				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F (cont.)	5645494	BWHA	02/28/2017	Updated Commands: Updated Table 29: Updated details in “BYTE 2”, “BYTE 3” and “BYTE 4” columns corresponding to “Manufacturer / Device ID” command. Update Data Integrity: Update Data Retention: Removed “Data Retention Time Security Registers nonvolatile register array” parameter and its details. Updated Ordering Information: Updated Valid Combinations — Automotive Grade / AEC-Q100: Updated description. Removed a row corresponding to “MFI” under “FL132K”. Removed rows corresponding to “MFI”, “MFV”, “NFI” and “NFV” under “FL164K”. Updated to new template.
*G	5709491	GNKK	04/25/2017	Updated the Cypress logo and copyright information.
*H	5742469	NFB	05/19/2017	Added “Not Recommended for New Design (NRND)” status.
*I	6228963	BWHA	07/04/2018	Updated Ordering Information section and added a note “Halogen free definition is in accordance with IEC 61249-2-21”

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