THE DATASHEET OF

RR2L4SDDTE25

FEATURES

- Single 5V to 21V application
- Wide Input Voltage Range from 1.0V to 21V with external Vcc
- Output Voltage Range: 0.5V to 0.86* Vin
- Enhanced Line/Load Regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start/Soft-Stop
- Enable input with Voltage Monitoring Capability
- Thermally Compensated Current Limit with robust hiccup mode over current protection
- Smart internal LDO to improve light load and full load efficiency
- External Synchronization with Smooth Clocking
- Enhanced Pre-Bias Start-Up
- Precision Reference Voltage (0.5V+/-0.5%) with margining capability
- Vp for Tracking Applications ((Source/Sink Capability +/-12A)
- Integrated MOSFET drivers and Bootstrap Diode
- Thermal Shut Down
- Programmable Power Good Output with tracking capability
- Monotonic Start-Up
- Operating temp: -40°C < Tj < 125°C
- Small Size: 5mm x 6mm PQFN
- Lead-free, Halogen-free and RoHS Compliant

DESCRIPTION

The IR3894 SupIRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3894 a space-efficient solution, providing accurate power delivery.

IR3894 is a versatile regulator which offers programmable switching frequency and the fixed internal current limit

The switching frequency is programmable from 300 kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, thermally compensated current limit over voltage protection and thermal shutdown to give required system level security in the event of fault conditions.

APPLICATIONS

- Netcom Applications
- Embedded Telecom Systems
- Server Applications
- Storage Applications
- Distributed Point of Load Power Architectures

BASIC APPLICATION

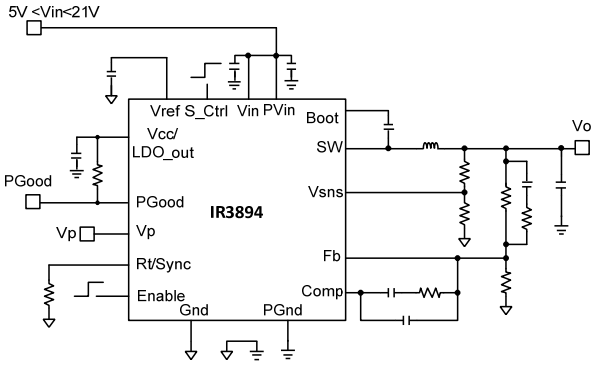


Figure 1: IR3894 Basic Application Circuit

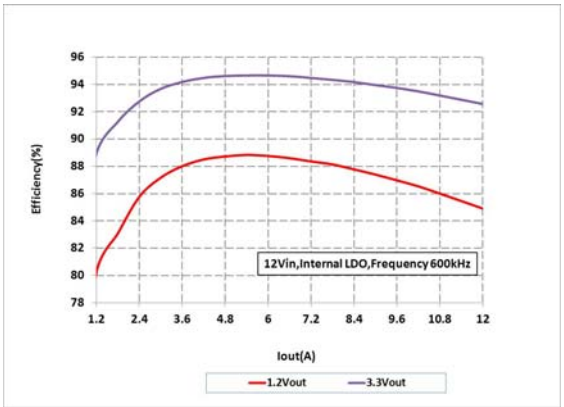
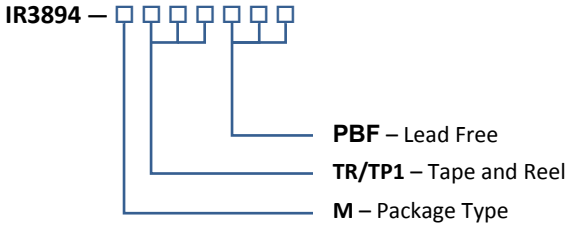


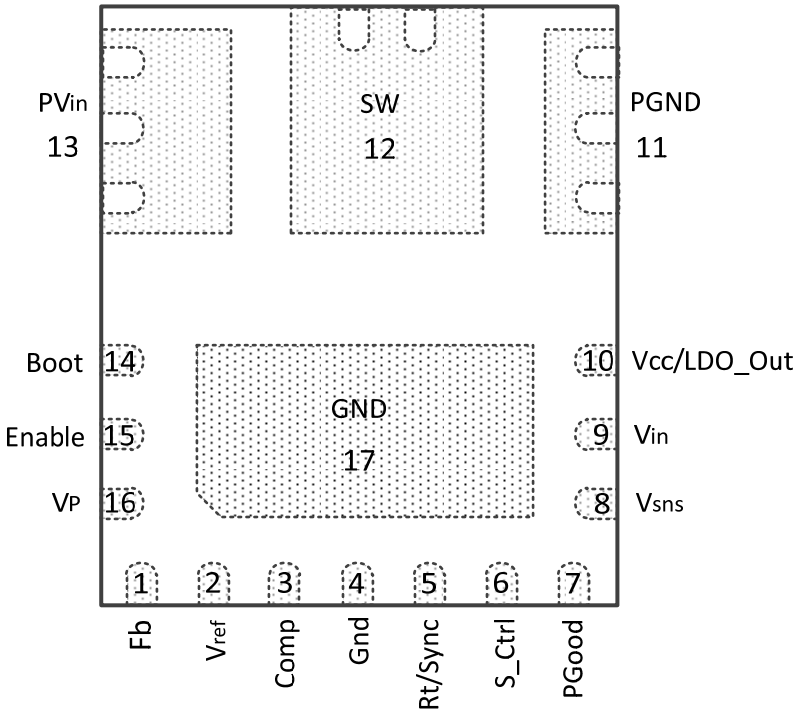
Figure 2: IR3894 Efficiency

ORDERING INFORMATION

Package	Tape & Reel Qty	Part Number
M	750	**IR3894MTR1PBF**
M	4000	**IR3894MTRPBF**



PIN DIAGRAM
5m x 6mm POWER QFN
(TOP VIEW)



$$\theta_{JA} = 30°C/W$$
$$\theta_{J\text{-}PCB} = 2°C/W$$

BLOCK DIAGRAM

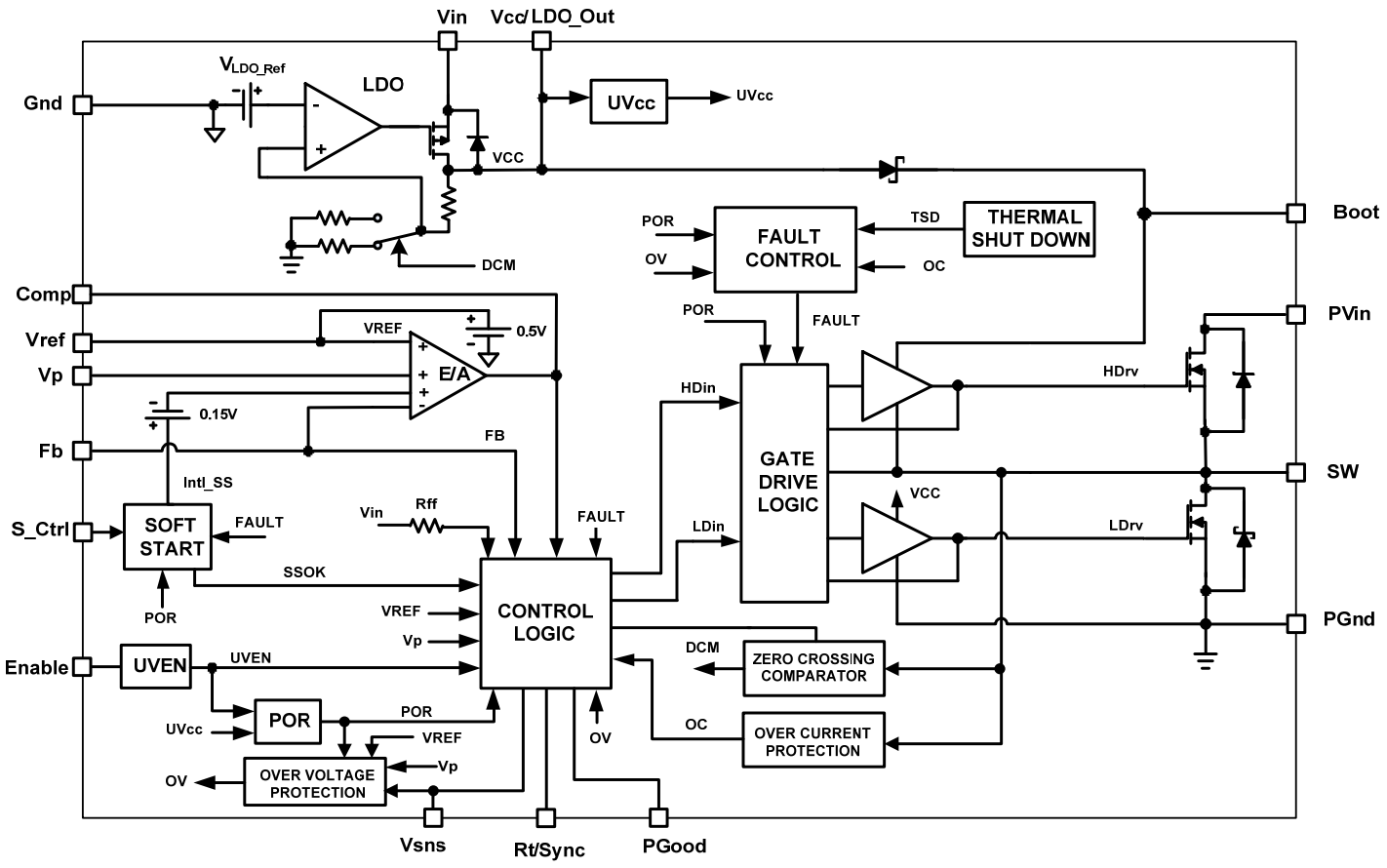


Figure 3: IR3894 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Vref	Internal reference voltage , it can be used for margining operation also. In normal mode and sequencing mode, a 100pF ceramic capacitor is recommended between this pin and Gnd. In tracking mode operation, Vref should be tied to Gnd.
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb to provide loop compensation.
4	Gnd	Signal ground for internal reference and control circuitry.
5	Rt/Sync	Multi-function pin to set switching frequency. Use an external resistor from this pin to Gnd to set the free-running switching frequency. An external clock signal to connect to this pin through a diode, the device's switching frequency is synchronized with the external clock.
6	S_Ctrl	Soft start/stop control. A high logic input enables the device to go into the internal soft start; a low logic input enables the output soft discharged. Pull this pin to Vcc if this function is not used.
7	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to the voltage lower than or equal to the Vcc.
8	Vsns	Sense pin for over-voltage protection and PGood. It is optional to tie this pin to Fb pin directly instead of using a resistor divider from Vout.
9	Vin	Input voltage for Internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If external supply is connected to Vcc/LDO_out pin, this pin should be shorted to Vcc/LDO_Out pin.
10	Vcc/LDO_Out	Input Bias Voltage, output of internal LDO. Place a minimum 2.2µF cap from this pin to PGnd.
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	Switch node. This pin is connected to the output inductor.
13	PVin	Input voltage for power stage.
14	Boot	Supply voltage for high side driver, a 100nF capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn on and off the device, if this pin is connected to PVin pin through a resistor divider, input voltage UVLO can be implemented.
16	Vp	Input to error amplifier for tracking purposes. In the normal operation, it is left floating and no external capacitor is required. In the sequencing or the tracking mode operation, an external signal can be applied as the reference.
17	Gnd	Signal ground for internal reference and control circuitry.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
Vcc/LDO_Out	-0.3V to 8V (Note 2)
Boot	-0.3V to 33V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
Boot to SW	-0.3V to Vcc + 0.3V (Note 1)
S_Ctrl, PGood	-0.3V to Vcc + 0.3V (Note 1)
Other Input/Output Pins	-0.3V to +3.9V
PGnd to Gnd	-0.3V to +0.3V
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C (Note 2)
ESD Classification (HBM JESD22-A114)	2kV
Moisture Sensitivity Level	JEDEC Level 2@260°C

Note 1: Must not exceed 8V

Note 2: Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

	SYMBOL	MIN	MAX	UNITS
Input Voltage Range*	PV_{IN}	1.0	21	V
Input Voltage Range**	V_{IN}	5	21	
Supply Voltage Range***	V_{CC}	4.5	7.5	
Supply Voltage Range	Boot to SW	4.5	7.5	
Output Voltage Range	V_O	0.5	0.86xVin	
Output Current Range	I_O	0	±12	A
Switching Frequency	F_S	300	1500	kHz
Operating Junction Temperature	T_J	-40	125	°C

*Maximum SW node voltage should not exceed 25V.

**For internally biased single rail operation. When Vin drops below 6.8V, the internal LDO enters dropout. Please refer to Smart LDO section and Over Current Protection for detailed application information.

*** Vcc/LDO_out can be connected to an external regulated supply. If so, the Vin input should be connected to Vcc/LDO_out pin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over, 6.8V < Vin = PVin < 21V, Vref = 0.5V in 0°C < T_J < 125°C. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Stage						
Power Losses	P_{LOSS}	Vin = 12V, V_O = 1.2V, I_O = 12A, Fs = 600kHz, L = 0.51uH, Vcc = 6.4V (Internal LDO),Note 4		2.1		W
Top Switch	$R_{ds(on)\_Top}$	VBoot - Vsw= 6.4V,I_O = 12A,T_j=25°C		13.2	17.2	mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	Vcc = 6.4V, I_O = 12A		7.2	9.4	
Bootstrap Diode Forward Voltage		I(Boot) = 15mA	200	300	500	mV
SW Leakage Current	I_{SW}	SW = 0V, Enable = 0V			1	µA
		SW = 0V, Enable = high, Vp = 0V				
Dead Band Time	T_{db}	Note 4		20		ns
Supply Current						
VIN Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching			100	µA
VIN Supply Current (dynamic)	$I_{in(Dyn)}$	EN = High, Fs = 600kHz, Vin = PVin = 21V		14	18	mA
VCC LDO Output						
Output Voltage	V_{cc}	Vin(min) = 6.8V, Icc = 0-50mA, Cload = 2.2uF, DCM = 0	6.0	6.4	6.7	V
		Vin(min) = 6.8V, Icc = 0-50mA, Cload = 2.2uF, DCM = 1	4.0	4.4	4.85	
VCC Dropout	V_{cc_drop}	Icc=50mA,Cload=2.2uF			0.8	V
Short Circuit Current	Ishort			70		mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Zero-crossing Comparator Delay	Tdly_zc	Note 4		256/Fs		s
Zero-crossing Comparator Offset	Vos_zc	Note 4	-4	0	4	mV
Oscillator						
Rt Voltage	Vrt			1.0		V
Frequency Range	F_s	Rt = 80.6K	270	300	330	kHz
		Rt = 39.2K	540	600	660	
		Rt = 15.0K	1350	1500	1650	
Ramp Amplitude	Vramp	Vin = 6.8V, Vin slew rate max = 1V/µs, Note 4		1.02		Vp-p
		Vin = 12V, Vin slew rate max = 1V/µs, Note 4		1.80		
		Vin = 21V, Vin slew rate max = 1V/µs, Note 4		3.15		
		Vcc=Vin=5V, For external Vcc operation,Note 4		0.75		
Ramp Offset	Ramp(os)	Note 4		0.16		V
Min Pulse Width	Tmin(ctrl)	Note 4			60	ns
Max Duty Cycle	Dmax	Fs = 300kHz, PVin = Vin = 12V	86			%
Fixed Off Time	Toff	Note 4		200	250	ns
Sync Frequency Range	Fsync		270		1650	kHz
Sync Pulse Duration	Tsync		100	200		ns
Sync Level Threshold	High		3			V
	Low				0.6	
Error Amplifier						
Input Offset Voltage	Vos_Vref	VFb – Vref, Vref = 0.5V	-1.5		+1.5	%
	Vos_Vp	VFb – Vp, Vp = 0.5V,Vref=0	-1.5		+1.5	
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVp(E/A)		0		+4	
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 4	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 4	20	30	40	MHz
DC Gain	Gain	Note 4	100	110	120	dB
Maximum output Voltage	Vmax(E/A)		1.7	2.0	2.3	V
Minimum output Voltage	Vmin(E/A)				100	mV
Common Mode input Voltage			0		1.2	V
Reference Voltage						
Feedback Voltage	Vfb	Vref and Vp pin floating		0.5		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy		0°C < Tj < 70°C	-0.5		+0.5	%
		-40°C < Tj < 125°C, Note 3	-1.0		+1.0	
Vref Margining Voltage	Vref_marg		0.4		1.2	V
Sink Current	Isink_Vref	Vref = 0.6V	12.7	16.0	19.3	µA
Source Current	Isrc_Vref	Vref = 0.4V	12.7	16.0	19.3	
Vref Comparator Threshold	Vref_disable	Vref pin connected externally			0.15	V
	Vref_enable		0.4			
Soft Start/Stop						
Soft Start Ramp Rate	Ramp(SS_start)		0.16	0.2	0.24	mV/µs
Soft Start Ramp Rate	Ramp(SS_stop)		-0.24	-0.2	-0.16	
S_Ctrl Threshold	High		2.4			V
	Low				0.6	
Power Good						
PGood Turn on Threshold	VPG(on)	Vsns Rising, 0.4V < Vref < 1.2V	85	90	95	% Vref
		Vsns Rising, Vref < 0.1V	85	90	95	% Vp
PGood Lower Turn off Threshold	VPG(lower)	Vsns Falling, 0.4V < Vref < 1.2V	80	85	90	% Vref
		Vsns Falling, Vref < 0.1V	80	85	90	% Vp
PGood Turn on Delay	VPG(on)_Dly	Vsns Rising,see VPG(on)		1.28		ms
PGood Upper Turn off Threshold	VPG(upper)	Vsns Rising, 0.4V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp
PGood Comparator Delay	VPG(comp)_ Dly	Vsns < VPG(lower) or Vsns > VPG(upper)	1	2	3.5	µs
PGood Voltage Low	PG(voltage)	IPgood = -5mA			0.5	V
Tracker Comparator Upper Threshold	VPG(tracker_ upper)	Vp Rising, Vref < 0.1V		0.4		V
Tracker Comparator Lower Threshold	VPG(tracker_ lower)	Vp Falling, Vref < 0.1V		0.3		
Tracker Comparator Delay	Tdelay(tracker)	Vp Rising, Vref < 0.1V,see VPG(tracker_upper)		1.28		ms
Under-Voltage Lockout						
Vcc-Start Threshold	V_{CC}_UVLO_	Vcc Rising Trip Level	4.0	4.2	4.4	V
Vcc-Stop Threshold	V_{CC}_UVLO_	Vcc Falling Trip Level	3.7	3.9	4.1	
Enable-Start-Threshold	Enable_UVLO_	Supply ramping up	1.14	1.2	1.26	V
Enable-Stop-Threshold	Enable_UVLO_	Supply ramping down	0.95	1	1.05	
Enable Leakage Current	Ien	Enable = 3.3V			1	µA
Over-Voltage Protection						
OVP Trip Threshold	OVP_Vth	Vsns Rising, 0.45V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp

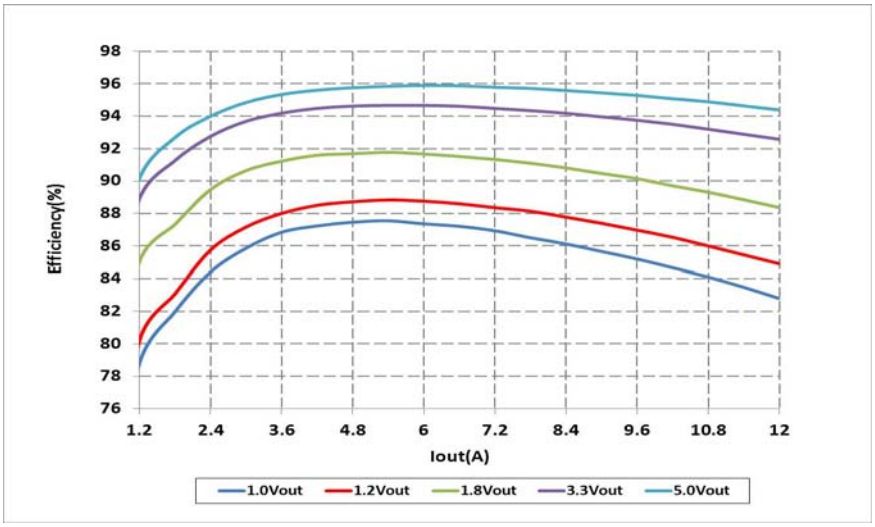
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OVP Comparator Delay	OVP_Tdly		1	2	3.5	µs
Over-Current Protection						
Current Limit	I_{LIMIT}	Tj = 25°C, Vcc = 6.4V	13.8	15.6	18.5	A
Hiccup Blanking Time	Tblk_Hiccup			20.48		ms
Over-Temperature Protection						
Thermal Shutdown Threshold	Ttsd	Note 4		145		°C
Hysteresis	Ttsd_hys	Note 4		20		

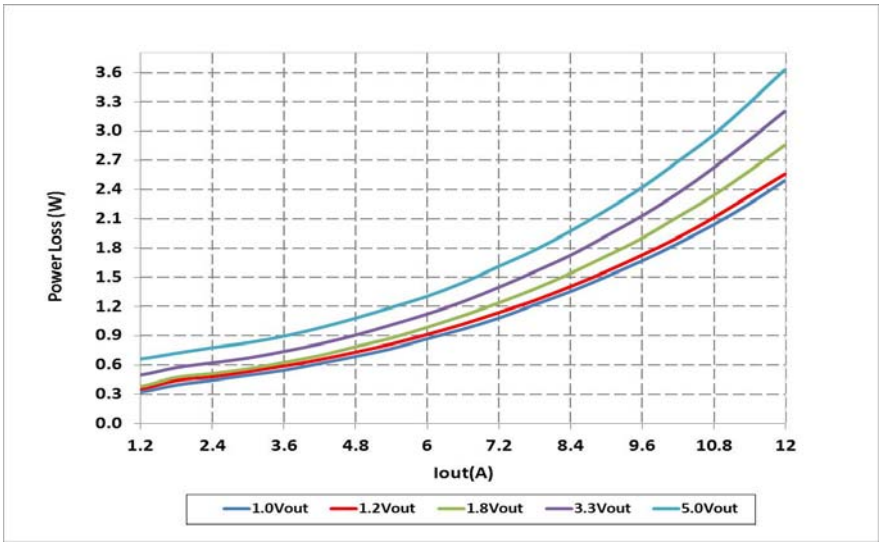
Note 3: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.
Note 4: Guaranteed by design but not tested in production.

TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vcc = Internal LDO (4.4V/6.4V), Io = 0A-12A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3898, the inductor losses and the losses of the input and output capacitors. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
1	0.51	59PR9876N (Vitec)	0.29
1.2	0.51	59PR9876N (Vitec)	0.29
1.8	0.72	744325072(Wurth Elektronik)	1.3
3.3	1.2	744325120(Wurth Elektronik)	1.8
5	1.2	744325120(Wurth Elektronik)	1.8



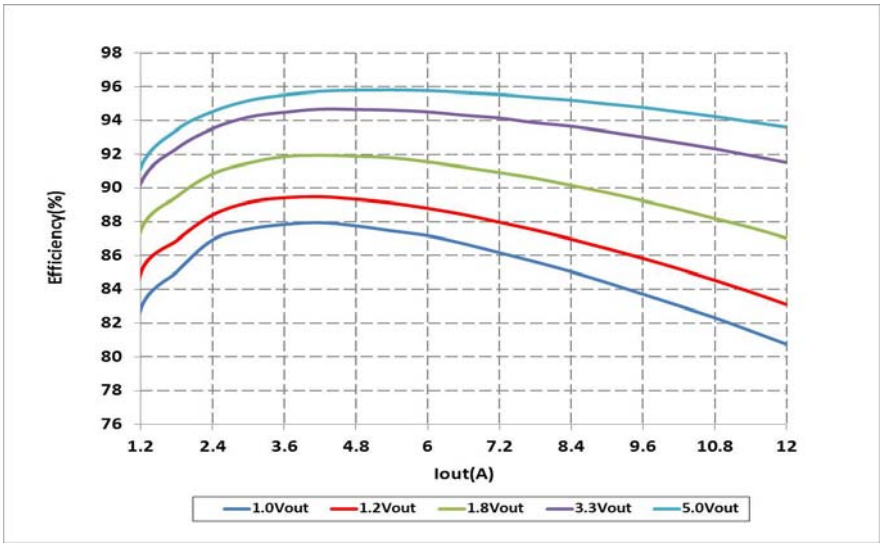


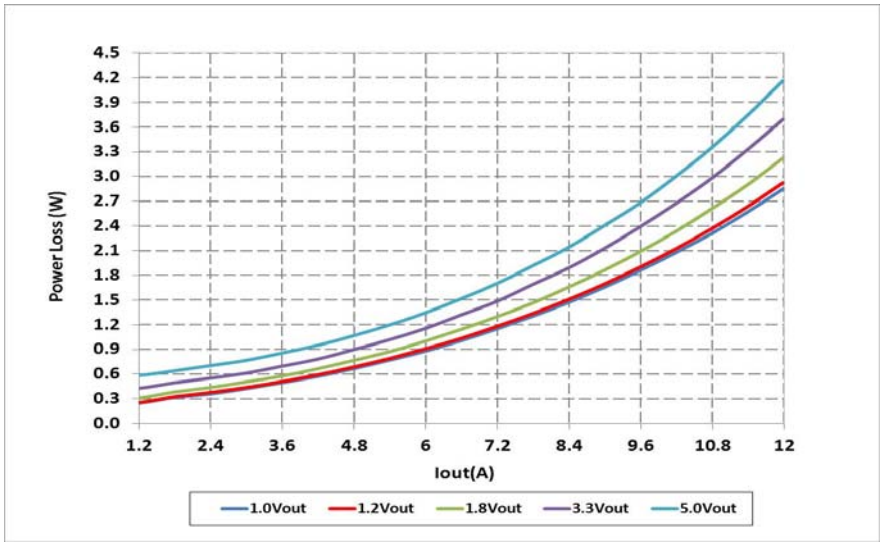
TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vcc = External 5V, Io = 0A-12A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3898, the inductor losses and the losses of the input and output capacitors.

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
1	0.51	59PR9876N (Vitec)	0.29
1.2	0.51	59PR9876N (Vitec)	0.29
1.8	0.72	744325072(Wurth Elektronik)	1.3
3.3	1.2	744325120(Wurth Elektronik)	1.8
5	1.2	744325120(Wurth Elektronik)	1.8



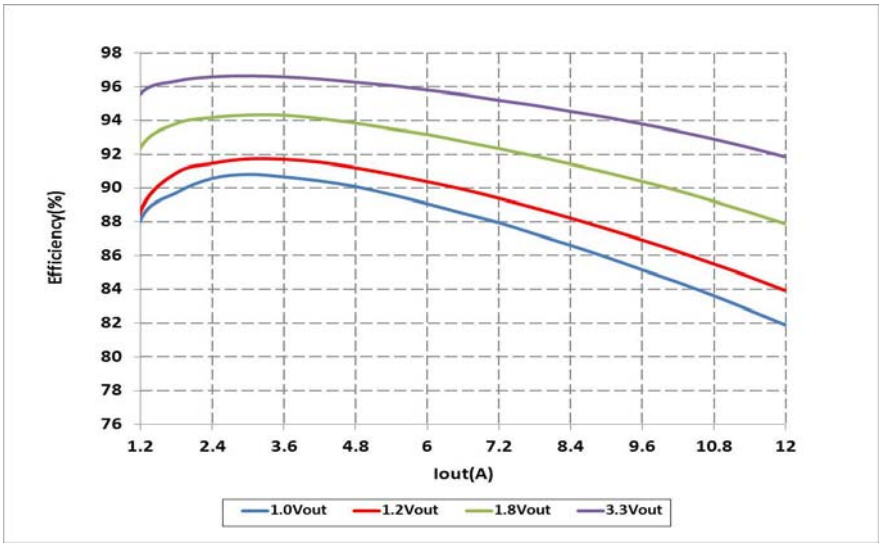


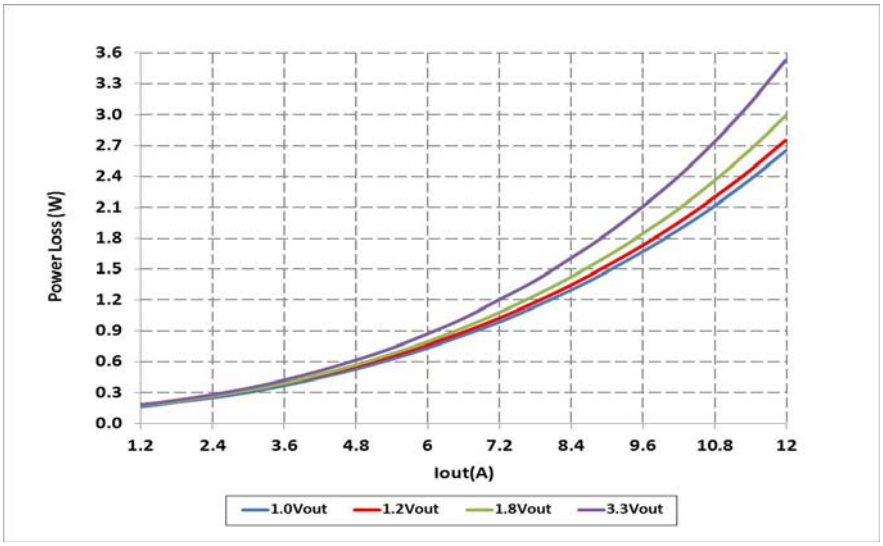
TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 5.0V, Vcc = 5.0V, Io = 0A-12A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3898, the inductor losses and the losses of the input and output capacitors.

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
1	0.4	59PR9875N (Vitec)	0.29
1.2	0.4	59PR9875N (Vitec)	0.29
1.8	0.51	59PR9876N (Vitec)	0.29
3.3	0.51	59PR9876N (Vitec)	0.29

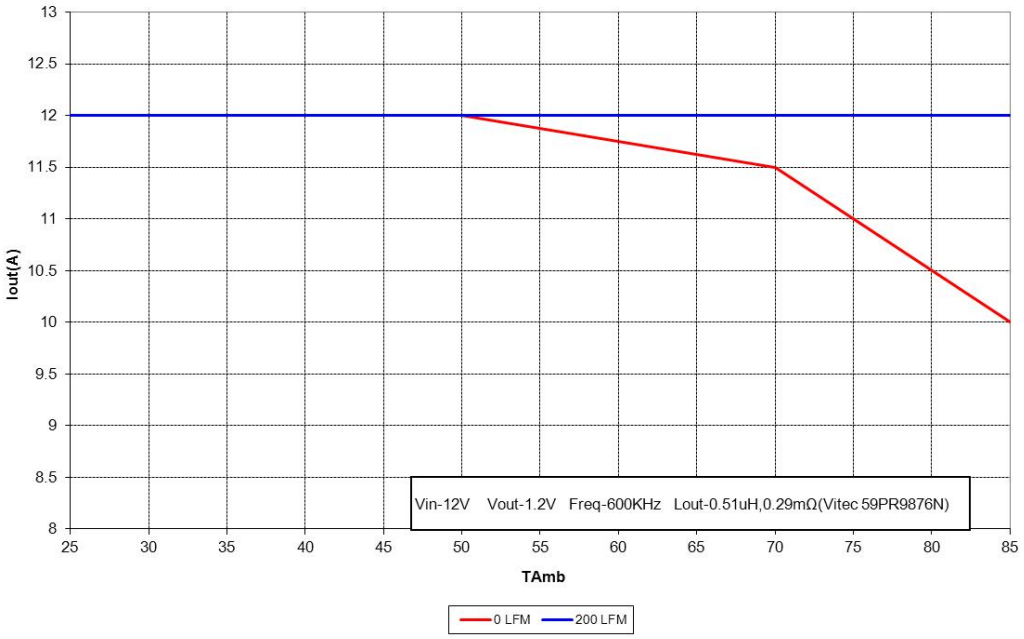




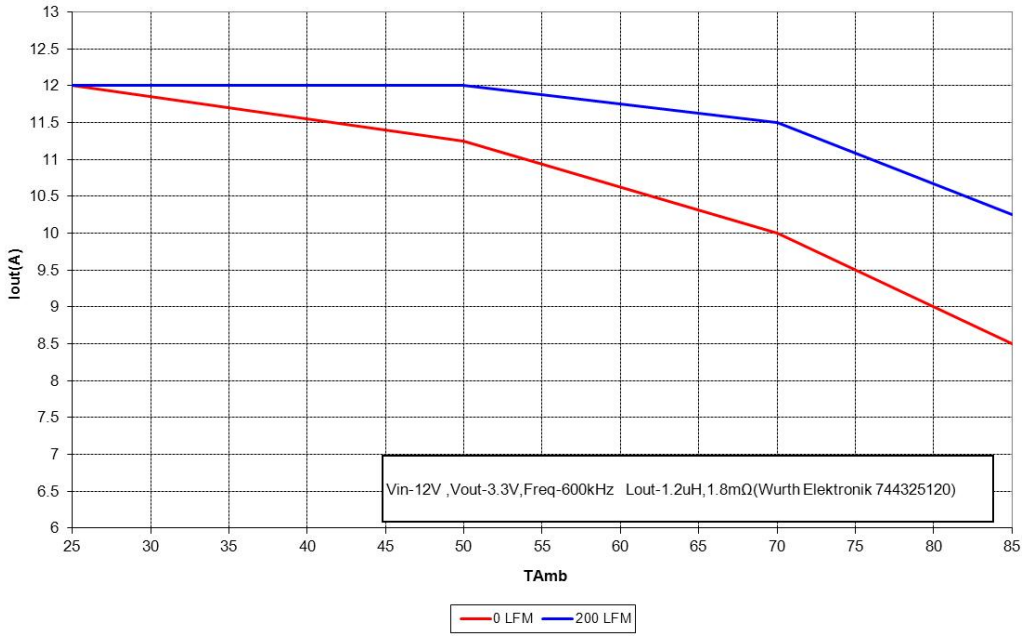
THERMAL DERATING CURVES

Measurement done on Evaluation board of IRDC3894.PCB is 4 layer board with 2 oz Copper, FR4 material, size 2.23"x2"

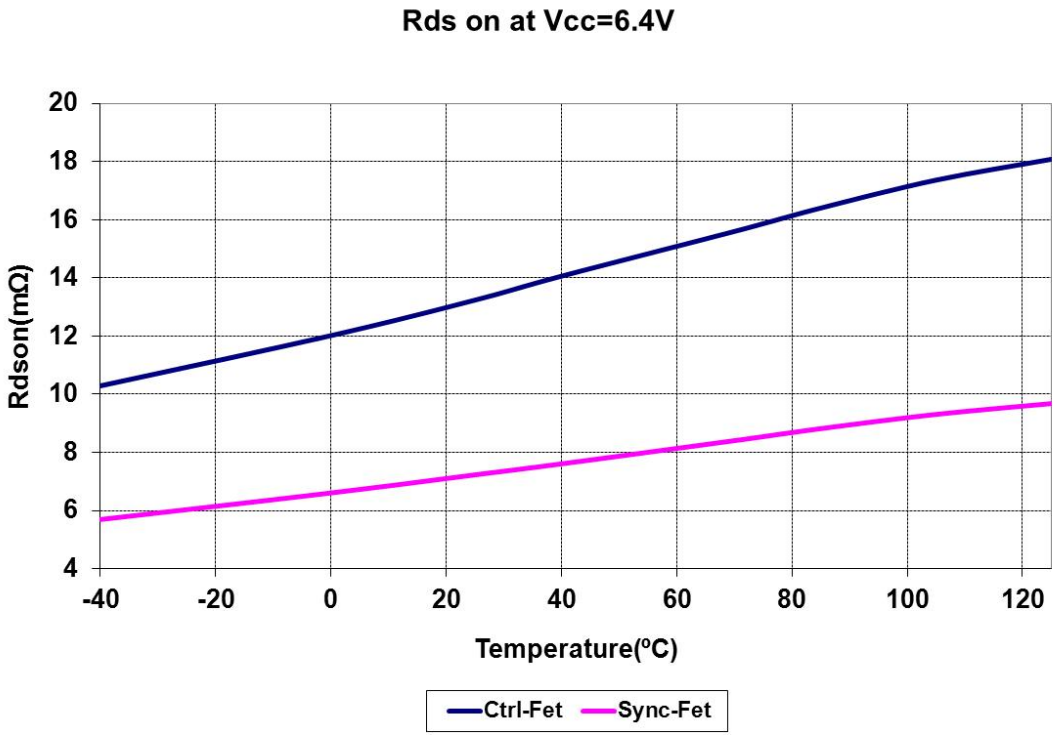
PVin = 12V, Vout=1.2V, Vcc = Internal LDO (6.4V), Fs = 600kHz



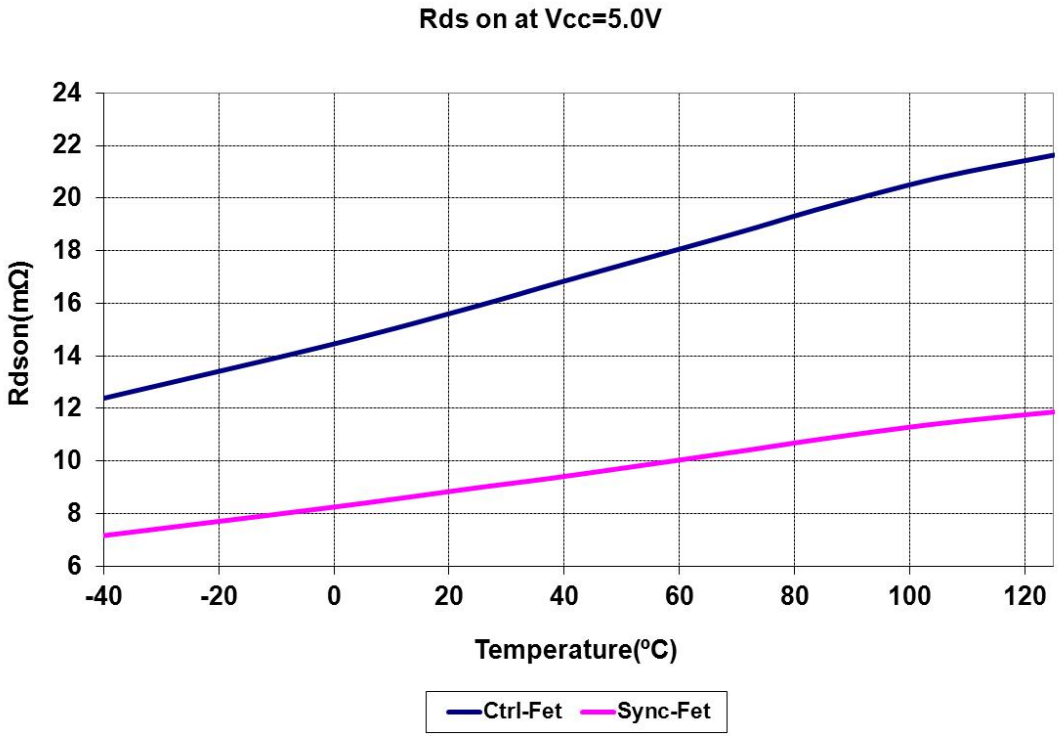
PVin = 12V, Vout=3.3V, Vcc = Internal LDO (6.4V), Fs = 600kHz



RDSON OF MOSFETS OVER TEMPERATURE AT V_{CC}=6.4V

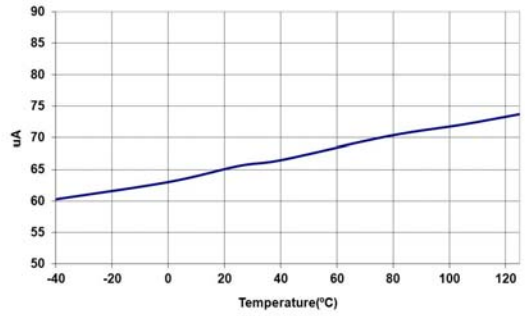


RDSON OF MOSFETS OVER TEMPERATURE AT V_{CC}=5.0V

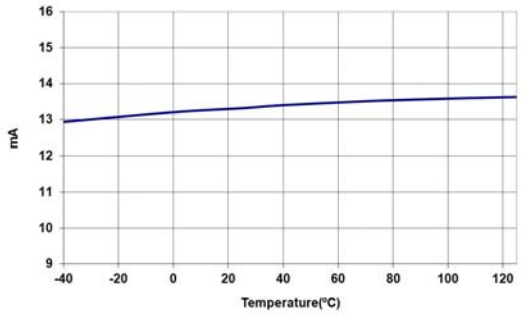


TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

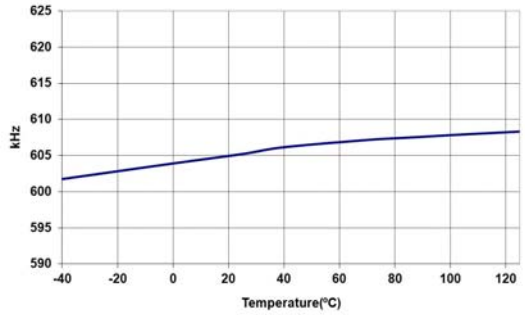
Iin (Stand by)



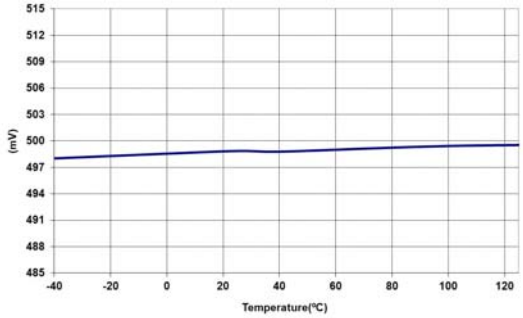
Iin (Dyn)



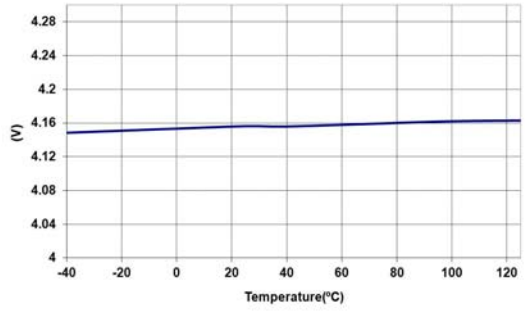
Frequency



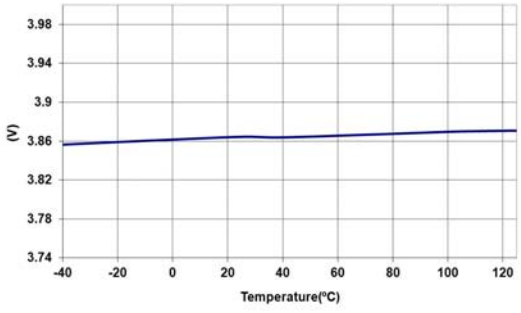
Vfb



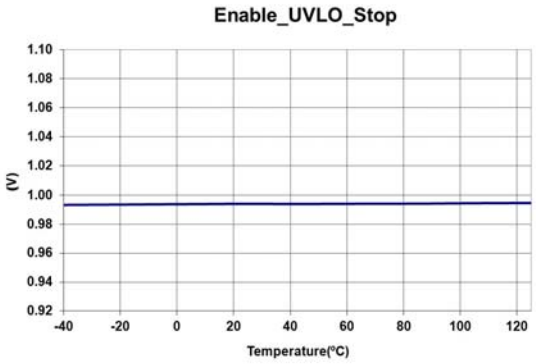
Vcc_UVLO_Start

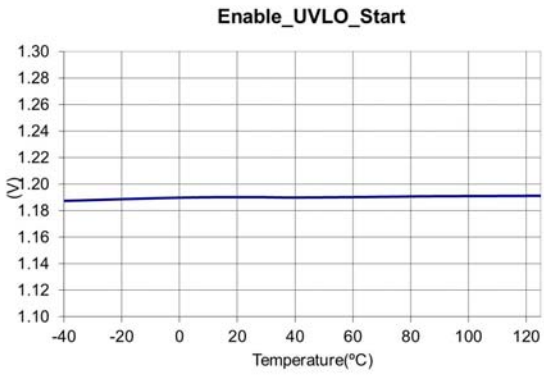


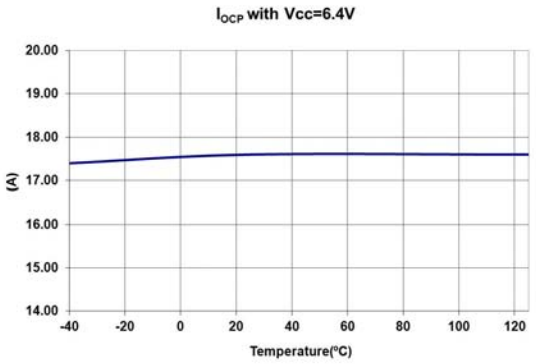
Vcc_UVLO_Stop



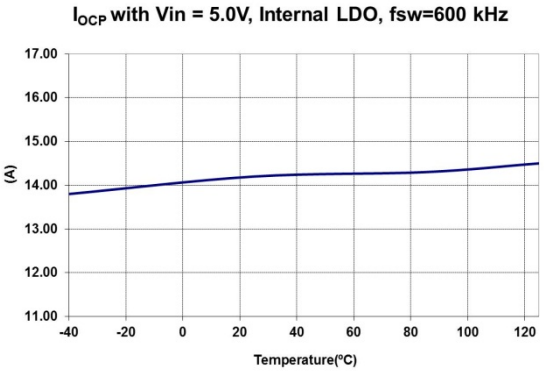
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)



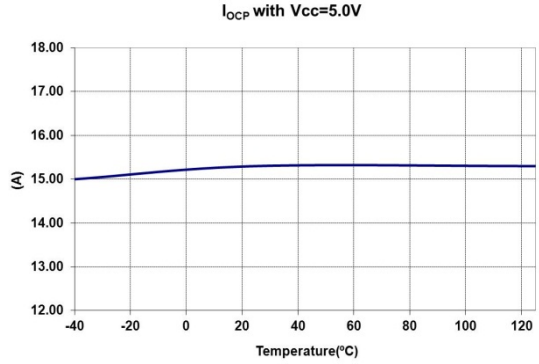




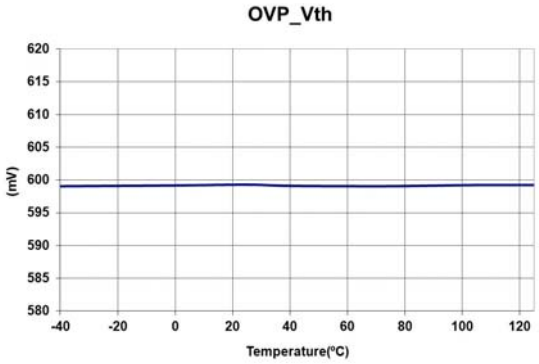
Internal LDO in regulation



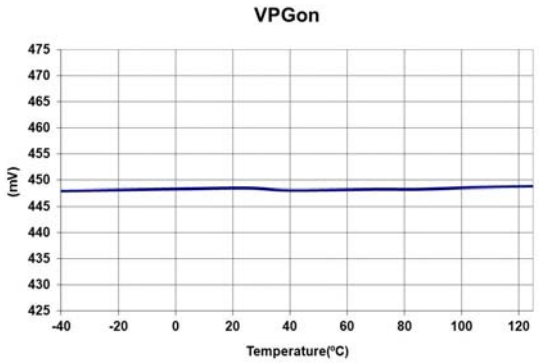
Internal LDO in dropout mode

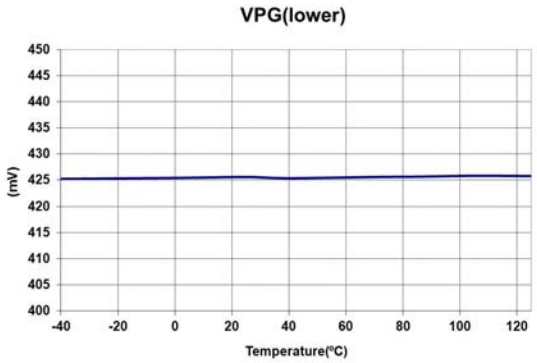


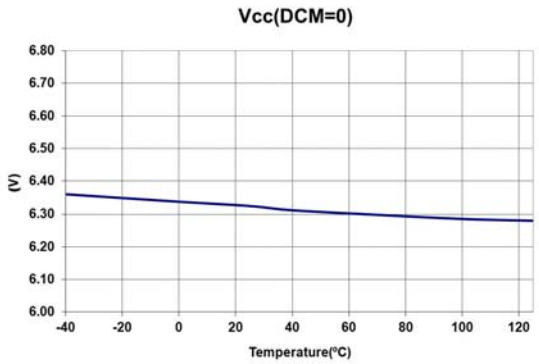
With an External 5V Vcc Voltage

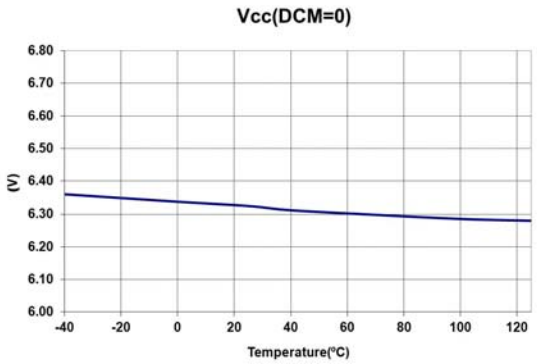


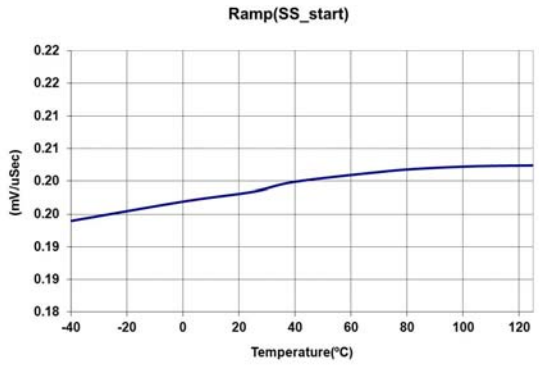
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)











THEORY OF OPERATION

DESCRIPTION

The IR3894 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300 KHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3894 provides precisely regulated output voltage programmed via two external resistors from 0.5V to 0.86*Vin.

The IR3894 operates with an internal bias supply (LDO) which is connected to the Vcc/LDO_out pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-to-peak inductor current, a lower bias voltage, 4.4V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.4V, is used. This feature helps the converter to reduce power losses. For internal biased single-rail operation, if the input voltage drops below 6.8V, the internal LDO starts to enter dropout mode.

The IC can also be operated with an external supply from 4.5 to 7.5V, allowing an extended operating input voltage (PVin) range from 1.0V to 21V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to Vcc/LDO_out pin and the Vin pin should be shorted to Vcc/LDO_out pin.

The device utilizes the on-resistance of the low side MOSFET (sync FET) for the over current protection. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3894 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuit monitors the voltage of Vcc/Ldo pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc/LDO_Out and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

ENABLE

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3894 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3894 does not turn on until the bus voltage reaches the desired level (Fig. 4). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3894 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3894, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3894 to be disabled at least until PVIN exceeds the desired output voltage level.

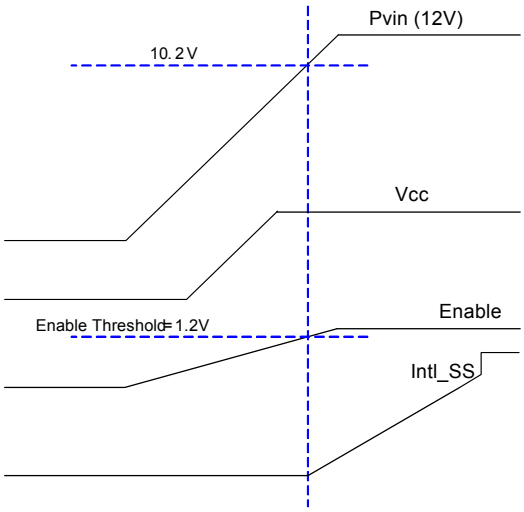


Figure 4: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

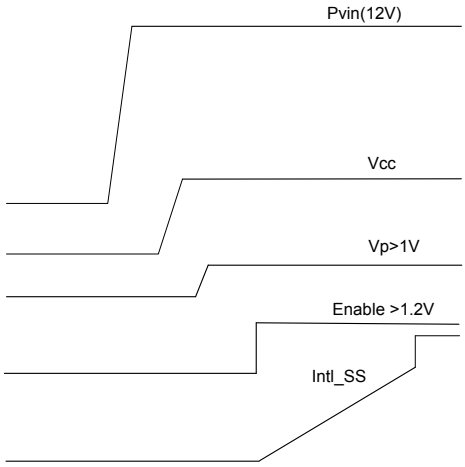


Figure 5a: Recommended startup for Normal operation

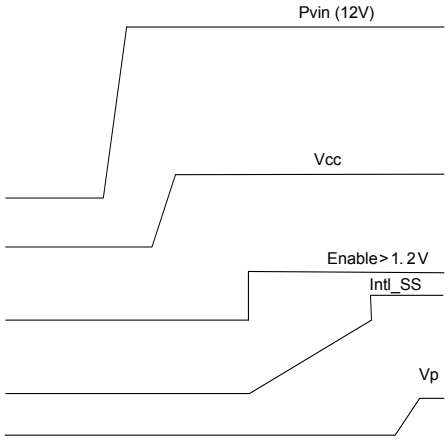


Figure 5b: Recommended startup for sequencing operation (ratiometric or simultaneous)

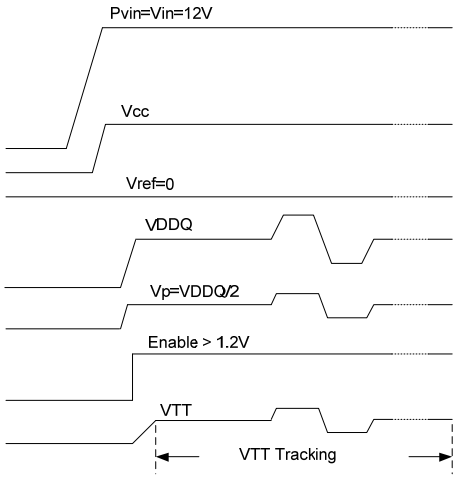


Figure 5c: Recommended startup for memory tracking operation (VTT-DDR4)

Figure 5a shows the recommended start-up sequence for the normal (non-tracking, non-sequencing) operation of IR3894, when Enable is used as a logic input. Figure 5b shows the recommended startup sequence for sequenced operation of IR3894 with Enable used as logic input. Figure 5c shows the recommended startup sequence for tracking operation of IR3894 with Enable used as logic input.

In normal and sequencing mode operation, Vref is left floating. A 100pF ceramic capacitor is recommended between this pin and Gnd. In tracking mode operation, Vref should be tied to Gnd.

It is recommended to apply the Enable signal after the VCC voltage has been established. If the Enable signal is present before VCC, a 50kΩ resistor can be used in series with the Enable pin to limit the current flowing into the Enable pin.

PRE-BIAS STARTUP

IR3894 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 6a shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. Figure 6b shows the series of 16x8 startup pulses.

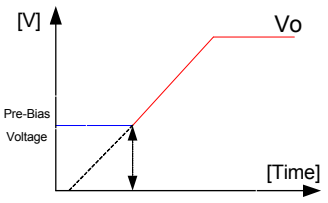


Figure 6a: Pre-Bias startup

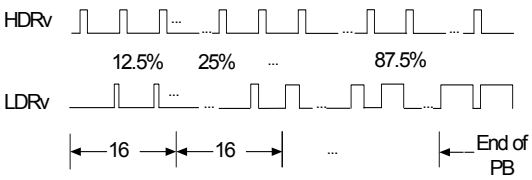


Figure 6b: Pre-Bias startup pulses

SOFT-START

IR3894 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.2mV/µs from 0V to 1.5V. Figure 7 shows the waveforms during soft start (also refer to Fig. 20). The normal Vout start up time is fixed, and is equal to:

$$T_{start} = \frac{(0.65V\text{-}0.15V)}{0.2mV/\mu s} = 2.5ms \qquad (1)$$

During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

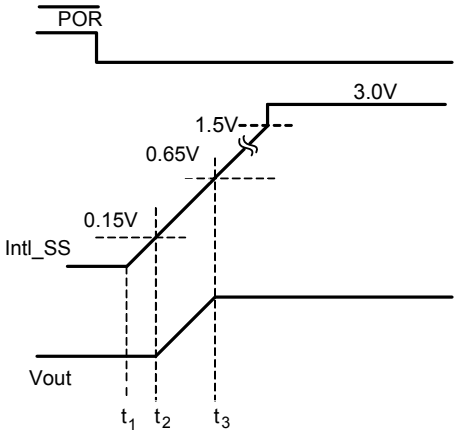


Figure 7: Theoretical operation waveforms during soft-start (non tracking / non sequencing)

OPERATING FREQUENCY

The switching frequency can be programmed between 300 kHz – 1500 kHz by connecting an external resistor from R_t pin to Gnd. Table 1 tabulates the oscillator frequency versus R_t.

SHUTDOWN

IR3894 can be shutdown by pulling the Enable pin below its 1.0V threshold. This will tri-state both the high side and the low side driver.

TABLE 1: SWITCHING FREQUENCY (FS) VS. EXTERNAL RESISTOR (R_T)

Rt (KΩ)	Freq (kHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.6	1300
16.2	1400
15	1500

OVER CURRENT PROTECTION

The over current (OC) protection is performed by sensing current through the $R_{DS(on)}$ of the Synchronous Mosfet. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The current limit is pre-set internally and is compensated according to the IC temperature. So at different ambient temperature, the over-current trip threshold remains almost constant.

Note that the over current limit is a function of the Vcc voltage. Refer to the typical performance curves of the OCP current limit with the internal LDO and the external Vcc voltage. Detailed operation of OCP is explained as follows.

Over Current Protection circuit senses the inductor current flowing through the Synchronous Mosfet closer to the valley point. OCP circuit samples this current for 40nsec typically after the rising edge of the PWM set pulse which has a width of 12.5% of the switching period. The PWM pulse starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise are lower and helps to prevent false tripping due to noise and transient. An OC condition is detected if the load current exceeds the threshold, the converter enters into hiccup mode. PGood will go low and the internal soft start signal will be pulled low. The converter goes into hiccup mode with a 20.48ms (typ.) delay as shown in Figure 8. The convertor stays in this mode until the over load or short circuit is removed. The actual DC output current limit point will be greater than the valley point by an amount equal to approximate y

half of peak to peak inductor ripple current. The current limit point will be a function of the inductor value, input ,output voltage and the frequency of operation.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta I}{2} \quad (2)$$

I_{OCP}= DC current limit hiccup point
I_{LIMIT}= Current limit Valley Point
ΔI=Inductor ripple current

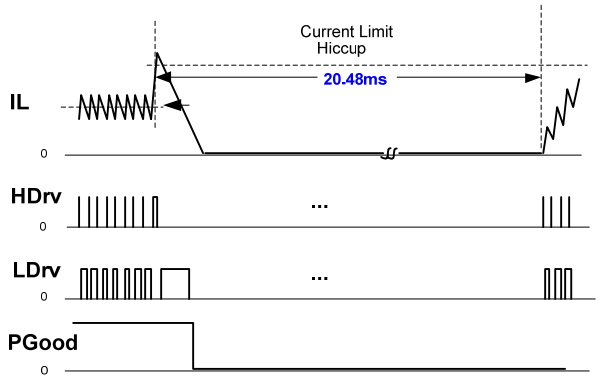


Figure 8: Timing Diagram for Current Limit Hiccup

THERMAL SHUTDOWN

Temperature sensing is provided inside IR3894. The trip threshold is typically set to 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

EXTERNAL SYNCHRONIZATION

IR3894 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to Gnd is required to set the free-running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. On the contrary, when the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running gradually. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin, as shown in Figure 9a. Figure 9b shows the timing diagram of these transitions.

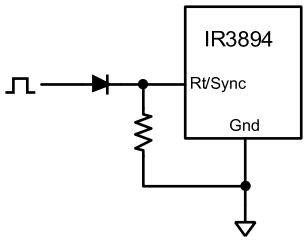


Figure 9a: Configuration of External Synchronization

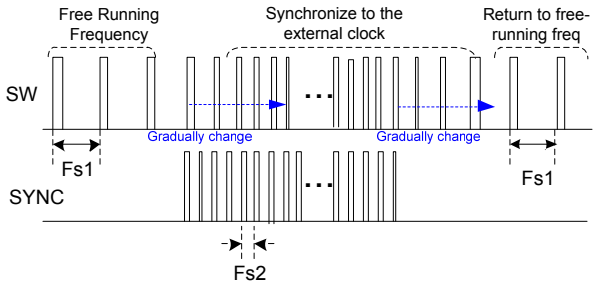


Figure 9b: Timing Diagram for Synchronization to the external clock (Fs1>Fs2 or Fs1<Fs2)

An internal circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Even though the frequency of the external synchronization clock can vary in a wide range, the PLL circuit will make sure that the ramp amplitude is kept constant, requiring no adjustment of the loop compensation. Vin variation also affects the ramp amplitude, which will be discussed separately in Feed-Forward section.

Feed-Forward

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when Vin varies in a large range. In IR3894, F.F. function is enabled when Vin pin is connected to PVin pin. In this case, the internal low dropout (LDO) regulator is used. The PWM ramp amplitude (Vramp) is proportionally changed with Vin to maintain Vin/Vramp almost constant throughout Vin variation range (as shown in Fig. 10). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast Vin change. The maximum Vin slew rate is within 1V/µs.

If an external bias voltage is used as Vcc, Vin pin should be connected to Vcc/LDO_out pin instead of PVin pin. Then the F.F. function is disabled. A re-calculation of control loop parameters is needed for re-compensation.

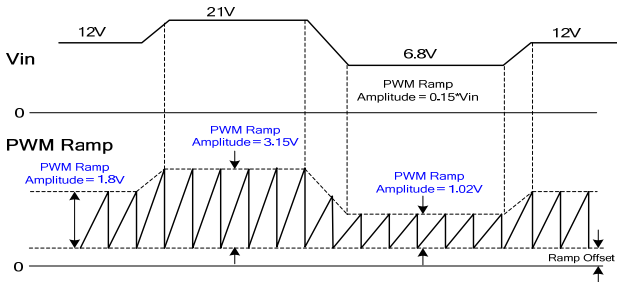


Figure 10: Timing Diagram for Feed-Forward (F.F.) Function

SMART LOW DROPOUT REGULATOR (LDO)

IR3894 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers. In order to improve overall efficiency over the whole load range, LDO voltage is set to 6.4V (typical.) at mid- or heavy load condition to reduce Rds(on) and thus MOSFET conduction loss; and it is reduced to 4.4 (typical.) at light load condition to reduce gate drive loss.

The smart LDO can select its output voltage according to the load condition by sensing switch node (SW) voltage. At light load condition when part of the inductor current flows in the reverse direction (DCM=1), $V_{SW} > 0$ on LDrv falling edge in a switching cycle. If this case happens for consecutive 256 switching cycles, the smart LDO reduces its output to 4.4V. If in any one of the 256 cycles, Vsw < 0 on LDrv falling edge, the counter is reset and LDO voltage doesn't change. On the other hand, if Vsw < 0 on LDrv falling edge (DCM=0), LDO output is increased to 6.4V. A hysteresis band is added to Vsw comparison to avoid chattering. Figure 11a shows the timing diagram. Whenever device turns on, LDO always starts with 6.4V, and then goes to 4.4V/6.4V depending upon the load condition. For internally biased single rail operation, Vin pin should be connected to PVin pin, as shown in Figure 11b. If external bias voltage is used, Vin pin should be connected to Vcc/LDO_Out pin, as shown in Figure 11c.

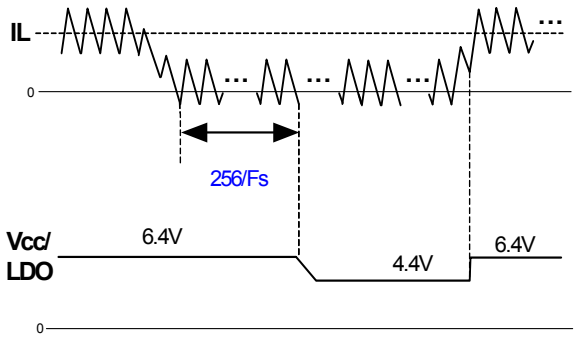


Figure 11a: Time Diagram for SmartLDO

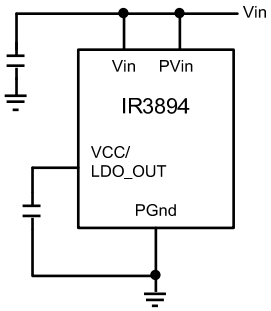


Figure 11b: Internally Biased Single Rail Operation

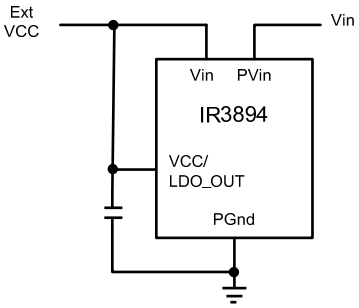


Figure 11c: Use External Bias Voltage

When the Vin voltage is below 6.8V, the internal LDO enters the dropout mode at medium and heavy load. The dropout voltage increases with the switching frequency. Figure 11d shows the LDO voltage for 600 kHz and 1500 kHz switching frequency respectively.

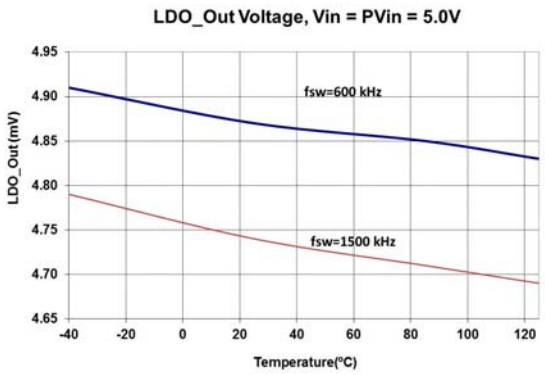


Figure 11d: LDO dropout Voltage

OUTPUT VOLTAGE TRACKING AND SEQUENCING

IR3894 can accommodate user programmable tracking and/or sequencing options using Vp, Vref, Enable, and Power Good pins. In the block diagram presented on page 3, the error-amplifier (E/A) has been depicted with three positive inputs. Ideally, the input with the lowest voltage is used for regulating the output voltage and the other two inputs are ignored. In practice the voltage of the other two inputs should be about 200mV greater than the low-voltage input so that their effects can completely be ignored. Vp is internally biased to 3.3V via a high impedance path. For normal operation, Vp and Vref is left floating (Vref should have a bypass capacitor).

Therefore, in normal operating condition, after Enable goes high, the internal soft-start (Intl_SS) ramps up the output voltage until Vfb (voltage of feedback/Fb pin) reaches about 0.5V. Then Vref takes over and the output voltage is regulated.

Tracking-mode operation is achieved by connecting Vref to GND. In tracking-mode, Vfb always follows Vp, which means Vout is always proportional to Vp voltage (typical for DDR/VTT rail applications). The effective Vp variation range is 0V~1.2V. Fig. 5c illustrates the start-up of VTT tracking for DDR4 application. Vp is proportional to VDDQ. After Vp is established, asserting Enable initiates the internal soft-start. VTT, which is the output of POL, starts to ramp up and tracks Vp.

In sequencing mode of operation (simultaneous or ratiometric), Vref is left floating and Vp is kept to ground level until Intl_SS signal reaches the final value. Then Vp is ramped up and Vfb follows Vp. When Vp>0.5V the error-amplifier switches to Vref and the output voltage is regulated with Vref. The final Vp voltage after sequencing startup should between 0.7V ~ 3.3V.

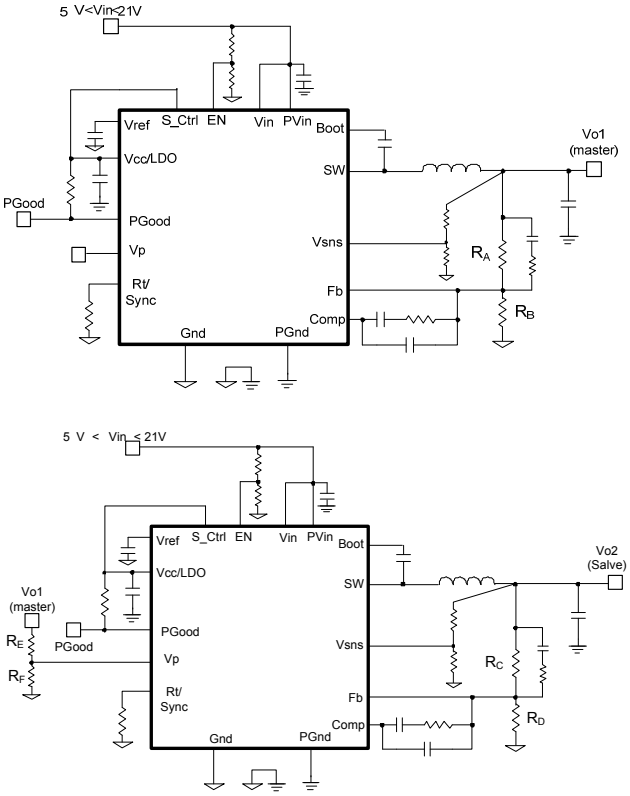


Figure 12: Application Circuit for Simultaneous and Ratiometric Sequencing

Tracking and sequencing operations can be implemented to be simultaneous or ratiometric (refer to Fig. 13 and 14). Figure 12 shows typical circuit configuration for sequencing operation. With this power-up configuration, the voltage at the Vp pin of the slave reaches 0.5V before the Fb pin of the master. If $\mathbf{R_E/R_F = R_C/R_D}$, simultaneous startup is achieved. That is, the output voltage of the slave follows that of the master until the voltage at the Vp pin of the slave reaches 0.5 V. After the voltage at the Vp pin of the slave exceeds 0.5V, the internal 0.5V reference of the slave dictates its output voltage. In reality the regulation gradually shifts from Vp to internal Vref. The circuit shown in Fig. 12 can also be used for simultaneous or ratiometric tracking operation if Vref of the slave is connected to GND. Table 2 summarizes the required conditions to achieve simultaneous/ratiometric tracking or sequencing operations.

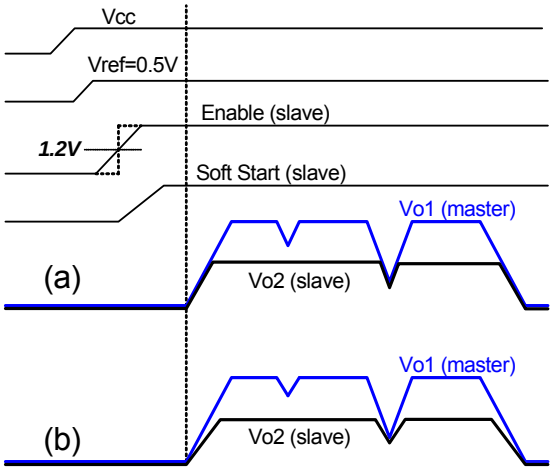


Figure 13: Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

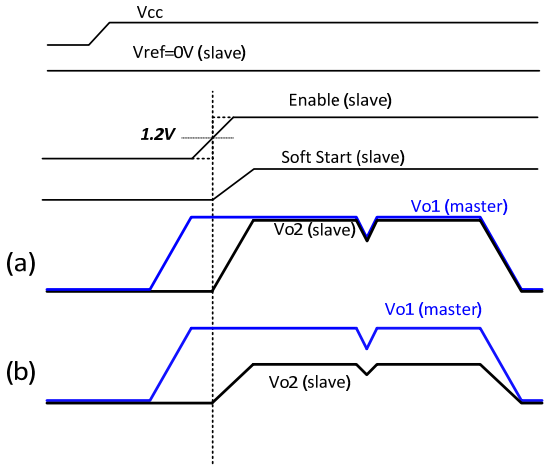


Figure 14: Typical waveforms in tracking mode of operation: (a) simultaneous, (b) ratiometric

TABLE 2: REQUIRED CONDITIONS FOR SIMULTANEOUS/RATIOMETRIC TRACKING AND SEQUENCING (FIG. 12)

Operating Mode	Vref (Slave)	Vp	Required Condition
Normal (Non-sequencing, Non-tracking)	0.5V (Floating)	Floating	—
Simultaneous Sequencing	0.5V	Ramp up from 0V	$R_A/R_B>R_E/R_F=R_C/R_D$
Ratiometric Sequencing	0.5V	Ramp up from 0V	$R_A/R_B>R_E/R_F>R_C/R_D$
Simultaneous Tracking	0V	Ramp up before En	$R_E/R_F=R_C/R_D$
Ratiometric Tracking	0V	Ramp up before En	$R_E/R_F>R_C/R_D$

VREF

This pin reflects the internal reference voltage which is used by the error amplifier to set the output voltage. In most operating conditions this pin is only connected to an external bypass capacitor and it is left floating. A 100pF ceramic capacitor is recommended for the bypass capacitor. To keep stand by current to minimum, Vref is not allowed come up until EN starts going high. In tracking mode this pin should be pulled to GND. For margining applications, an external voltage source is connected to Vref pin and overrides the internal reference voltage. The external voltage source should have a low internal resistance (<100Ω) and be able to source and sink more than 25µA.

POWER GOOD OUTPUT (TRACKING, SEQUENCING, VREF MARGINING)

IR3894 continually monitors the output voltage via the sense pin (Vsns) voltage. The Vsns voltage is an input to the window comparator with upper and lower threshold of 0.6V and 0.45V respectively. PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation.

The threshold is set differently at different operating modes and the results of the comparison sets the PGood signal. Figures 15, 16, and 17 show the timing diagram of the PGood signal at different operating modes. Vsns signal is also used by OVP comparator for detecting output over voltage condition.

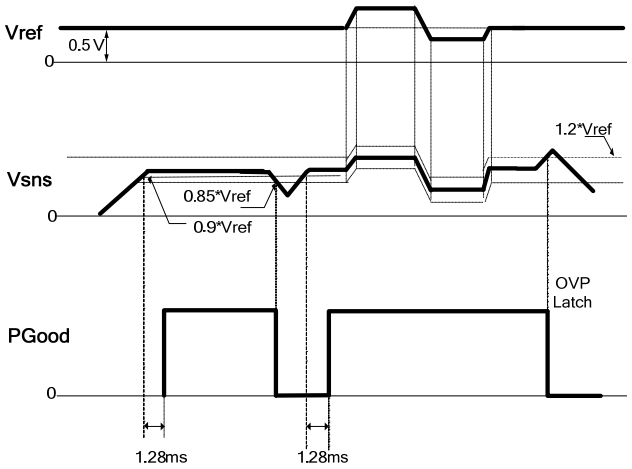


Figure 15: Non-sequence, Non-tracking Startup and Vref Margin (Vp pin floating)

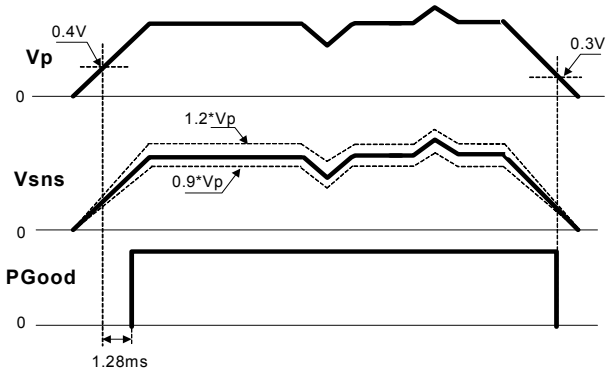


Figure 16: Vp Tracking (Vref =0V)

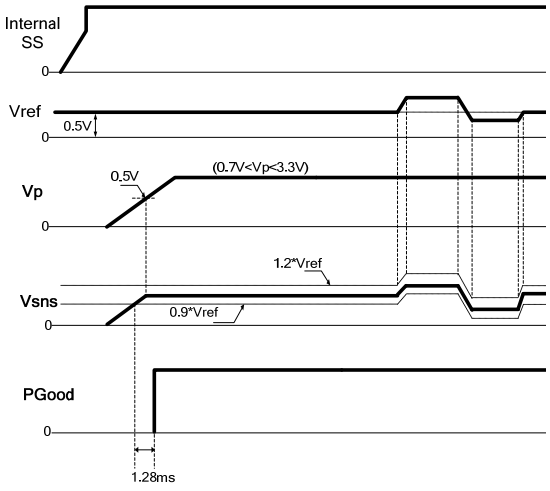


Figure 17: Vp Sequence and Vref Margin

OVER-VOLTAGE PROTECTION (OVP)

OVP is achieved by comparing Vsns voltage to an OVP threshold voltage. In non-tracking mode, OVP threshold voltage is 1.2×Vref; in tracking mode, it is set at 1.2×Vp. When Vsns exceeds the OVP threshold, an over voltage trip signal asserts after 2us (typ.) delay. Then the control FET is latched off immediately, PGood flags low. The sync FET remains on to discharge the output capacitor. When the Vsns voltage drops below the threshold, the sync FET turns off to prevent the complete depletion of the output capacitor. The control FET remains latched off until user cycle either Vcc or Enable.

OVP comparator becomes active only when the device is enabled. Furthermore, for OVP to be active Vref has to exceed 0.2V in non-tracking mode, or Vp has to exceed the threshold in tracking-mode, as illustrated in Fig 18a and Fig 18b. If either of the above conditions is not satisfied, OVP is disabled. Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally. Figure 18c shows the timing diagram for OVP in non-tracking mode.

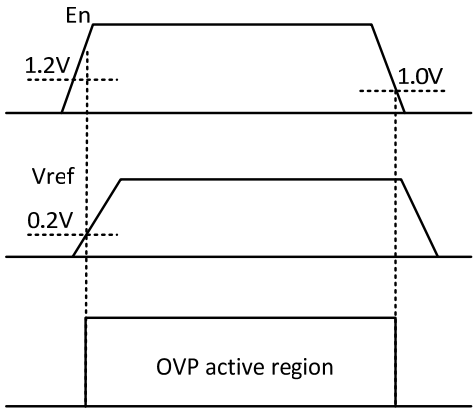


Figure 18a: Activation of OVP in non-tracking mode

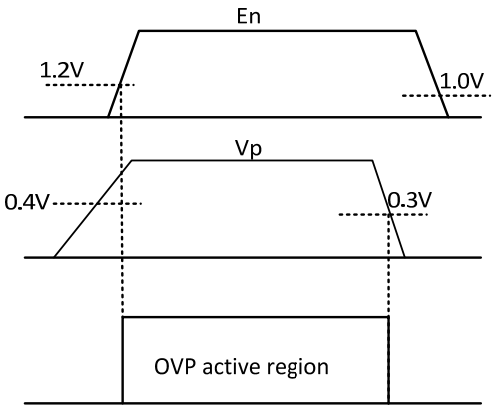


Figure 18b: Activation of OVP in tracking mode

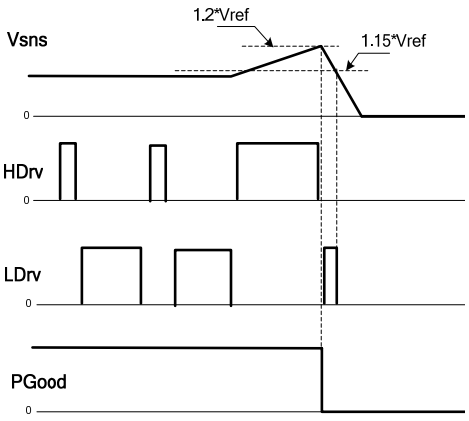


Figure 18c: Timing Diagram for OVP in non-tracking mode

SOFT-STOP (S_CTRL)

Soft-stop function can make output voltage discharge gradually. To enable this function, S_Ctrl is kept low first when EN goes high. Then S_Ctrl is pulled high to cross the logic level threshold (typical. 2V), the internal soft-start ramp is initiated. So Vo follows Intl_SS to ramp up until it reaches its steady state. In soft-stop process, S_Ctrl needs to be pulled low before EN goes low. After S_Ctrl goes below its threshold, a decreasing ramp is generated at Intl_SS with the same slope as in soft-start ramp. Vo follows this ramp to discharge softly until shutdown completely. Figure 19 shows the timing diagram of S_Ctrl controlled soft-start and soft-stop.

If the falling edge of Enable signal asserts before S_Ctrl falling edge, the converter is still turned off by Enable. Both gate drivers are turned off immediately and Vo discharges to zero. Figure 20 shows the timing diagram of Enable controlled soft-start and soft-stop. Soft stop feature also ensures that Vout discharges and also regulates the current precisely to zero with no undershoot.

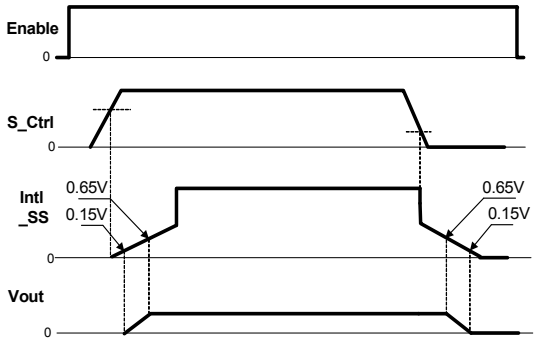


Figure 19: Timing Diagram for S_Ctrl controlled Soft Start/Soft Stop

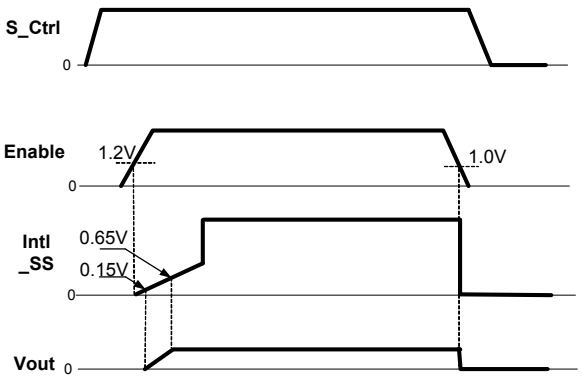


Figure 20: Timing Diagram for Enable controlled Soft Start/Shutdown

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for Ctrl FET to be reliably turned on. This is very critical parameter for low duty cycle, high frequency applications. Conventional approach limits the pulse width to prevent noise, jitter and pulse skipping. This results to lower closed loop bandwidth.

IR has developed a proprietary scheme to improve and enhance minimum pulse width which utilizes the benefits of voltage mode control scheme with higher switching frequency, wider conversion ratio and higher closed loop bandwidth, the latter results in reduction of output capacitors. Any design or application using IR3894 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 60 ns.
This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s} \qquad (3)$$

In any application that uses IR3894, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \qquad (4)$$

$$\therefore t_{on(\min)} \le \frac{V_{out}}{V_{in} \times F_s} \qquad (5)$$

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \qquad (6)$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.5 V. Therefore, for $V_{out(min)}$ = 0.5 V,

$$\therefore V_{in} \times F_s \le \frac{V_{out(\min)}}{t_{on(\min)}}$$

$$\therefore V_{in} \times F_s \le \frac{0.5\ \text{V}}{60\ \text{ns}} = 8.33\ \text{V/uS}$$

Therefore, at the maximum recommended input voltage of 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 396 kHz. Conversely, for operation at the maximum recommended operating frequency (1.65 MHz) and minimum output voltage (0.5V). The input voltage (PVin) should not exceed 5.05V, otherwise pulse skipping will happen.

MAXIMUM DUTY RATIO

A certain off-time is specified for IR3894. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time remains at a relatively fixed ratio to switching period in low and mid frequency range, while in high frequency range this ratio increases, thus the lower the maximum duty ratio at which IR3894 can operate. Figure 21 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed forward.

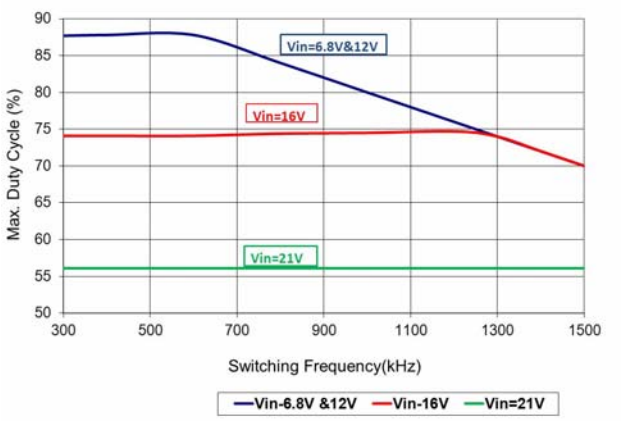


Figure 21: Maximum duty cycle vs. switching frequency.

DESIGN EXAMPLE

The following example is a typical application for IR3894. The application circuit is shown in Fig.28.

V_{in}=12 V (±10%)
V_o=1.2 V
I_o= 12 A
Ripple Voltage=±1%*V_o
ΔV_o= ±6% *V_o (for 50% load transient)
F_s=600 kHz

Enabling the IR3894

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Fig. 22.

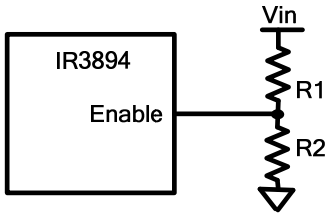


Figure 22: Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(\min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \qquad (7)$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(\min)} - V_{EN}} \qquad (8)$$

For $V_{in\ (min)}$=9.2V, R_1=49.9K and R_2=7.5K ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 39.2 KΩ, using Table 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.5V. The divider ratio is set to provide 0.5V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_5}{R_6}\right) \qquad (9)$$

When an external resistor divider is connected to the output as shown in Fig. 23.

$$R_6 = R_5 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \qquad (10)$$

For the calculated values of R5 and R6, see feedback compensation section.

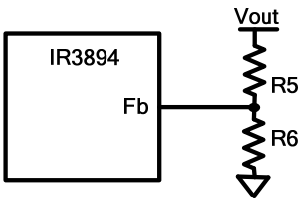


Figure 23: Typical application of the IR3894 for programming the output voltage

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Fig.24), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \qquad (11)$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage V_{in}. However, if the value of C1 is appropriately chosen, the voltage V_c across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong V_{in} + V_{cc} - V_D \qquad (12)$$

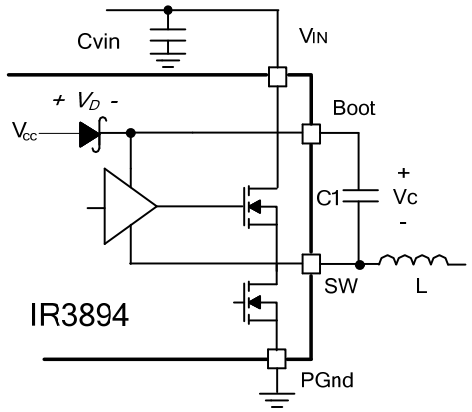


Figure 24: Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple current generated during the on time of the control FET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \qquad (13)$$

$$D = \frac{V_o}{V_{in}} \qquad (14)$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For I_o=12A and *D* = 0.1, the I_{RMS} = 3.6A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency.
For this application, it is advisable to have 4x10uF, 25V ceramic capacitors, C3216X5R1E106M from TDK.
In addition to these, although not mandatory, a 1x330uF, 25V SMD capacitor EEV-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t}; \quad \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \qquad (15)$$

Where:

V_{in} = Maximum input voltage

V_0 = Output Voltage

Δi = Inductor Peak-to-Peak Ripple Current

F_s = Switching Frequency

Δt = On time for Control FET

D = Duty Cycle

If $\Delta i \approx 30\% * I_o$, then the output inductor is calculated to be 0.5µH. Select *L*=0.51µH, 59PR9876N, from VITEC which provides a compact, low profile inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s} \qquad (16)$$

Where:

ΔV_0 = Output Voltage Ripple

ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3894 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Eight of TDK C2012X5R0J226M (22uF/0805/X5R/6.3V) capacitors is a good choice.

It is also recommended to use a 0.1µF ceramic capacitor at the output for high frequency filtering.

Feedback Compensation

The IR3894 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180°. The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \qquad (17)$$

Figure 25 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone, the system runs the risk of being unstable.

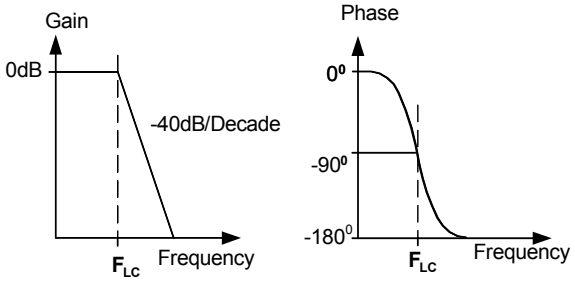


Figure 25: Gain and Phase of LC filter

The IR3894 uses a voltage-type error amplifier with high-gain (110dB) and high-bandwidth (30MHz). The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation. Type II compensation is shown in Fig. 26. This method requires that the output capacitors have enough ESR to satisfy stability requirements. If the output capacitor's ESR generates a zero at 5kHz to 50kHz, the zero generates acceptable phase margin and the Type II compensator can be used.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2\pi * ESR * C_o} \qquad (18)$$

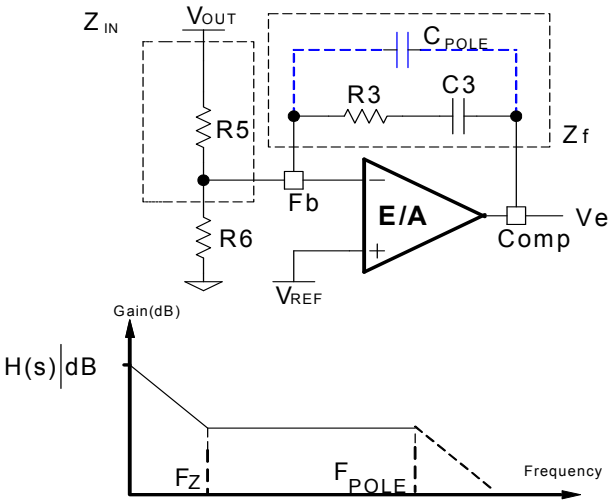


Figure 26: Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_{out}) is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_3}{sR_5C_3} \qquad (19)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$\left| H(s) \right| = \frac{R_3}{R_5} \qquad (20)$$

$$F_z = \frac{1}{2\pi * R_3 * C_3} \qquad (21)$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s \qquad (22)$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * R_5}{V_{in} * F_{LC}^2} \qquad (23)$$

Where:

V_{in} = Maximum Input Voltage
V_{osc} = Amplitude of the oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\,\% * F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \qquad (24)$$

Use equation 21 to calculate C3.

One more capacitor is sometimes added in parallel with C3 and R3. This introduces one more pole which is mainly used to suppress the switching noise.

The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_3 * C_{POLE}}{C_3 + C_{POLE}}} \qquad (25)$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_3}} \cong \frac{1}{\pi * R_3 * F_s} \qquad (26)$$

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, we should implement local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in Fig. 27.

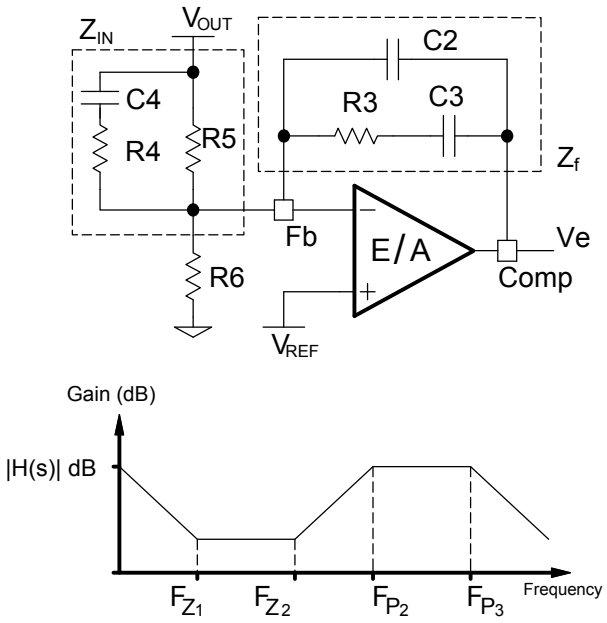


Figure 27: Type III Compensation network and its asymptotic gain plot

Again, the transfer function is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f, according to Fig. 27, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_3)\left[1+sC_4(R_4+R_5)\right]}{sR_5(C_2+C_3)\left[1+sR_3\left(\frac{C_2*C_3}{C_2+C_3}\right)\right](1+sR_4C_4)} \quad (27)$$

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad (28)$$

$$F_{P2} = \frac{1}{2\pi*R_4*C_4} \quad (29)$$

$$F_{P3} = \frac{1}{2\pi*R_3\left(\frac{C_2*C_3}{C_2+C_3}\right)} \cong \frac{1}{2\pi*R_3*C_2} \quad (30)$$

$$F_{Z1} = \frac{1}{2\pi*R_3*C_3} \quad (31)$$

$$F_{Z2} = \frac{1}{2\pi*C_4*(R_4+R_5)} \cong \frac{1}{2\pi*C_4*R_5} \quad (32)$$

Cross over frequency is expressed as:

$$F_o = R_3*C_4*\frac{V_{in}}{V_{osc}}*\frac{1}{2\pi*L_o*C_o} \quad (33)$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to crossover frequency, the compensation type can be different. Table 3 shows the compensation types for relative locations of the crossover frequency.

TABLE 3: DIFFERENT TYPES OF COMPENSATORS

Compensator Type	F_{ESR} vs F_O	Typical Output Capacitor
Type II	$F_{LC} < F_{ESR} < F_O < F_S/2$	Electrolytic
Type III	$F_{LC} < F_O < F_{ESR}$	SP Cap, Ceramic

The higher the crossover frequency is, the potentially faster the load transient response will be. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency (F_o) is selected such that:

$$F_o \le (1/5 \sim 1/10)*F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

For this design we have:

V_{in}=12V
V_o=1.2V
V_{osc}=1.8V (This is a function of Vin, pls. see feed forward section)
V_{ref}=0.5V
L_o=0.51uH
C_o=8x22uF, ESR≈3mΩ each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 22uf capacitor used in this design is 10uf at 1.2 V dc bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation.

The small signal value may be obtained from the manufacturer's datasheets, design tools or spice models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency f_{lc} and using equation (17) to compute the small signal c_o.

These result to:

F_{LC}=24.9 kHz

F_{ESR}=5.3 MHz

$F_s/2$=300 kHz

Select crossover frequency F_0=100 kHz

Since $F_{LC}<F_0<Fs/2<F_{ESR}$, Type III is selected to place the pole and zeros.

Detailed calculation of compensation Type III:

Desired Phase Boost Θ = 70°

$$F_{Z2} = F_o\sqrt{\frac{1-\sin\ \Theta}{1+\sin\ \Theta}} = 17.6\ \text{kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+\sin\ \Theta}{1-\sin\ \Theta}} = 567.1\ \text{kHz}$$

Select:

$$F_{Z1} = 0.5 * F_{Z2} = \ 8.8\ \text{kHz and}$$

$$F_{P3} = 0.5 * F_s = 300\ \text{kHz}$$

Select C_4 = 2.2nF.

Calculate R_3, C_3 and C_2:

$$R_3 = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{C_4 * V_{in}}; R_3 = 1.75\ \text{k}\Omega$$

Select R_3 = 1.82 kΩ:

$$C_3 = \frac{1}{2\pi * F_{Z1} * R_3}\ ; C_3 = 9.9\ \text{nF},\quad \text{Select: } C_3 = 10\ \text{nF}$$

$$C_2 = \frac{1}{2\pi * F_{P3} * R_3};\ C_2 = 354\ \text{pF},\quad \text{Select: } C_2 = 220\ \text{pF}$$

Calculate R_4, R_5 and R_6:

$$R_4 = \frac{1}{2\pi * C_4 * F_{P2}};\quad R_4 = 127\ \Omega,\quad \text{Select: } R_4 = 100\ \Omega$$

$$R_5 = \frac{1}{2\pi * C_4 * F_{Z2}} - R_4;\quad R_5 = 4.1\ \text{k}\Omega,$$

Select R_5 = 4.02 kΩ:

$$R_6 = \frac{V_{ref}}{V_o - V_{ref}} * R_5;\ R_6 = 2.87\ \text{k}\Omega\quad \text{Select: } R_6 = 2.87\ \text{k}\Omega$$

Setting the Power Good Threshold

In this design IR3894 is used in normal (non-tracking, non-sequencing) mode, therefore the PGood thresholds are internally set at 90% and 120% of Vref. At startup as soon as Vsns voltage reaches 0.9*0.5V=0.45V (Fig. 15), and after 1.28ms delay, PGood signal is asserted. As long as the Vsns voltage is between the threshold range, Enable is high, and no fault happens, the PGood remains high.

The following formula can be used to set the PGood threshold. $V_{out\ (PGood\_TH)}$ can be taken as 90% of Vout. Choose R8=2.87KΩ.

$$R7 = \left(\frac{V_{out(PGood\_TH)}}{0.9 * Vref} - 1\right) * R8 \qquad (34)$$

$$R7 = 4.02K\Omega$$

The PGood is an open drain output. Hence, it is necessary to use a pull up resistor, R_{PG}, from PGood pin to Vcc. The value of the pull-up resistor must be chosen such as to limit the current flowing into the PGood pin to be less than 5mA when the output voltage is not in regulation. A typical value used is 49.9kΩ.

OVP comparator also uses Vsns signal for over Voltage dectection.With above values for R7 and R8, OVP trip point ($Vout\_{OVP}$) is

$$Vout\_{OVP} = Vref * 1.2 * (R7 + R8) / R8 = 1.44V \qquad (35)$$

Vref Bypass Capacitor

A minimum value of 100pF bypass capacitor is recommended to be placed between Vref and Gnd pins.This capacitor should be placed as close as possible to Vref pin.

APPLICATION DIAGRAM

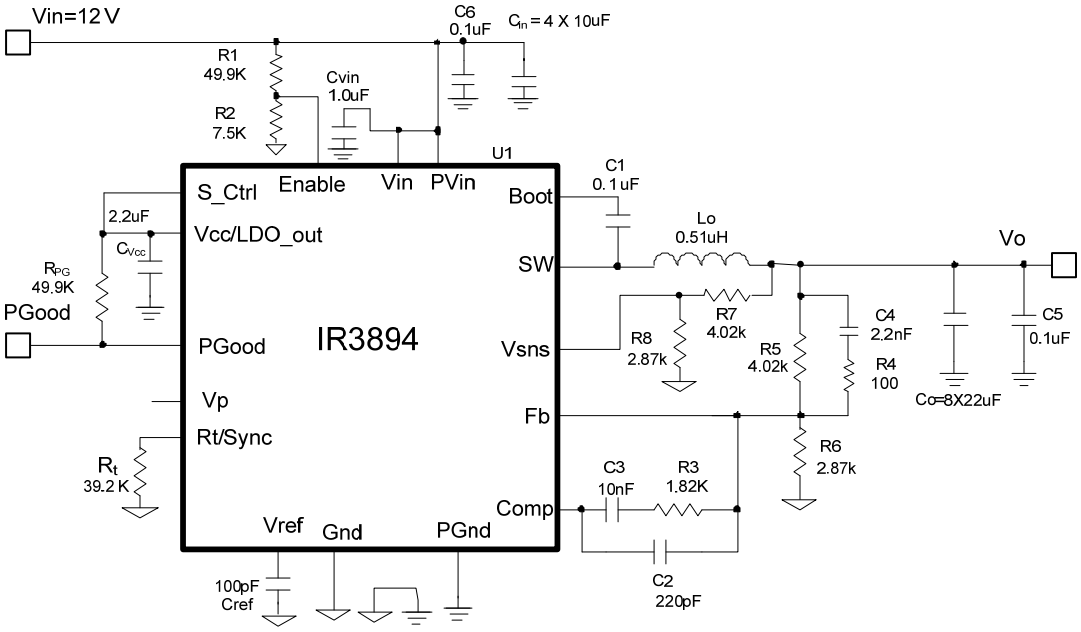


Figure 28: Application Circuit for a 12V to 1.2V, 12A Point of Load Converter

Suggested bill of materials for the application circuit

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cin	1	330uF	SMD Electrolytic F size 25V 20%	Panasonic	EEV-FK1E331P
	4	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
C1 C5 C6	3	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
Cref	1	100pF	0603,50V,NP0, 5%	Murata	GRM1885C1H101JA01D
C4	1	2200pF	0603,50V,X7R	Murata	GRM188R71H222KA01B
C2	1	220pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H221JA01D
Co	8	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
CVcc	1	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
C3	1	10nF	0603, 25V, X7R, 10%	Murata	GRM188R71E103KA01J
Cvin	1	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
Lo	1	0.51uH	SMD 11.0x7.2x7.5mm, 0.29mΩ	Vitec	59PR9876N
R3	1	1.82K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1821V
R5 R7	2	4.02K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4021V
R6 R8	2	2.87K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF2871V
R4	1	100	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1000V
Rt	1	39.2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3922V
R1 Rpg	2	49.9K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
R2	1	7.5K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF7551V
U1	1	IR3894	PQFN 5x6mm	IR	IR3894MPBF

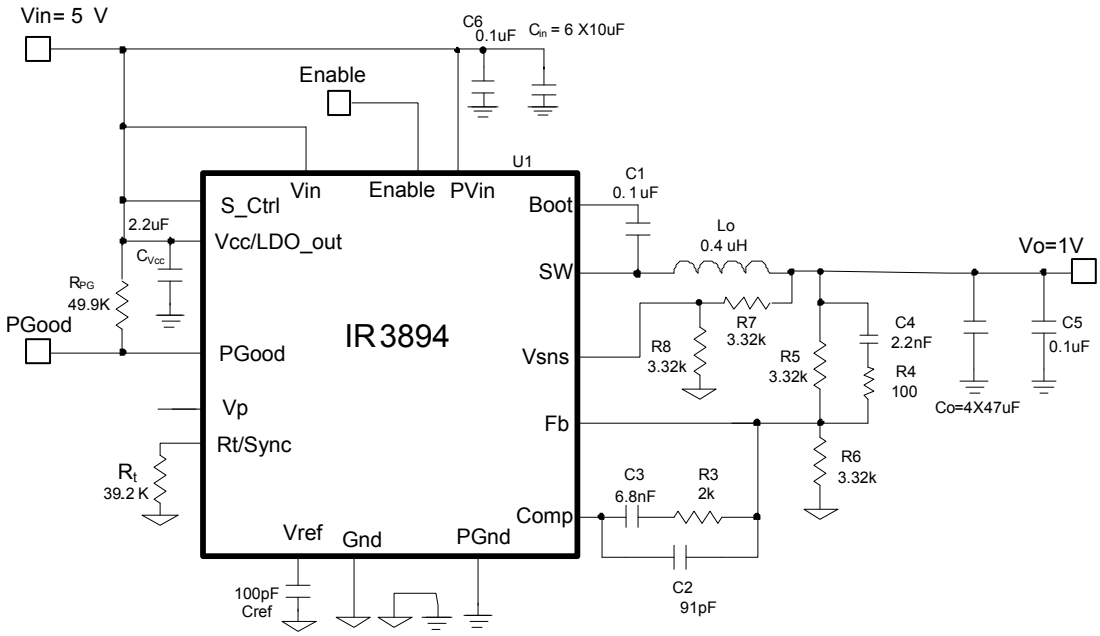


Figure 29: Application Circuit for a 5V to 1V, 12A Point of Load Converter

Suggested bill of materials for the application circuit

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cin	1	330uF	SMD Electrolytic F size 25V 20%	Panasonic	EEV-FK1E331P
	6	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
C1 C5 C6	3	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
Cref	1	100pF	0603,50V,NP0, 5%	Murata	GRM1885C1H101JA01D
C4	1	2200pF	0603,50V,X7R	Murata	GRM188R71H222KA01B
C2	1	91pF	0603, 50V, NP0, 5%	TDK	C1608C0G1H910J
Co	4	47uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J476M
CVcc	1	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
C3	1	6.8nF	0603, 25V, X7R, 10%	Murata	GRM188R71H682KA01D
Cvin	1	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
Lo	1	0.4uH	SMD 11.0x7.2x7.5mm, 0.29mΩ	Vitec	59PR9875N
R3	1	2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3GEYJ202V
R5 R6 R7 R8	4	3.32k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3321V
R4	1	100	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1000V
Rt	1	39.2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3922V
Rpg	1	49.9K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
U1	1	IR3894	PQFN 5x6mm	IR	IR3894MPBF

TYPICAL OPERATING WAVEFORMS

PVin = 12V, Vo = 1.2V, Iout = 0-12A, Room Temperature, No Air flow

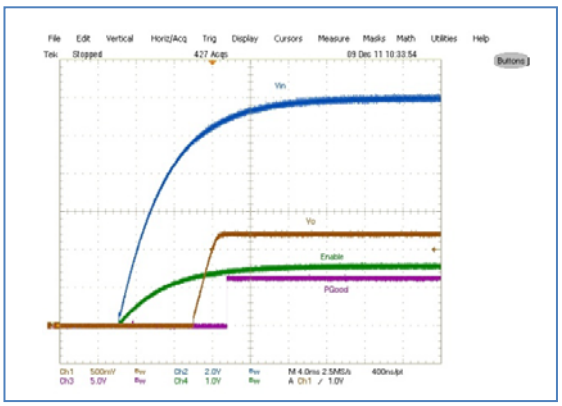


Figure 30: Start up at 12A Load,
Ch_1:Vout, Ch_2:Vin, Ch_3:P_{Good} Ch_4:Enable

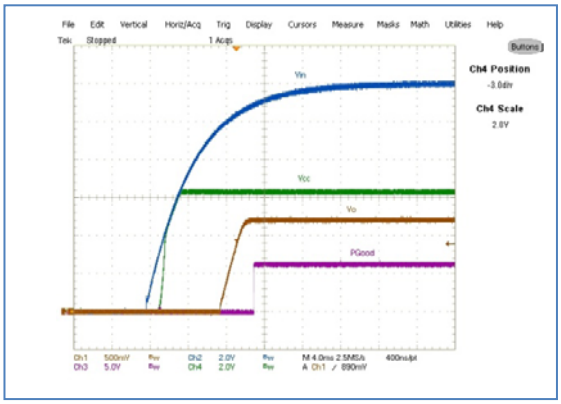


Figure 31: Start up at 12A Load,
Ch_1: Vout , Ch_2:Vin, Ch_3:P_{Good}, Ch_4:V_{cc}

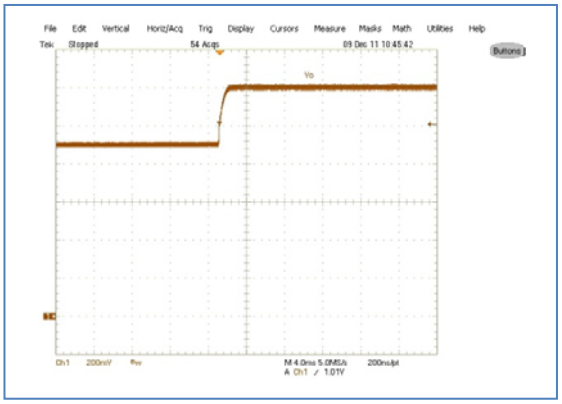


Figure 32: Start up with Pre Bias Voltage,
0A Load, Ch_1:V_o

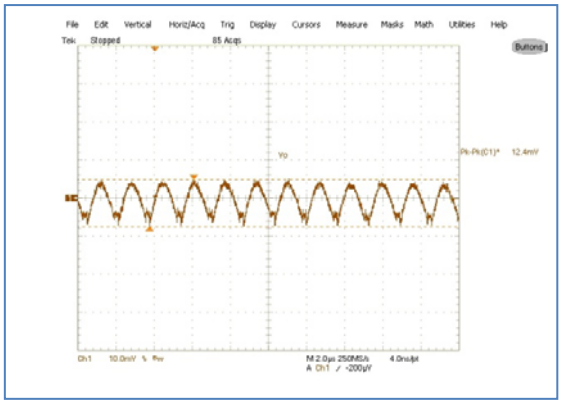


Figure 33: Output Voltage Ripple,
12A Load, Ch_1:Vout

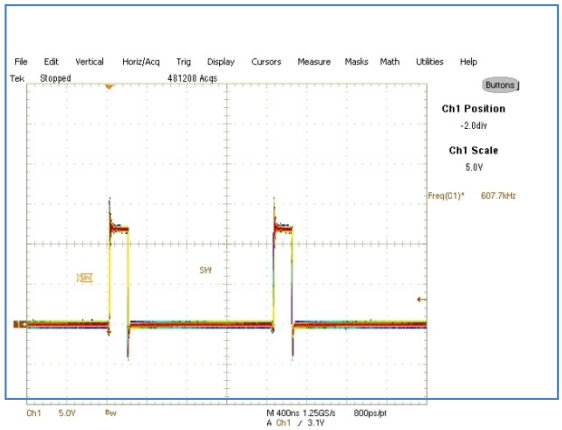


Figure 34: Inductor node at 12A load, Ch_1:SW node

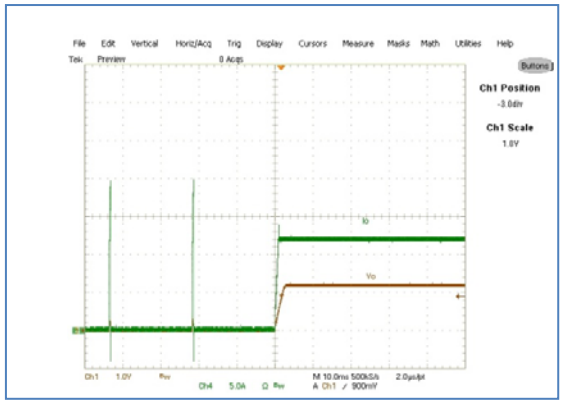


Figure 35: Short Circuit Recovery,
Ch_1-Vout, Ch_4:Iout (5A/Div)

TYPICAL OPERATING WAVEFORMS

Vin = 12V, Vo = 1.2V, Iout = 0-12A, Room Temperature, No Air Flow

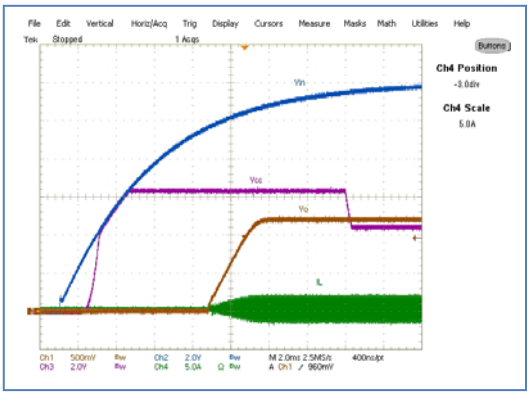


Figure 36: Turn on at No Load showing Vcc level
Ch1-Vout, Ch2-Vin,Ch3-Vcc,Ch4-Inductor current

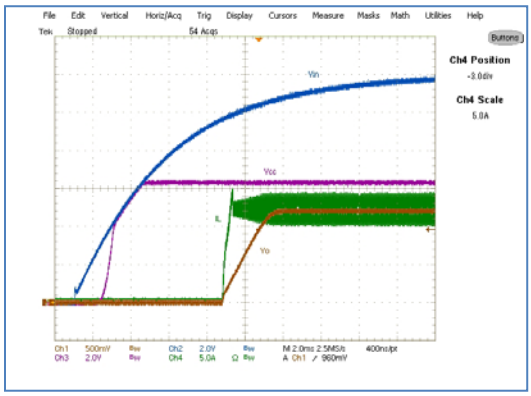
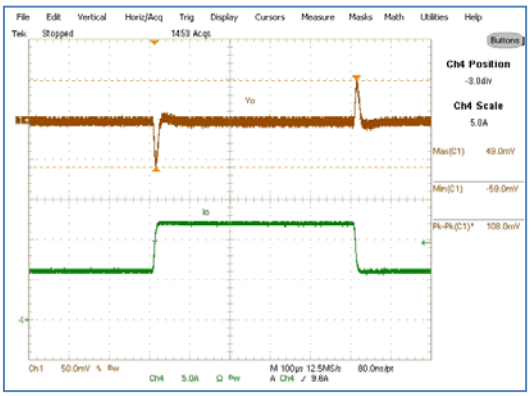
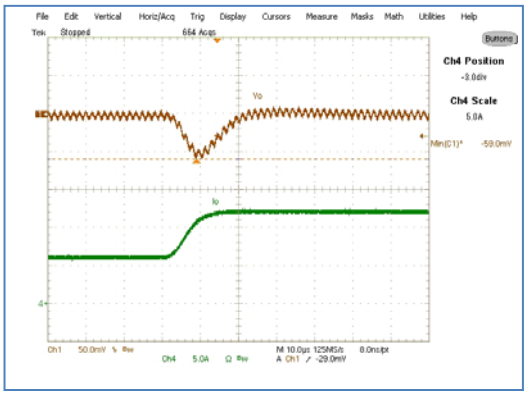


Figure 37: Turn on at No Load showing Vcc level
Ch1-Vout, Ch2-Vin,Ch3-Vcc,Ch4-Inductor current





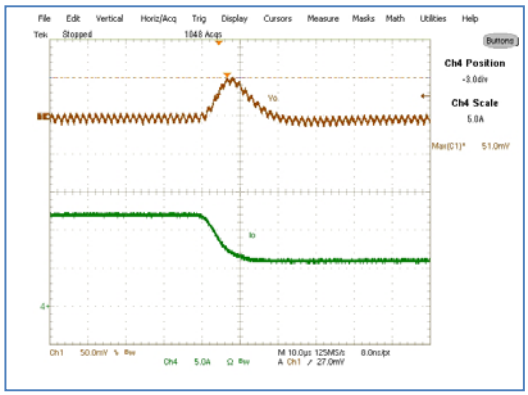


Figure 38: Transient Response, 6A to 12A step at 2.5A/uSec slew rate,
Ch_1:V_{out}, Ch4-Iout (5A/Div)

TYPICAL OPERATING WAVEFORMS

PVin = 12V, Vo = 1.2V, Iout = 0-12A, Room Temperature, No Air flow

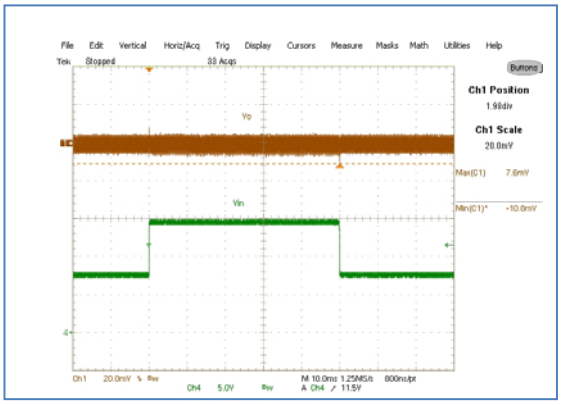


Figure 39: Feed forward for Vin change from 6.8 to 16V, Ch_1:V_{out}, Ch_4:V_{in}

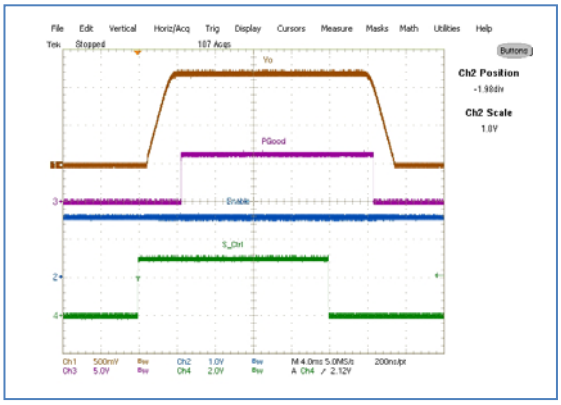


Figure 40: Start/Stop using S_Ctrl Pin, Ch_1:V_{out}, Ch_2:Enable, Ch_3: P_{Good},Ch_4:S_Ctrl

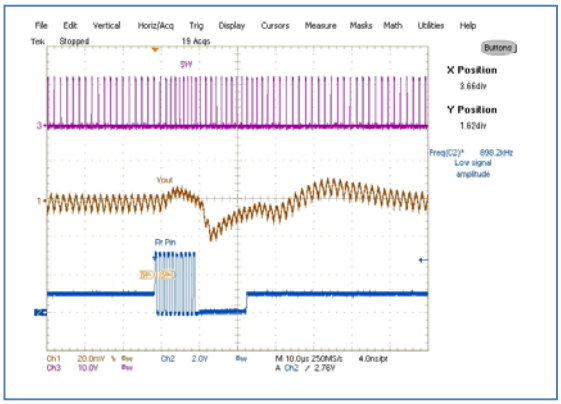


Figure 41: External frequency synchronization to 800kHz from free running 600kHz, Ch_1:V_o, Ch2:Rt/Sync voltage,Ch_3:SW Node voltage

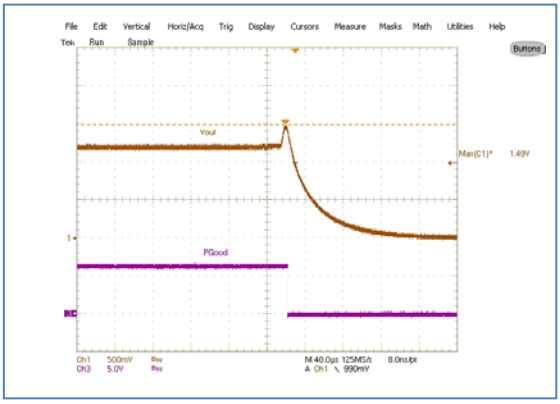


Figure 42: Over Voltage Protection, Ch_1:Vout, Ch_3:PGood

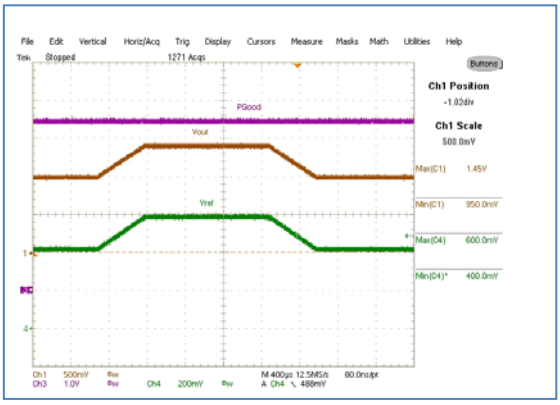


Figure 43: Voltage margining using Vref pin Ch_1:Vout, Ch3:P_{Good},Ch_4:V_{ref}

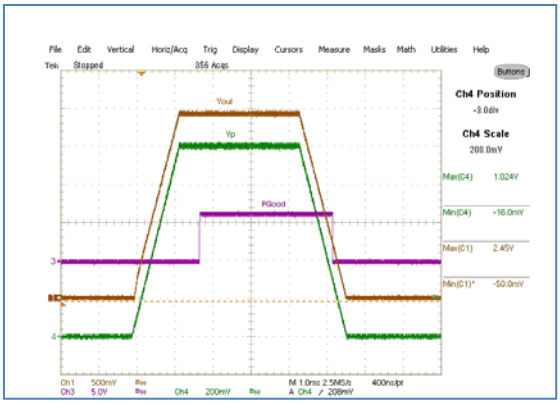


Figure 44: Voltage tracking using Vp pin Ch_1-Vout, Ch3:P_{Good} ,Ch_4:V_p

TYPICAL OPERATING WAVEFORMS

Vin = 12V, Vo = 1.2V, Iout = 0-12A, Room Temperature, No Air Flow

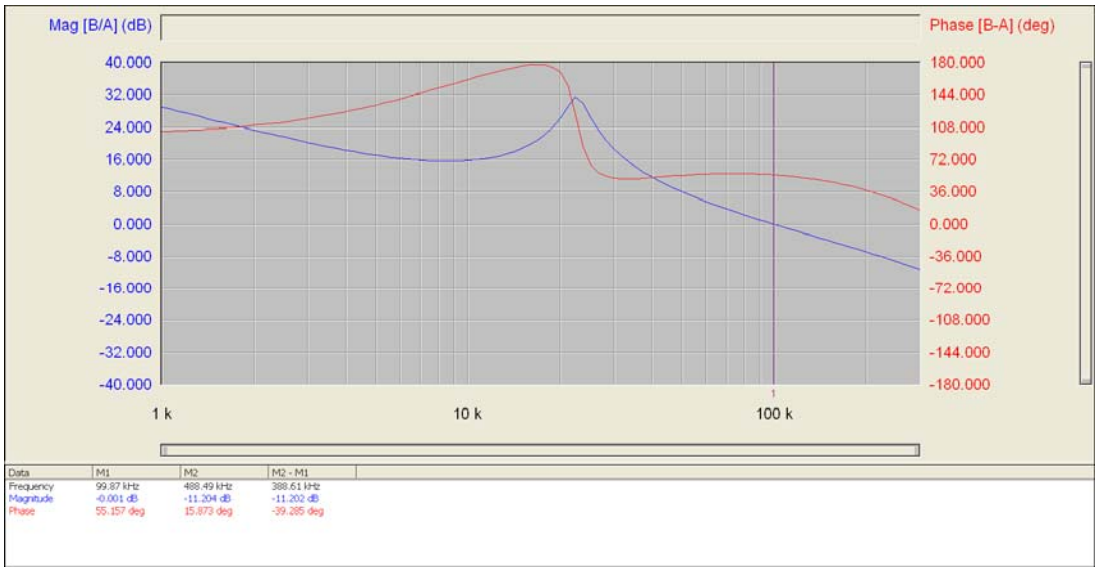


Figure 45: Bode Plot at 12A load shows a bandwidth of 99.9kHz and phase margin of 55.2°

Figure 46: Thermal Image of the Board at 12A Load,
Test Point 1 is IR3894,
Test Point 2 is inductor

LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3899 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3899.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vin, Vcc and Vref should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figures 46a-d illustrates the implementation of the layout guidelines outlined above, on the IRDC3899 4-layer demo board.

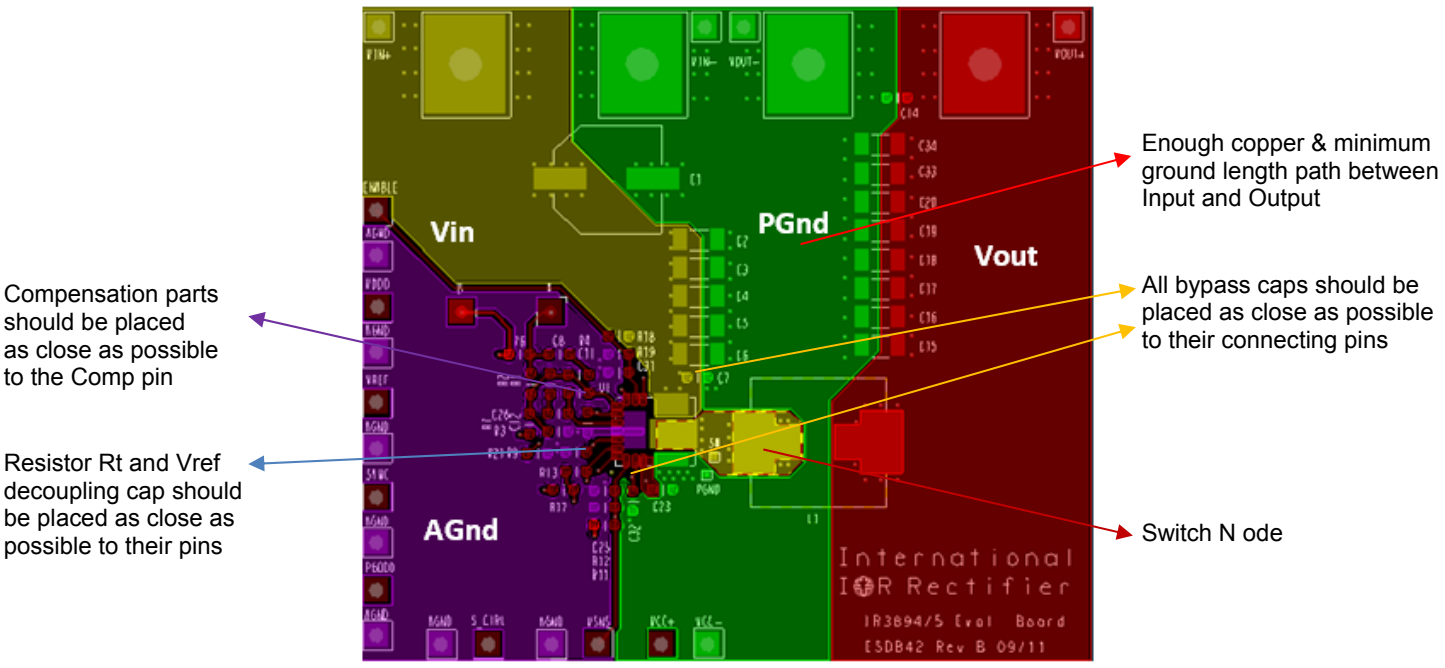


Figure 47a: IRDC3894 Demo board Layout Considerations – Top layer

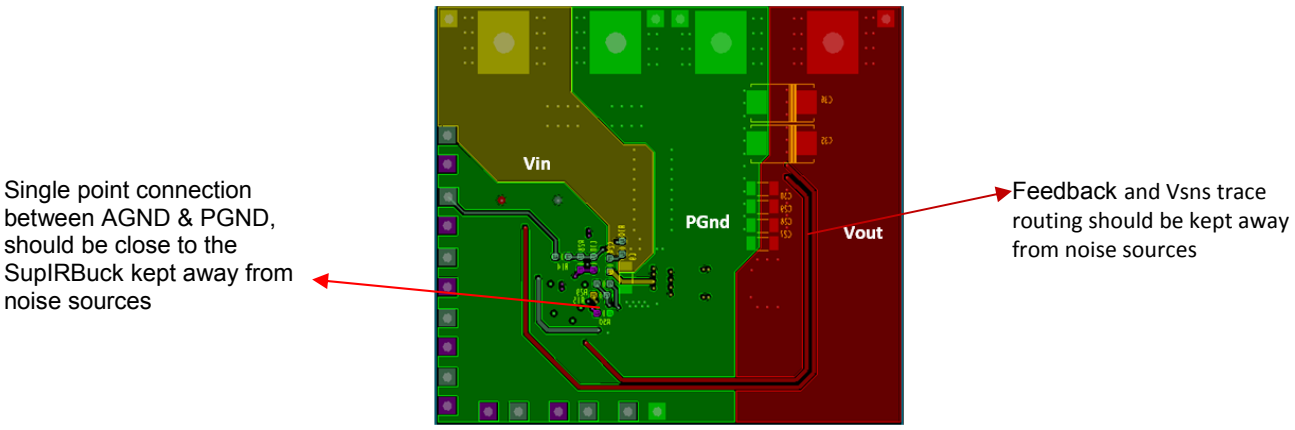


Figure 47b: IRDC3894 Demo board Layout Considerations – Bottom Layer

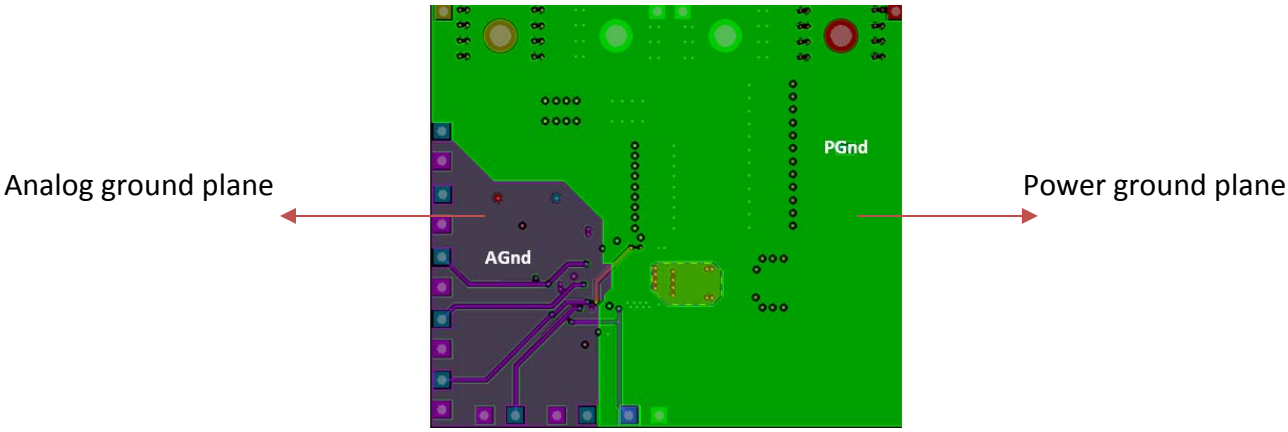


Figure 47c: IRDC3894 Demo board Layout Considerations – Mid Layer 1

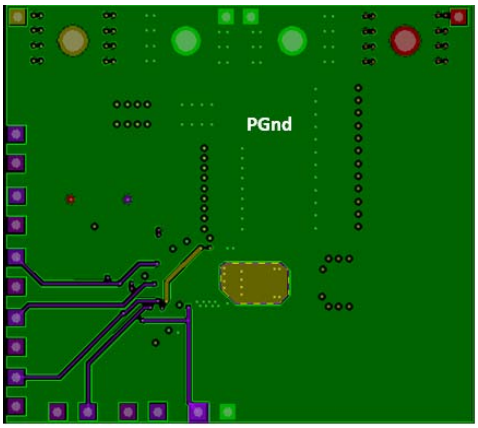


Figure 47d: IRDC3894 Demo board Layout Considerations – Mid Layer 2

PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to "SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note**." (AN1132)**

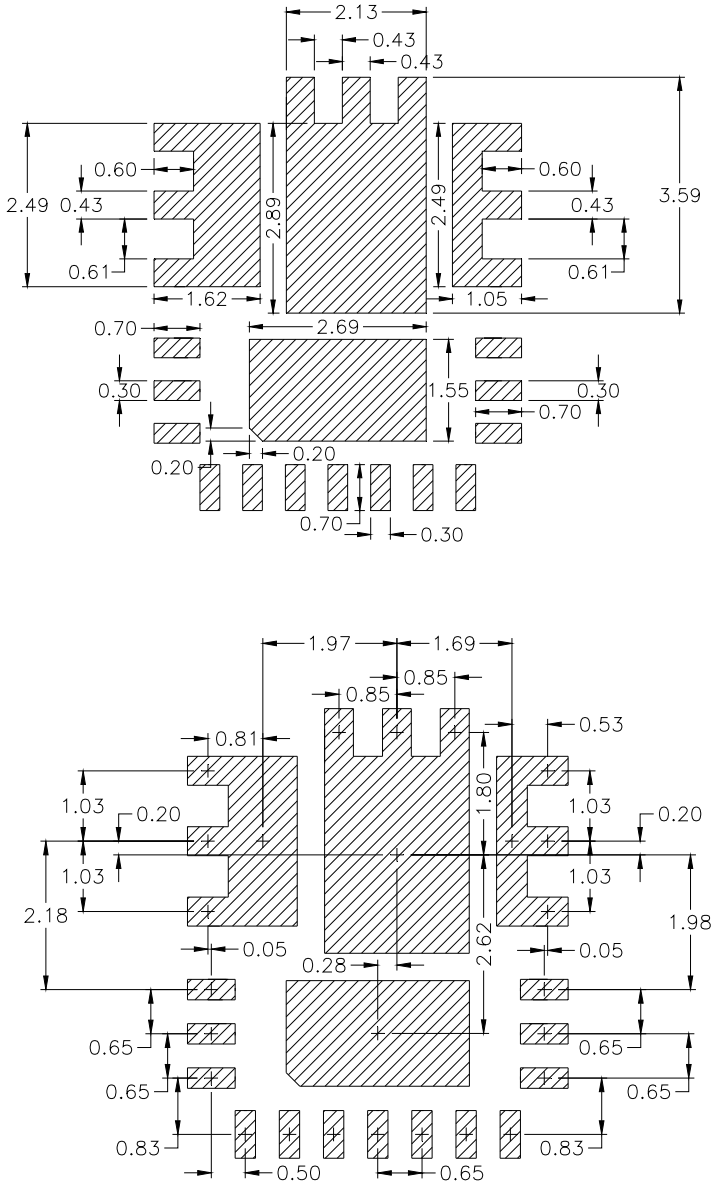


Figure 48: PCB Metal Pad Sizing and Spacing (all dimensions in mm)

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format

SOLDER RESIST

- IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.
- When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)
- However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined or Copper Defined.
- When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment.
- Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

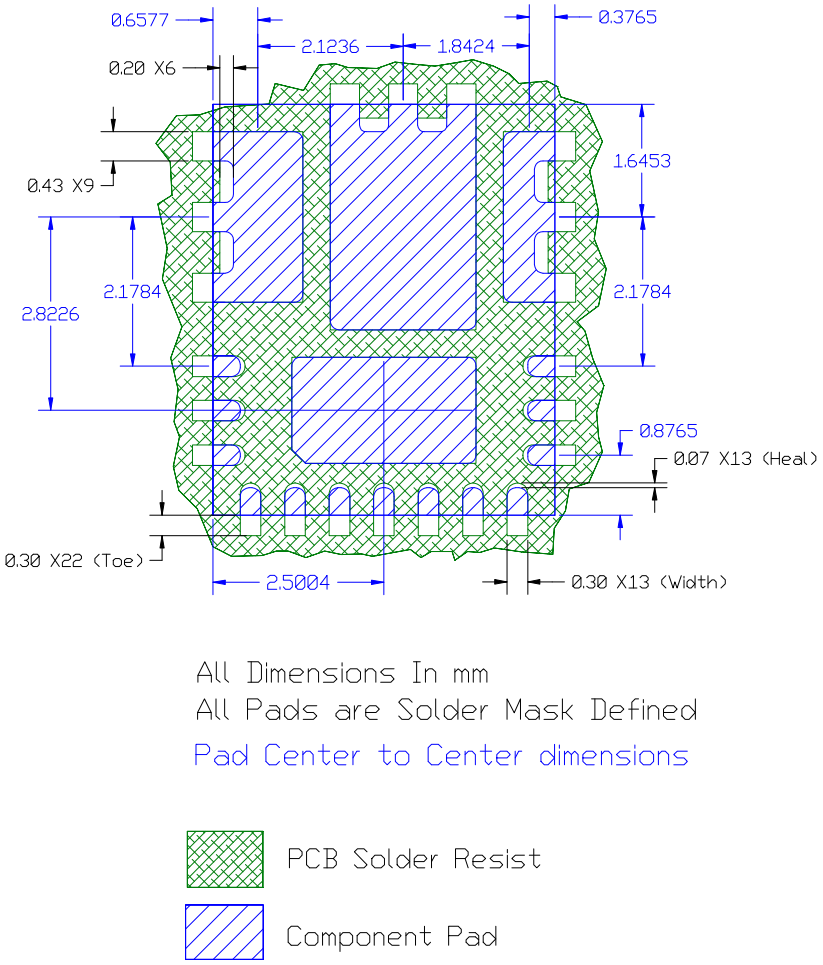


Figure 49: Solder resist

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STENCIL DESIGN

- Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.
- Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

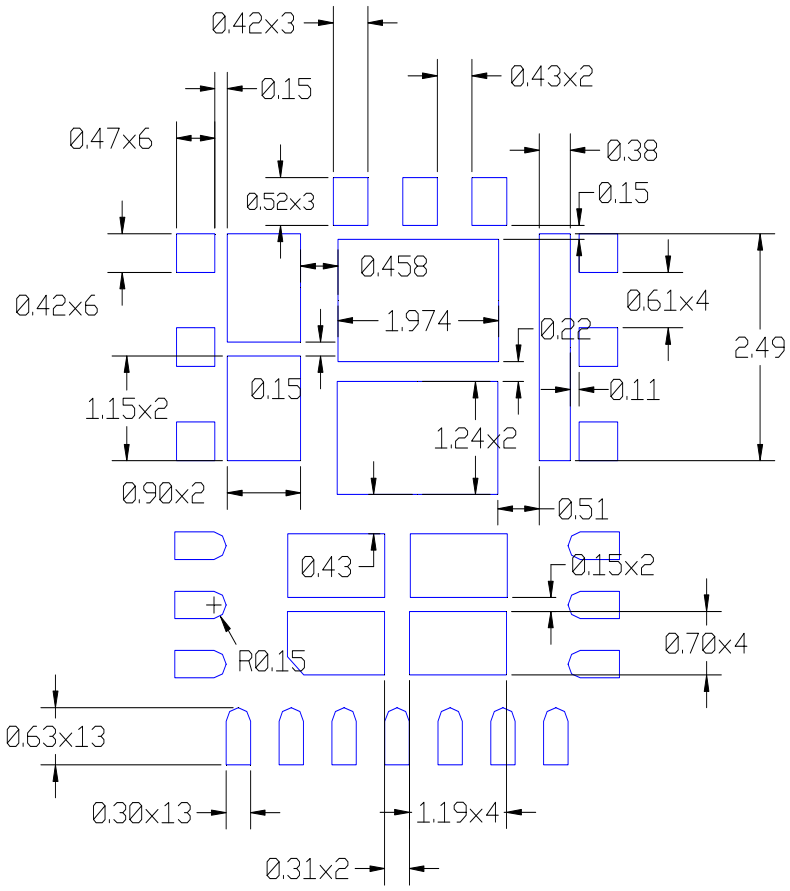

Figure 50: Stencil Pad Spacing (all dimensions in mm)

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MARKING INFORMATION

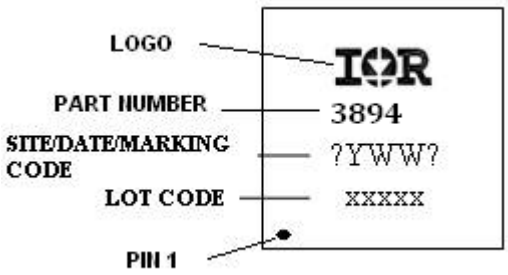

Figure 51: Marking information

PACKAGE INFORMATION

DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.800	1.000	0.0315	0.0394	L	0.350	0.450	0.0138	0.0177
A1	0.000	0.050	0.0000	0.0020	M	2.441	2.541	0.0961	0.1000
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0316
b1	0.250	0.350	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.969 BASIC		Q	1.265	1.365	0.0498	0.0537
E	6.000 BASIC		2.362 BASIC		R	2.644	2.744	0.1041	0.1080
e	1.033 BASIC		0.0407 BASIC		S	1.500	1.600	0.0591	0.0630
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0335 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	

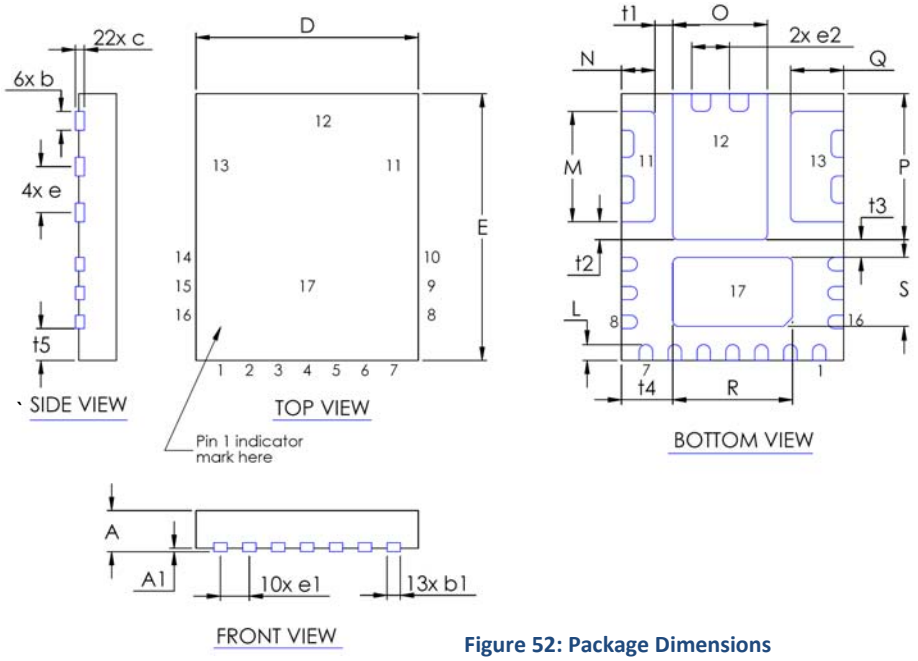

Figure 52: Package Dimensions

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