

## LOW-JITTER SAW OSCILLATOR (SPSO)

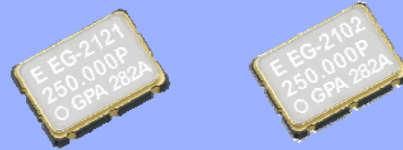
OUTPUT : LV-PECL, LVDS, HCSL

# EG-2121 / 2102CA

- Frequency range : 53.125 MHz to 700 MHz
- Supply voltage : 2.5 V ... EG-2121CA  
3.3 V ... EG-2102CA
- Output : LV-PECL or LVDS or HCSL
- Function : Output enable (OE)
- External dimensions : 7.0 × 5.0 × 1.2 mm
- Very low jitter and low phase noise by SAW unit.



Product Number (please contact us)  
 EG-2121CA: Q3805CAx0xxx00  
 : X1M000101xxxx00  
 EG-2102CA: Q3806CA00xxx00  
 : X1M000091xxxx00



Actual size

EG-2121CA

EG-2102CA



### Specifications (characteristics)

#### ► Differential LV-PECL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		LV-PECL		
Output frequency range	$f_o$	53.125 MHz to 500 MHz	100 MHz to 700 MHz	Please contact us about available frequencies.
Supply voltage	$V_{cc}$	2.5 V $\pm 0.125$ V	3.3 V $\pm 0.3$ V	
Storage temperature	$T_{stg}$	-40 °C to +100 °C		Storage as single product.
Operating temperature	$T_{use}$	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance	$f_{tol}$	G: $\pm 50 \times 10^{-6}$ ,H: $\pm 100 \times 10^{-6}$		
Current consumption	$I_{cc}$	80 mA Max.	100 mA Max.	OE= $V_{cc}$ , L_ECL=50 $\Omega$
Disable current	$I_{dis}$	20 mA Max.	32 mA Max.	OE=GND
Symmetry	SYM	P:40 % to 60 % ( $f_o > 350$ MHz)	P:45 % to 55 %	at outputs crossing point
		P:45 % to 55 % ( $f_o \leq 350$ MHz)		
		D:48 % to 52 % ( $f_o \leq 175$ MHz)		
Output voltage	$V_{OH}$	1.55 V Typ.	2.35 V Typ.	DC characteristics
	$V_{cc}-1.025$ V to $V_{cc}-0.88$ V			
	$V_{OL}$	0.8 V Typ.	1.6 V Typ.	
Output load condition (ECL)	$L_{ECL}$	50 $\Omega$		Terminated to $V_{cc} - 2.0$ V
Input voltage	$V_{IH}$	70 % $V_{cc}$ Min.		OE terminal
	$V_{IL}$	30 % $V_{cc}$ Max.		
Rise time / Fall time	$t_r / t_f$	400 ps Max.		Between 20% and 80% of ( $V_{OH}-V_{OL}$ )
Start-up time	$t_{str}$	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	$tpj$	0.8 ps Max.		$f_o < 100$ MHz
		0.5 ps Max.		100 MHz $\leq f_o < 200$ MHz
		0.3 ps Max.		200 MHz $\leq f_o$
Frequency aging	$f_{aging}$	$\pm 10 \times 10^{-6}$ / year Max.		+25 °C, First year, $V_{cc}=2.5$ V,3.3 V

#### ► LVDS Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		LVDS		
Output frequency range	$f_o$	53.125 MHz to 700 MHz		Please contact us about available frequencies.
Supply voltage	$V_{cc}$	2.5 V $\pm 0.125$ V	3.3 V $\pm 0.3$ V	
Storage temperature	$T_{stg}$	-40 °C to +100 °C		Storage as single product.
Operating temperature	$T_{use}$	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance	$f_{tol}$	G: $\pm 50 \times 10^{-6}$ ,H: $\pm 100 \times 10^{-6}$		
Current consumption	$I_{cc}$	30 mA Max.	45 mA Max.	OE= $V_{cc}$ , L_LVDS= 100 $\Omega$
Disable current	$I_{dis}$	20 mA Max.	30 mA Max.	OE=GND
Symmetry	SYM	L:40 % to 60 % ( $f_o > 350$ MHz)	L:40 % to 60 % ( $f_o > 350$ MHz)	at outputs crossing point
		L:45 % to 55 % ( $f_o \leq 350$ MHz)		
		V:48 % to 52 % ( $f_o \leq 175$ MHz)		
Output voltage	$V_{OD}$	350 mV Typ. 247 mV to 454 mV		DC characteristics
	$dV_{OD}$	50 mV Max.		
	$V_{OS}$	1.25 V Typ. 1.125 V to 1.375 V		
	$dV_{OS}$	150 mV Max.		
Output load condition (LVDS)	$L_{LVDS}$	100 $\Omega$		Connected between OUT to $\overline{OUT}$
Input voltage	$V_{IH}$	70 % $V_{cc}$ Min.		OE terminal
	$V_{IL}$	30 % $V_{cc}$ Max.		
Rise time / Fall time	$t_r / t_f$	400 ps Max.		Between 20 % and 80 % of Differential Output Peak to Peak voltage
Start-up time	$t_{str}$	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	$tpj$	0.8 ps Max.		$f_o < 100$ MHz
		0.5 ps Max.		100 MHz $\leq f_o < 200$ MHz
		0.3 ps Max.		200 MHz $\leq f_o$
Frequency aging	$f_{aging}$	$\pm 10 \times 10^{-6}$ / year Max.		+25 °C, First year, $V_{cc}=2.5$ V,3.3 V

**► HCSL Output**

Item	Symbol	EG-2121CA		EG-2102CA		Conditions / Remarks
		HCSL				
Output frequency range	f <sub>o</sub>	100 MHz to 350 MHz				Please contact us about available frequencies.
Supply voltage	V <sub>cc</sub>	2.5 V ±0.125 V		3.3 V ±0.3 V		
Storage temperature	T <sub>stg</sub>	-40 °C to +125 °C				Storage as single product.
Operating temperature	T <sub>use</sub>	P: 0 °C to +70 °C ,R: -5 °C to +85 °C ,S: -20 °C to +70 °C				
Frequency tolerance	f <sub>tol</sub>	G: ±50 × 10 <sup>-6</sup> ,H: ±100 × 10 <sup>-6</sup>				OE=V <sub>cc</sub> ,L <sub>HCSL</sub> =50 Ω
Current consumption	I <sub>cc</sub>	80 mA Max.		85 mA Max.		
Disable current	I <sub>dis</sub>	20 mA Max.		35 mA Max.		OE=GND
Symmetry	SYM	45 % to 55 %				at outputs crossing point
Output Voltage	V <sub>OH</sub>	0.75 V Typ.				DC characteristics
	V <sub>OL</sub>	-0.3 V Typ.				
Output load condition (HCSL)	L <sub>HCSL</sub>	50 Ω				Terminated to GND
Input voltage	V <sub>IH</sub>	70 % V <sub>cc</sub> Min.				OE terminal
	V <sub>IL</sub>	30 % V <sub>cc</sub> Max.				
Rise time / Fall time	t <sub>r</sub> / t <sub>f</sub>	500 ps Max.				Between 0.175 V and 0.525 V of output
Start-up time	t <sub>str</sub>	10 ms Max.				Time at minimum supply voltage to be 0 s
Phase Jitter	t <sub>pj</sub>	0.8 ps Max.				f <sub>o</sub> < 100 MHz
		0.5 ps Max.				100 MHz ≤ f <sub>o</sub> < 200 MHz
		0.3 ps Max.				200 MHz ≤ f <sub>o</sub>
Frequency aging *2	f <sub>aging</sub>	± 10 × 10 <sup>-6</sup> / year Max.				+25 °C, First year, V <sub>cc</sub> =2.5 V,3.3 V

 Product Name **EG-2121 CA 250.000000MHz P G P A**

(Standard form) ① ② ③ ④⑤⑥⑦

①Model ②Package type ③Frequency

④Output/Symmetry ⑤Frequency tolerance ⑥Operating temperature

⑦Frequency aging (A\*1: Frequency tolerance include aging, N\*2: Frequency tolerance exclude aging)

\*1 This includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, and aging(+25 °C,10 years).

\*2 This includes initial frequency tolerance, temperature variation, supply voltage variation, and reflow drift(except aging).

(⑤⑥⑦: GRA, GSA are not available)

 (⑤⑥: As for LV-PECL and LVDS output, for 53.125 MHz ≤ f<sub>o</sub> < 100 MHz only HP is available)

④	Output	Symmetry	
		EG-2121CA	EG-2102CA
P	LV-PECL	40 % to 60 % (f <sub>o</sub> > 350 MHz) 45 % to 55 % (f <sub>o</sub> ≤ 350 MHz)	45 % to 55 %
D	LV-PECL	48 % to 52 % (f <sub>o</sub> ≤ 175 MHz)	48 % to 52 % (f <sub>o</sub> ≤ 350 MHz)
L	LVDS	40 % to 60 % (f <sub>o</sub> > 350 MHz) 45 % to 55 % (f <sub>o</sub> ≤ 350 MHz)	
V	LVDS	48 % to 52 % (f <sub>o</sub> ≤ 175 MHz)	
H	HCSL	45 % to 55 %	

⑤Frequency tolerance	
G	±50 × 10 <sup>-6</sup>
H	±100 × 10 <sup>-6</sup>

⑥Operating temperature	
P	0 to +70°C
R	-5 to +85°C
S	-20 to +70°C

**Table 2 Jitter**

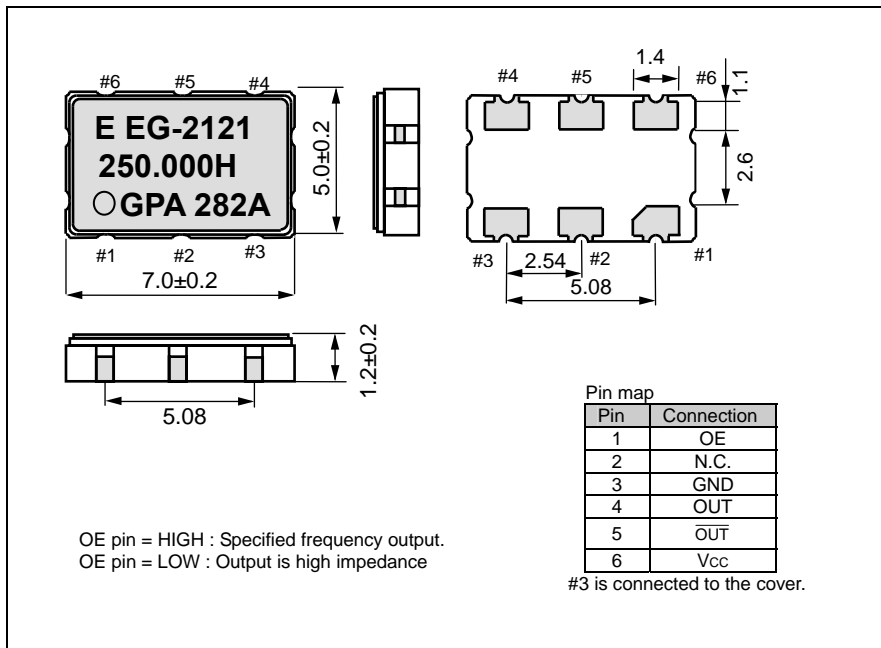
Item	Symbol	Specifications	Remarks
Jitter *	t <sub>DJ</sub>	0.2 ps Typ.	Deterministic Jitter
	t <sub>RJ</sub>	3 ps Typ.	Random Jitter
	t <sub>RMS</sub>	3 ps Typ.	σ (RMS of total distribution)
	t <sub>p-p</sub>	25 ps Typ.	Peak to Peak
	t <sub>acc</sub>	4 ps Typ.	Accumulated Jitter(σ) n=2 to 50000 cycles

\* Tested using a DTS-2075 Digital timing system made by WAVECREST with jitter analysis software VISI6. : Differential LV-PECL, LVDS output

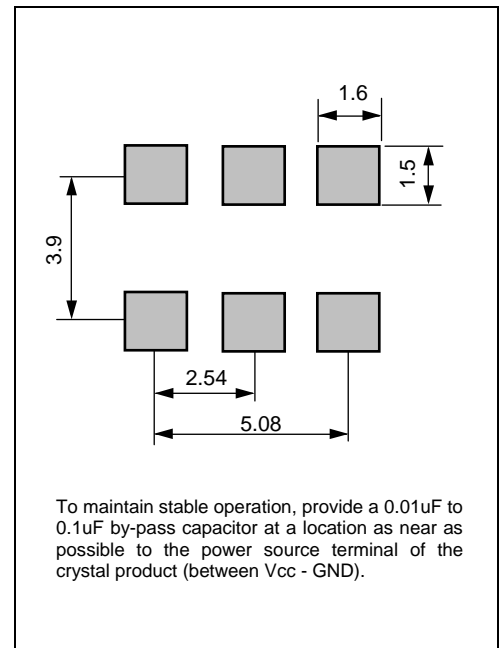
\* Based on SIA-3100C signal integrity analyzer made from WAVECREST. : HCSL output

**External dimensions**

(Unit:mm)


**Footprint (Recommended)**

(Unit:mm)



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	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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