To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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R1EX25032ASA00A/R1EX25064ASA00A
R1EX25032ATA00A/R1EX25064ATA00A

Serial Peripheral Interface
32k EEPROM (4-kword × 8-bit)
64k EEPROM (8-kword × 8-bit)
Electrically Erasable and Programmable Read Only Memory

REJ03C0358-0002
Preliminary
Rev.0.02
Jan.14.2009

Description

R1EX25xxx Series is the Serial Peripheral Interface compatible (SPI) EEPROM (Electrically Erasable and Programmable ROM). It realizes high speed, low power consumption and a high level of reliability by employing advanced MONOS memory technology and CMOS process and low voltage circuitry technology. It also has a 32-byte page programming function to make it's write operation faster.

Note: Renesas Technology's serial EEPROM are authorized for using consumer applications such as cellular phones, camcorders, audio equipments. Therefore, please contact Renesas Technology's sales office before using industrial applications such as automotive systems, embedded controllers, and meters.

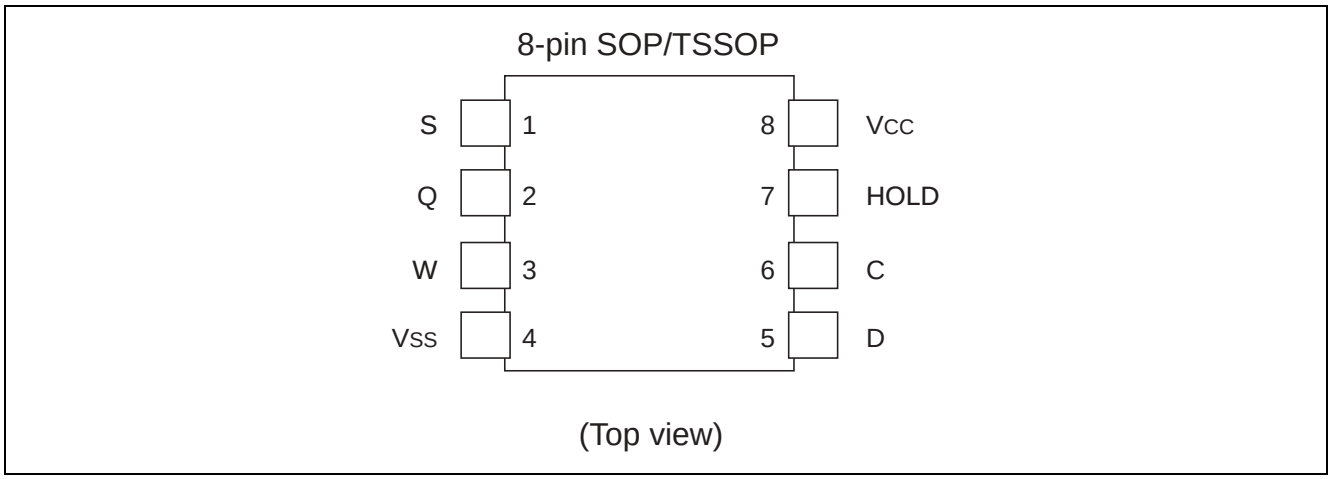
Features

- Single supply: 1.8 V to 5.5 V
- Serial Peripheral Interface compatible (SPI bus)
  - SPI mode 0 (0,0), 3 (1,1)
- Clock frequency: 5 MHz (2.5 V to 5.5 V), 3 MHz (1.8 V to 5.5 V)
- Power dissipation:
  - Standby: 2µA (max)
  - Active (Read): 3.0 mA (max)
  - Active (Write): 3.5 mA (max)
- Automatic page write: 32-byte/page
- Write cycle time: 5 ms
- Endurance: 1,000k Cycles @25°C
- Data retention: 100 Years @25°C
- Small size packages: SOP-8pin, TSSOP-8pin
- Shipping tape and reel
  - TSSOP-8pin : 3,000 IC/reel
  - SOP-8pin : 2,500 IC/reel
- Temperature range: –40 to +85°C
- Lead free product.

Ordering Information

Type No.	Internal organization	Operating voltage	Frequency	Package
R1EX25032ASA00A	32-kbit (4096 × 8-bit)	1.8 V to 5.5 V	5 MHz (2.5 V to 5.5 V) 3 MHz (1.8 V to 5.5V)	150mil 8-pin plastic SOP PRSP0008DF-B (FP-8DBV) Lead free
R1EX25064ASA00A	64-kbit (8192 × 8-bit)			
R1EX25032ATA00A	32-kbit (4096 × 8-bit)	1.8 V to 5.5 V	5 MHz (2.5 V to 5.5 V) 3 MHz (1.8 V to 5.5 V)	8-pin plastic TSSOP PTSP0008JC-B (TTP-8DAV) Lead free
R1EX25064ATA00A	64-kbit (8192 × 8-bit)			

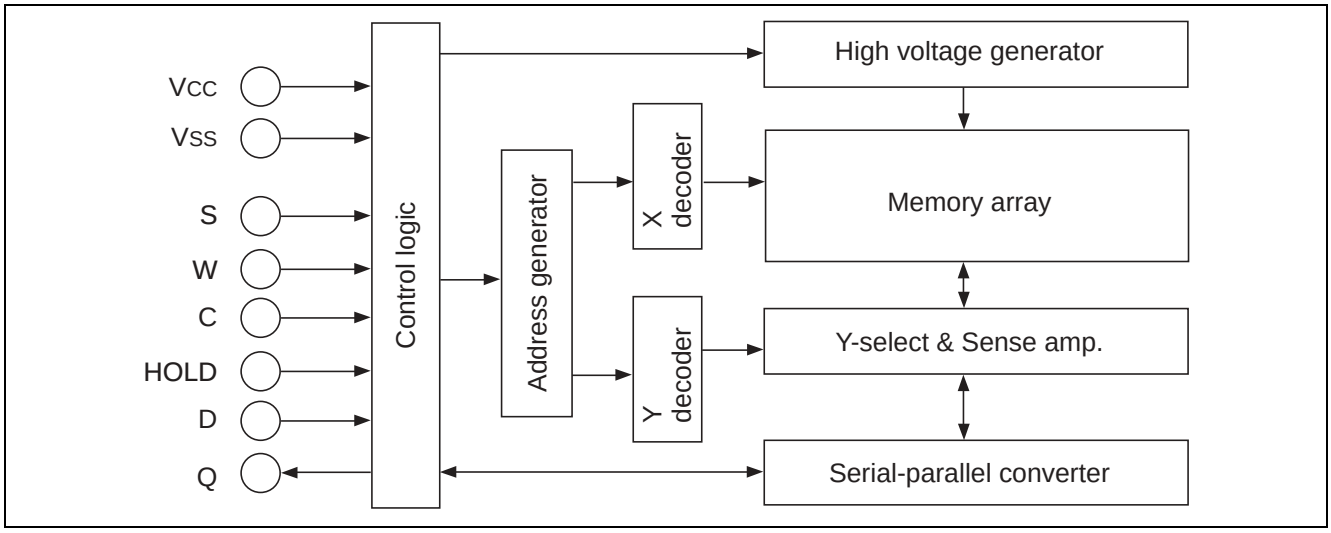
Pin Arrangement



Pin Description

Pin name	Function
C	Serial clock
D	Serial data input
Q	Serial data output
S	Chip select
W	Write protect
HOLD	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.6 to + 7.0	V
Input voltage relative to V_{SS}	V_{IN}	–0.5*[2] to +7.0*[3]	V
Operating temperature range*[1]	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Including electrical characteristics and data retention.
2. V_{IN} (min): –3.0 V for pulse width ≤ 50 ns.
3. Should not exceed V_{CC} + 1.0 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.8	—	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	$V_{CC} \times 0.7$	—	$V_{CC} + 0.5$*[2]	V
	V_{IL}	–0.3*[1]	—	$V_{CC} \times 0.3$	V
Operating temperature range	Topr	–40	—	+85	°C

Notes: 1. V_{IN} (min): –1.0 V for pulse width ≤ 50 ns.
2. V_{IN} (max): V_{CC} + 1.0 V for pulse width ≤ 50 ns.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance (D,C, S, W ,HOLD)	Cin*[1]	—	—	6.0	pF	Vin = 0 V
Output capacitance (Q)	$C_{I/O}$*[1]	—	—	8.0	pF	Vout = 0 V

Note: 1. Not 100% tested.

Memory cell characteristics (V_{CC} = 1.8 V to 5.5 V)

	Ta=25°C	Ta=85°C	Notes
Endurance	1,000k Cycles min.	100k Cycles min	1
Data retention	100 Years min.	10 Years min.	1

Notes: 1. Not 100% tested

DC Characteristics

Parameter		Symbol	Min	Max	Unit	Test conditions
Input leakage current		I_{LI}	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 to 5.5 V (S, D, C, HOLD, W)
Output leakage current		I_{LO}	—	2	µA	V_{CC} = 5.5 V, V_{OUT} = 0 to 5.5 V (Q)
V_{CC} current	Standby	I_{SB}	—	2	µA	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V
	Active	I_{CC1}	—	2	mA	V_{CC} = 3.6 V, Read at 5 MHz V_{IN} = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Q = OPEN
			—	3	mA	V_{CC} = 5.5 V, Read at 5 MHz V_{IN} = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Q = OPEN
		I_{CC2}	—	2	mA	V_{CC} = 3.6 V, Write at 5 MHz V_{IN} = $V_{CC} \times 0.1/V_{CC} \times 0.9$
			—	3.5	mA	V_{CC} = 5.5 V, Write at 5 MHz V_{IN} = $V_{CC} \times 0.1/V_{CC} \times 0.9$
Output voltage		V_{OL1}	—	0.4	V	V_{CC} = 5.5 V, I_{OL} = 2 mA
		V_{OL2}	—	0.4	V	V_{CC} = 2.5 V, I_{OL} = 1.5 mA
		V_{OH1}	$V_{CC} \times 0.8$	—	V	V_{CC} = 5.5 V, I_{OH} = –2 mA
		V_{OH2}	$V_{CC} \times 0.8$	—	V	V_{CC} = 2.5 V, I_{OH} = –0.4 mA

AC Characteristics

Test Conditions

- Input pules levels:
  - $V_{IL} = V_{CC} \times 0.2$
  - $V_{IH} = V_{CC} \times 0.8$
- Input rise and fall time: ≤ 10 ns
- Input and output timing reference levels: $V_{CC} \times 0.3$, $V_{CC} \times 0.7$
- Output reference levels: $V_{CC} \times 0.5$
- Output load: 100 pF

(Ta = –40 to +85°C, V_{CC} = 2.5 V to 5.5 V)

Parameter	Symbol	Alt	Min	Max	Unit	Notes
Clock frequency	f_C	f_{SCK}	—	5	MHz	
S active setup time	t_{SLCH}	t_{CSS1}	90	—	ns	
S not active setup time	t_{SHCH}	t_{CSS2}	90	—	ns	
S deselect time	t_{SHSL}	t_{CS}	90	—	ns	
S active hold time	t_{CHSH}	t_{CSH}	90	—	ns	
S not active hold time	t_{CHSL}	—	90	—	ns	
Clock high time	t_{CH}	t_{CLH}	90	—	ns	1
Clock low time	t_{CL}	t_{CLL}	90	—	ns	1
Clock rise time	t_{CLCH}	t_{RC}	—	1	µs	2
Clock fall time	t_{CHCL}	t_{FC}	—	1	µs	2
Data in setup time	t_{DVCH}	t_{DSU}	20	—	ns	
Data in hold time	t_{CHDX}	t_{DH}	30	—	ns	
Clock low hold time after HOLD not active	t_{HHCH}	—	70	—	ns	
Clock low hold time after HOLD active	t_{HLCH}	—	40	—	ns	
Clock high setup time before HOLD active	t_{CHHL}	—	60	—	ns	
Clock high setup time before HOLD not active	t_{CHHH}	—	60	—	ns	
Output disable time	t_{SHQZ}	t_{DIS}	—	100	ns	2
Clock low to output valid	t_{CLQV}	t_V	—	70	ns	
Output hold time	t_{CLQX}	t_{HO}	0	—	ns	
Output rise time	t_{QLQH}	t_{RO}	—	50	ns	2
Output fall time	t_{QHQL}	t_{FO}	—	50	ns	2
HOLD high to output low-Z	t_{HHQX}	t_{LZ}	—	50	ns	2
HOLD low to output high-Z	t_{HLQZ}	t_{HZ}	—	100	ns	2
Write time	t_W	t_{WC}	—	5	ms	

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$
2. Not 100% tested.

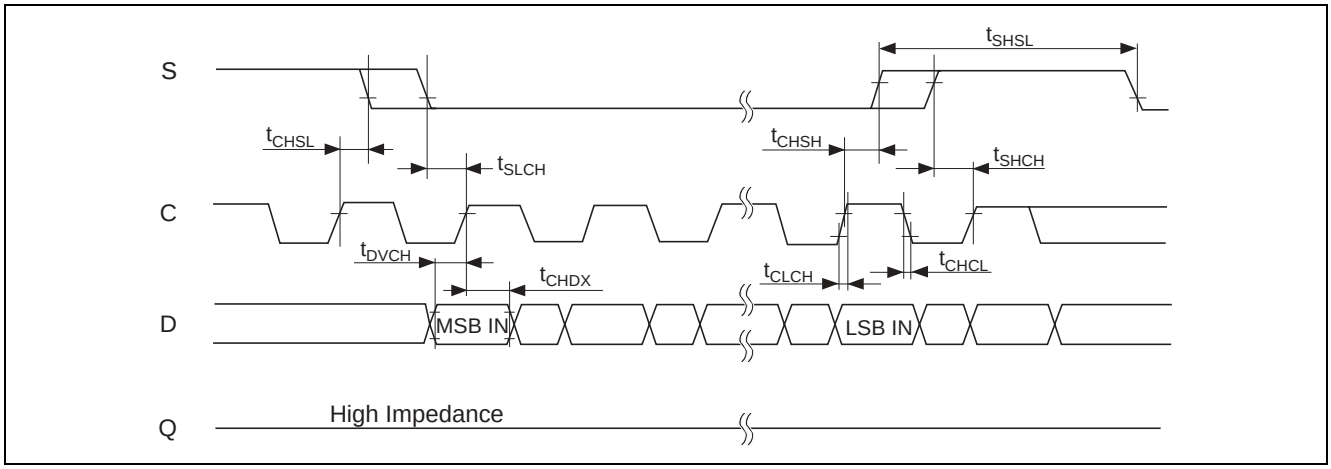
(Ta = –40 to +85°C, V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Alt	Min	Max	Unit	Notes
Clock frequency	f_C	f_{SCK}	—	3	MHz	
S active setup time	t_{SLCH}	t_{CSS1}	100	—	ns	
S not active setup time	t_{SHCH}	t_{CSS2}	100	—	ns	
S deselect time	t_{SHSL}	t_{CS}	150	—	ns	
S active hold time	t_{CHSH}	t_{CSH}	100	—	ns	
S not active hold time	t_{CHSL}	—	100	—	ns	
Clock high time	t_{CH}	t_{CLH}	150	—	ns	1
Clock low time	t_{CL}	t_{CLL}	150	—	ns	1
Clock rise time	t_{CLCH}	t_{RC}	—	1	µs	2
Clock fall time	t_{CHCL}	t_{FC}	—	1	µs	2
Data in setup time	t_{DVCH}	t_{DSU}	30	—	ns	
Data in hold time	t_{CHDX}	t_{DH}	50	—	ns	
Clock low hold time after HOLD not active	t_{HHCH}	—	140	—	ns	
Clock low hold time after HOLD active	t_{HLCH}	—	90	—	ns	
Clock high setup time before HOLD active	t_{CHHL}	—	120	—	ns	
Clock high setup time before HOLD not active	t_{CHHH}	—	120	—	ns	
Output disable time	t_{SHQZ}	t_{DIS}	—	200	ns	2
Clock low to output valid	t_{CLQV}	t_V	—	120	ns	
Output hold time	t_{CLQX}	t_{HO}	0	—	ns	
Output rise time	t_{QLQH}	t_{RO}	—	100	ns	2
Output fall time	t_{QHQL}	t_{FO}	—	100	ns	2
HOLD high to output low-Z	t_{HHQX}	t_{LZ}	—	100	ns	2
HOLD low to output high-Z	t_{HLQZ}	t_{HZ}	—	100	ns	2
Write time	t_W	t_{WC}	—	5	ms	

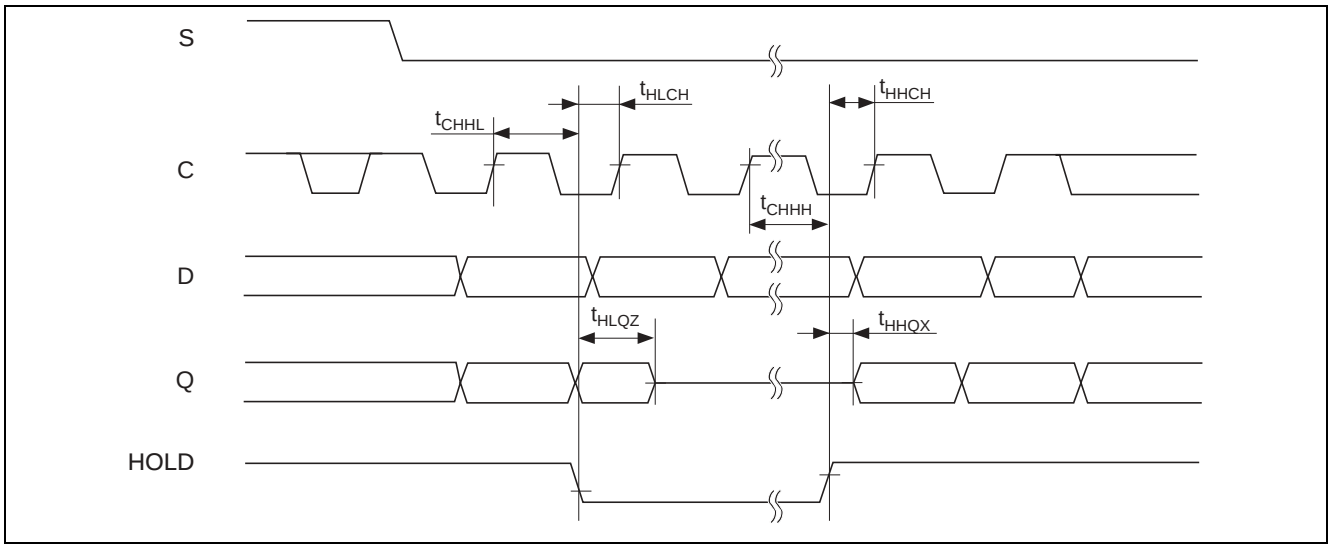
Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$
2. Not 100% tested.

Timing Waveforms

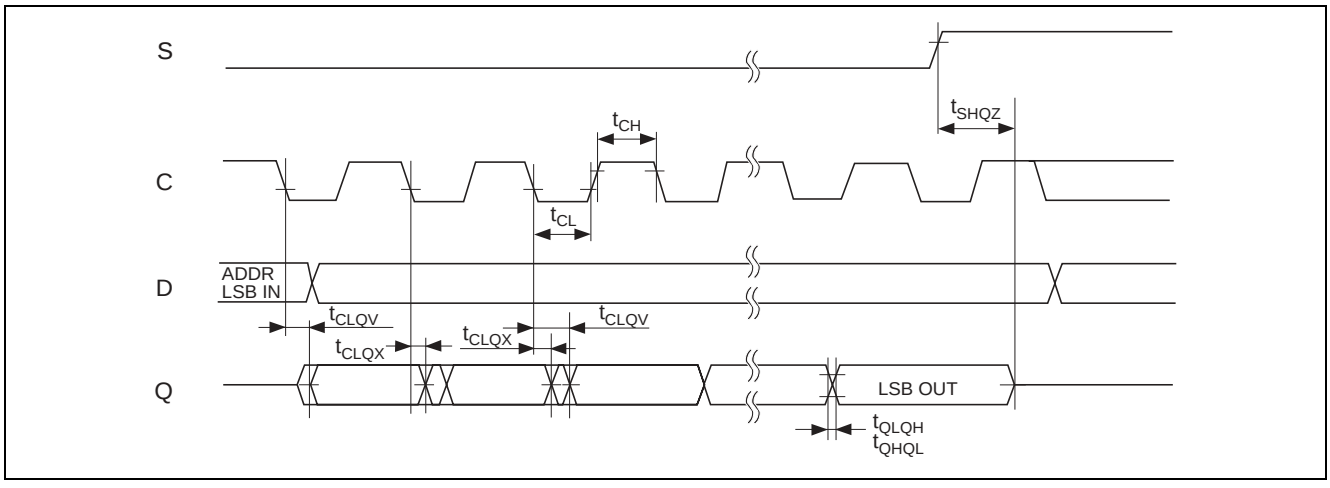
Serial Input Timing



Hold Timing



Output Timing



Pin Function

Serial data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (C).

Serial data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of serial clock (C).

Serial clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of serial clock (C). Data on serial data output (Q) changes after the falling edge of serial clock (C).

Chip select (S)

When this input signal is high, the device is deselected and serial data output (Q) is at high impedance. Unless an internal write cycle is in progress, the device will be in the standby mode. Driving chip select (S) low enables the device, placing it in the active power mode. After power-up, a falling edge on chip select (S) is required prior to the start of any instruction.

Hold (HOLD)

The hold (HOLD) signal is used to pause any serial communications with the device without deselecting the device. During the hold condition, the serial data output (Q) is high impedance, and serial data input (D) and serial clock (C) are don't care. To start the hold condition, the device must be selected, with chip select (S) driven low.

Write protect (W)

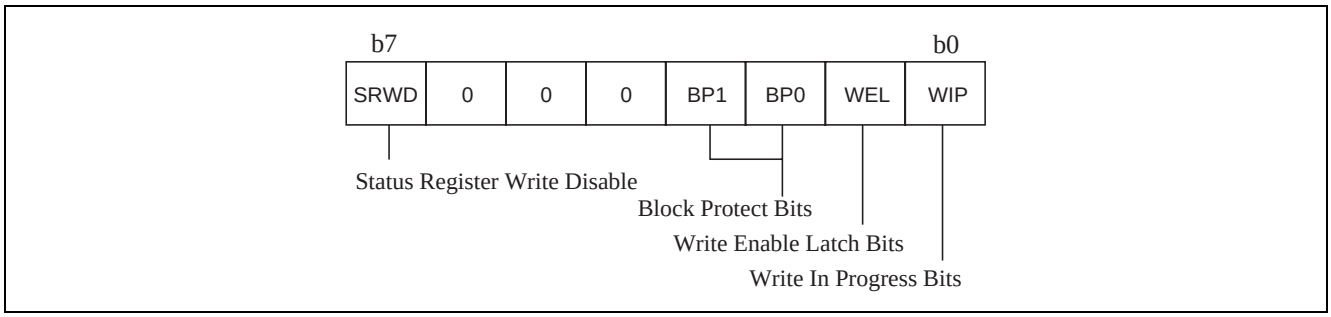
The main purpose of this input signal is to freeze the size of the area of memory that is protected against write instructions (as specified by the values in the BP1 and BP0 bits of the status register). This pin must be driven either high or low, and must be stable during all write operations.

Functional Description

Status Register

The following figure shows the Status Register Format. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

Status Register Format



WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP1, BP0 bits: The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions.

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjunction with the write protect (W) signal. The Status Register Write Disable (SRWD) bit and write protect (W) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits.

Instructions

Each instruction starts with a single-byte code, as summarized in the following table. If an invalid instruction is sent (one not contained in the following table), the device automatically deselects itself.

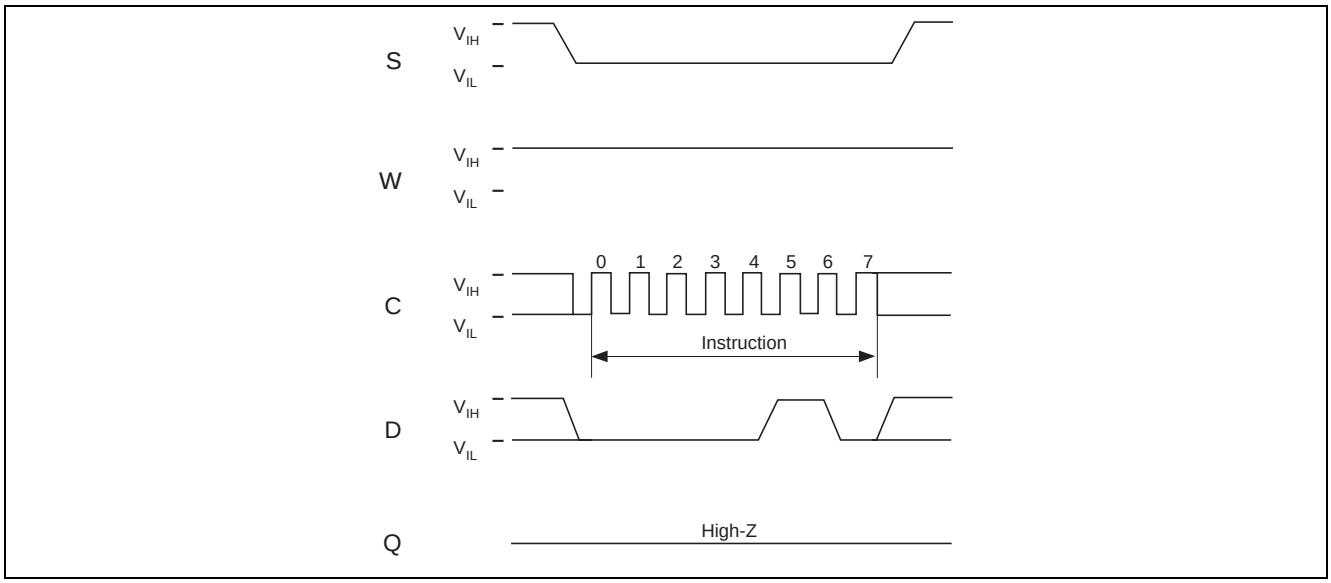
Instruction Set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Write Enable (WREN):

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device. As shown in the following figure, to send this instruction to the device, chip select (S) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D). The device then enters a wait state. It waits for the device to be deselected, by chip select (S) being driven high.

Write Enable (WREN) Sequence



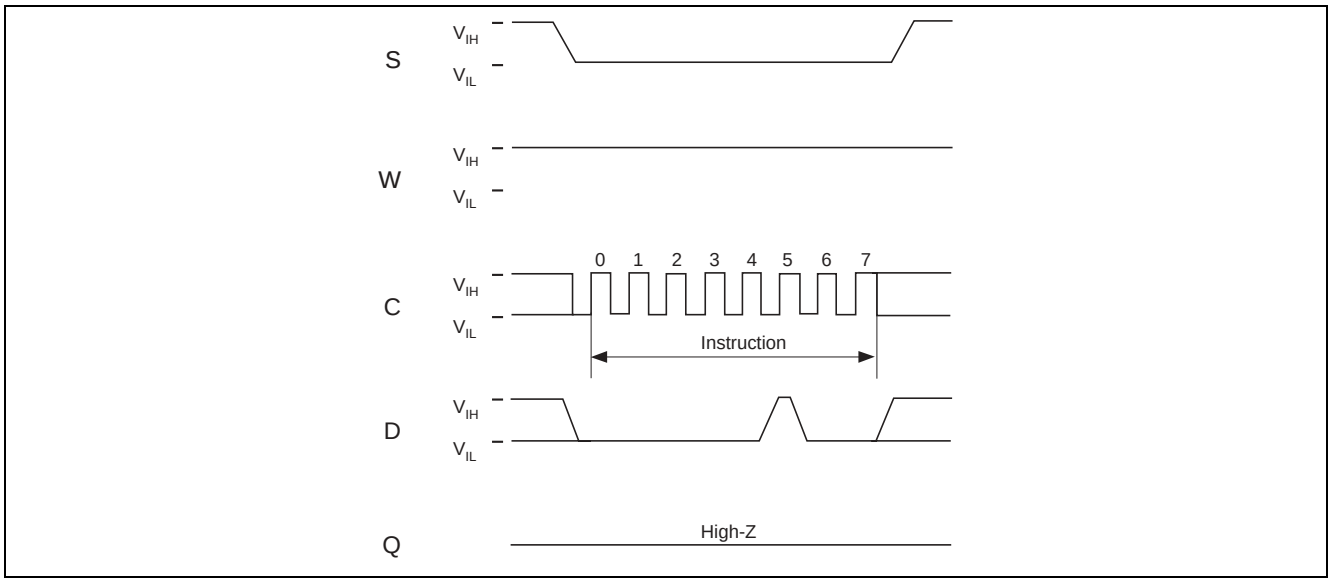
Write Disable (WRDI):

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device. As shown in the following figure, to send this instruction to the device, chip select (S) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D).

The device then enters a wait state. It waits for the device to be deselected, by chip select (S) being driven high. The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion

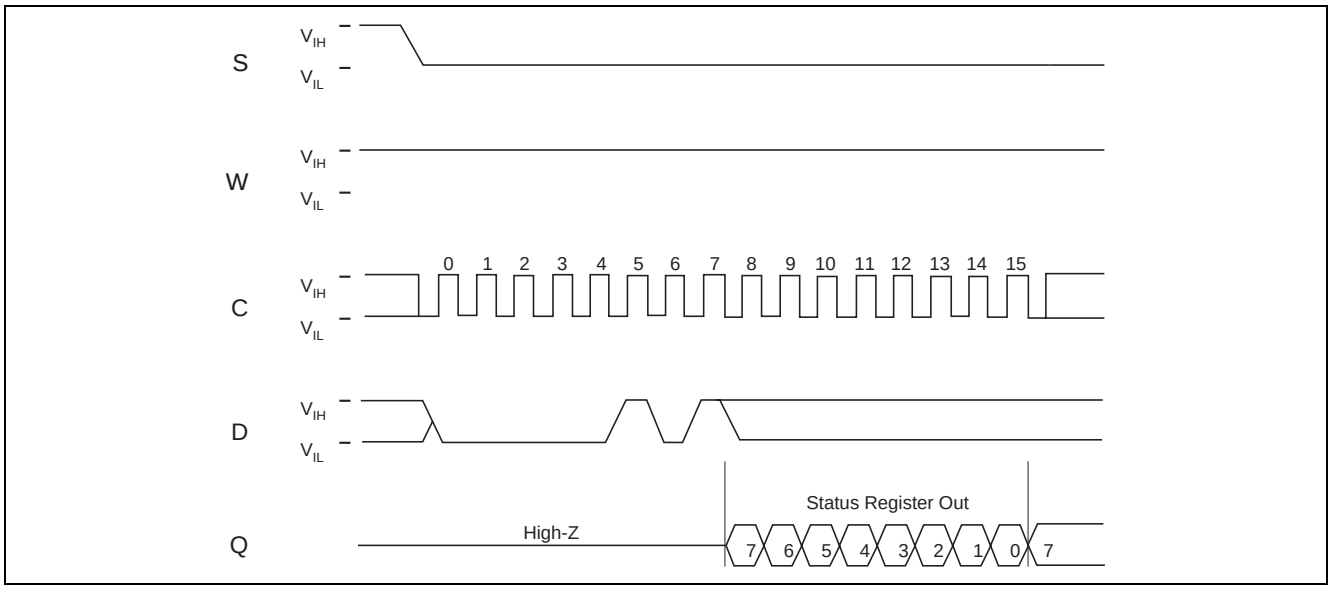
Write Disable (WRDI) Sequence



Read Status Register (RDSR):

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in the following figure.

Read Status Register (RDSR) Sequence



The status and control bits of the Status Register are as follows:

WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress. When reset to 0, no such cycles are in progress.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset and no Write or Write Status Register instructions are accepted.

BP1, BP0 bits: The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits are set to 1, the relevant memory area (as defined in the Status Register Format table) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjunction with the write protect (W) signal. The Status Register Write Disable (SRWD) bit and write protect (W) signal allows the device to be put in the Hardware Protected mode (When the Status Register Write Disable (SRWD) bit is set to 1, and write protect (W) signal is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

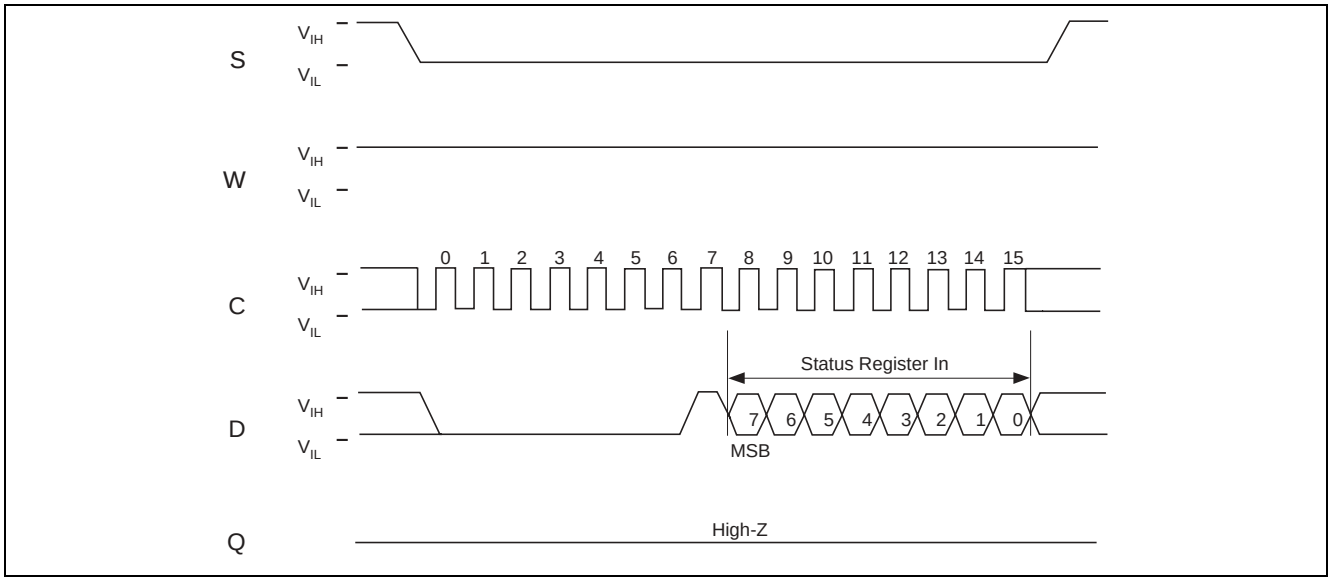
Write Status Register (WRSR):

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch(WEL). The instruction sequence is shown in the following figure. The Write Status Register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read as 0. Chip select (S) must be driven high after the rising edge of serial clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of serial clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed. As soon as chip select (S) is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, Write Enable Latch (WEL) is reset. The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in the Status Register Format table.

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the write protect (W) signal. The Status Register Write Disable (SRWD) bit and write protect (W) signal allows the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The contents of the Status Register Write Disable (SRWD) and Block Protect (BP1, BP0) bits are frozen at their current values just before the start of the execution of the Write Status Register (WRSR) instruction. The new, updated values take effect at the moment of completion of the execution of Write Status Register (WRSR) instruction.

Write Status Register (WRSR) Sequence



Read from Memory Array (READ):

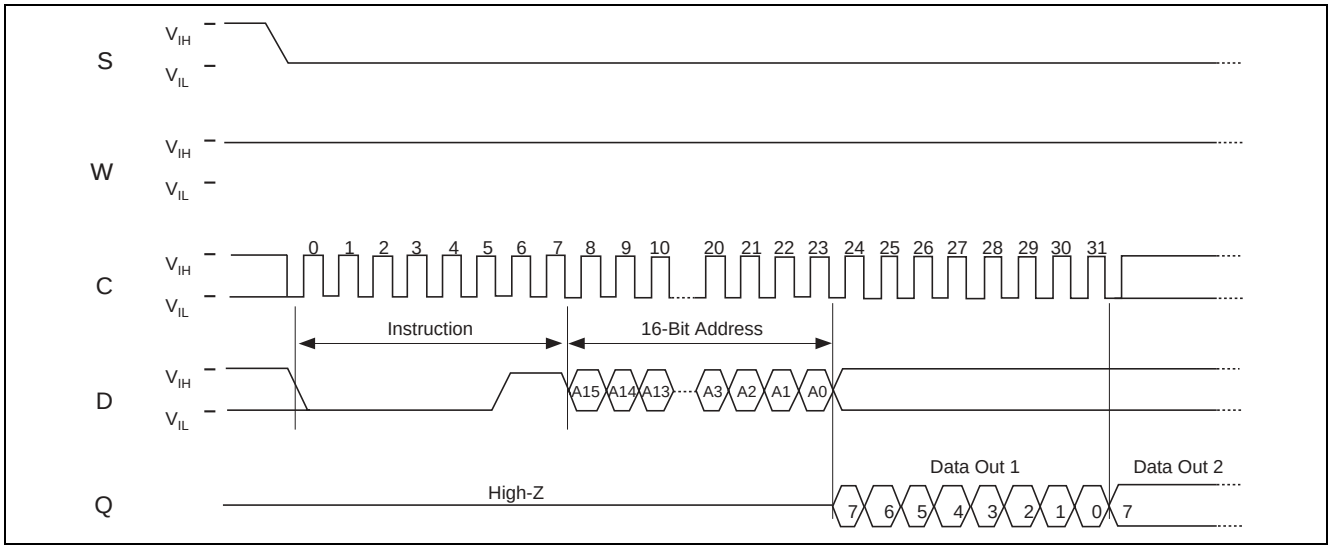
As shown in the following figure, to send this instruction to the device, chip select (S) is first driven low. The bits of the instruction byte and the address bytes are then shifted in, on serial data input (D). The addresses are loaded into an internal address register, and the byte of data at that address is shifted out, on serial data output (Q).

If chip select (S) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving chip select (S) high. The rising edge of the chip select (S) signal can occur at any time during the cycle. The addressed first byte can be any byte within any page. The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Read from Memory Array (READ) Sequence



Note: 1. Depending on the memory size, as shown in the following table, the most significant address bits are don't care.

Address Range Bits

Device	R1EX25064A	R1EX25032A
Address bits	A12 to A0	A11 to A0

Notes: 1. b15-b13 are don't care on the R1EX25064A
2. b15-b12 are don't care on the R1EX25032A

Write to Memory Array (WRITE):

As shown in the following figure, to send this instruction to the device, chip select (S) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on serial data input (D).

The instruction is terminated by driving chip select (S) high at a byte boundary of the input data. In the case of the following figure, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in AC Characteristics). At the end of the cycle, the Write In Progress (WIP) bit is reset to 0.

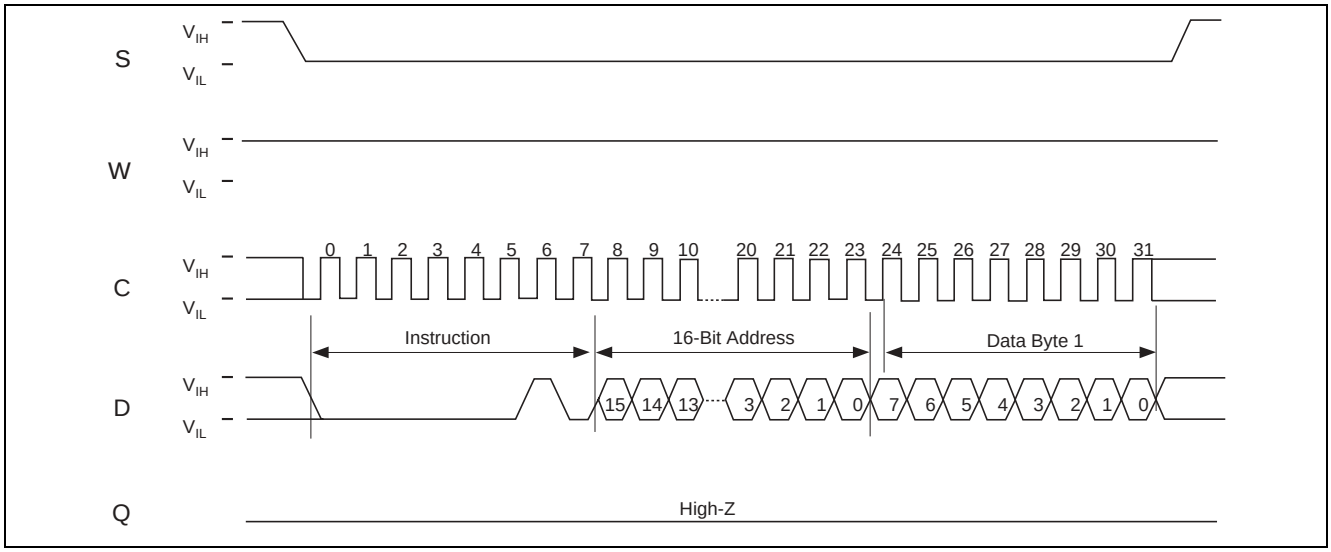
If, though, chip select (S) continues to be driven low, as shown in the following figure, the next byte of the input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these device is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

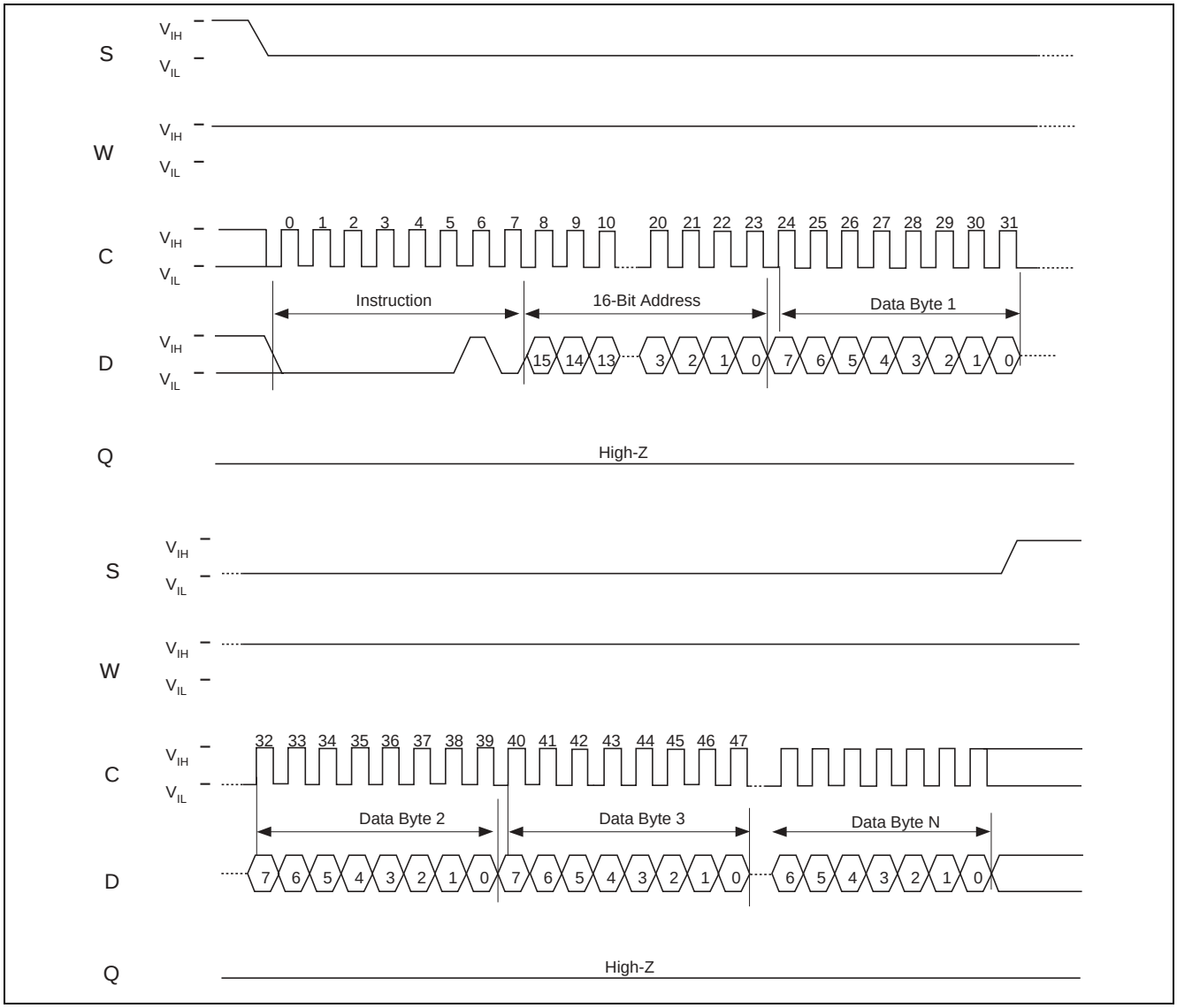
- If the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- If a Write cycle is already in progress
- If the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Byte Write (WRITE) Sequence (1 Byte)



Note: 1. Depending on the memory size, as shown in Address Range Bits table, the most significant address bits are don't care.

Byte Write (WRITE) Sequence (Page)



Note: 1. Depending on the memory size, as shown in Address Range Bits table, the most significant address bits are don't care.

Data Protect

The protection features of the device are summarized in the following table. When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless weather write protect (W) is driven high or low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of write protect (W):

- If write protect (W) is driven high, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If write protect (W) is driven low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- By setting the Status Register Write Disable (SRWD) bit after driving write protect (W) low.
- By driving write protect (W) low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull write protect (W) high.

If write protect (W) is permanently tied high, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Write Protected Block Size

Status register bits		Protected blocks	Array addresses protected	
BP1	BP0		R1EX25064A	R1EX25032A
0	0	None	None	None
0	1	Upper quarter	1800h – 1FFFh	0C00h – 0FFFh
1	0	Upper half	1000h – 1FFFh	0800h – 0FFFh
1	1	Whole memory	0000h – 1FFFh	0000h – 0FFFh

Protection Modes

W signal	SRWD bit	Mode	Write protection of the status register	Memory protect	
				Protected area*[1]	Unprotected area*[1]
1	0	Software protected (SPM)	Status register is writable (if the WREN) instruction has set the WEL bit). The values in the BP1 and BP0 bits can be changed.	Write protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status register is hardware write protected. The values in the BP1 and BP0 bits cannot be changed.	Write protected	Ready to accept Write instructions

Note: 1. As defined by the values in the Block Protected (BP1, BP0) bits of the Status Register, as shown in the former table.

Hold Condition

The hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the hold condition, the serial data output (Q) is high impedance, and serial data input (D) and serial clock (C) are don't care.

To enter the hold condition, the device must be selected, with chip select (S) low.

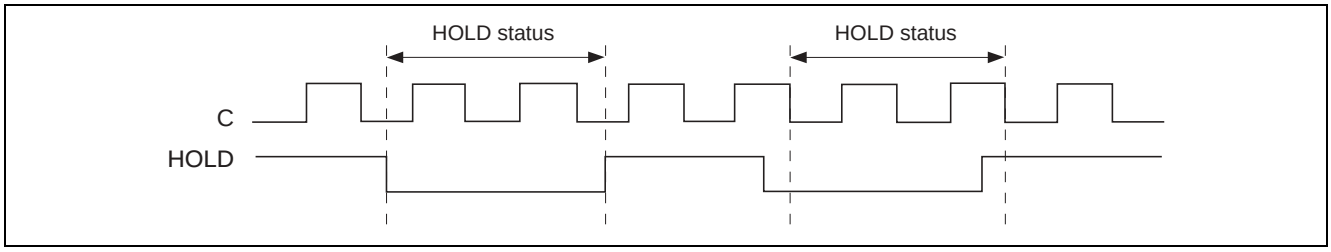
Normally, the device is kept selected, for the whole duration of the hold condition. Deselecting the device while it is in the hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The hold condition starts when the hold (HOLD) signal is driven low at the same time as serial clock (C) already being low (as shown in the following figure).

The hold condition ends when the hold (HOLD) signal is driven high at the same time as serial clock (C) already being low.

The following figure also shows what happens if the rising and falling edges are not timed to coincide with serial clock (C) being low.

Hold Condition Activation



Notes

Data Protection at V_{CC} On/Off

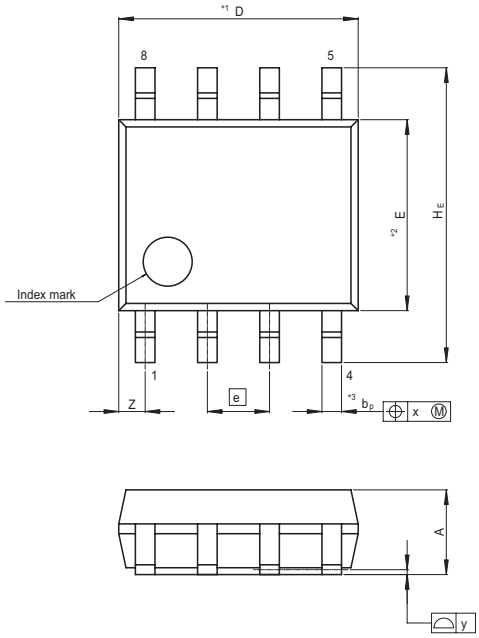
When V_{CC} is turned on or off, noise on S inputs generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to unintentional program mode. To prevent this unintentional programming, this EEPROM have a power on reset function. Be careful of the notices described below in order for the power on reset function to operate correctly.

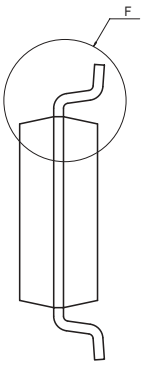
- S should be fixed to V_{CC} during V_{CC} on/off. Low to high or high to low transition during V_{CC} on/off may cause the trigger for the unintentional programming.
- V_{CC} should be turned on/off after the EEPROM is placed in a standby state.
- V_{CC} should be turned on from the ground level (V_{SS}) in order for the EEPROM not to enter the unintentional programming mode.
- V_{CC} turn on speed should be slower than 10 µs/V.
- When WRSR or WRITE instruction is executed before V_{CC} turns off, V_{CC} should be turned off after waiting write cycle time (t_W).

Package Dimensions

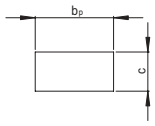
R1EX25032ASA00A/R1EX25064ASA00A (PRSP0008DF-B / Previous Code: FP-8DBV)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-3.9x4.89-1.27	PRSP0008DF-B	FP-8DBV	0.08g

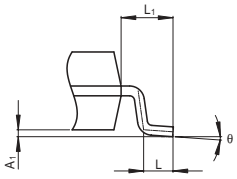




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)

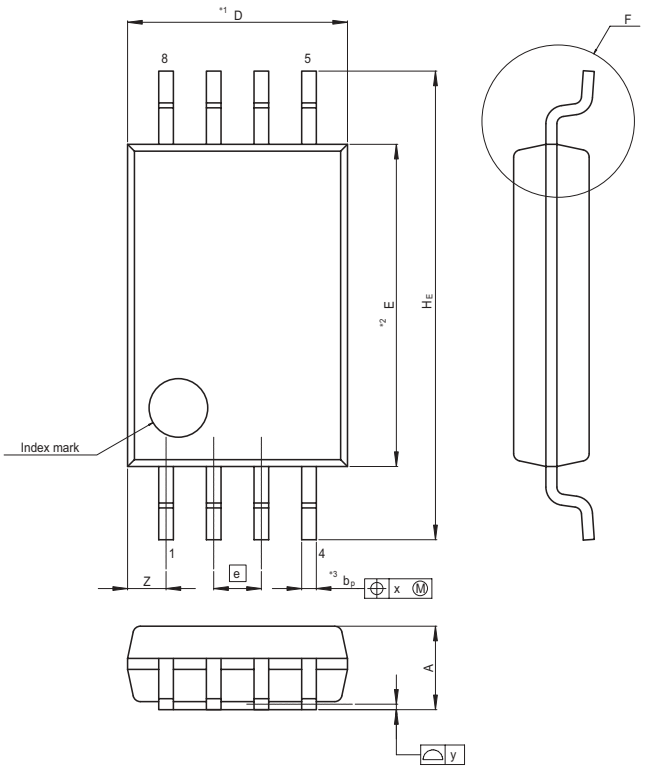


Detail F

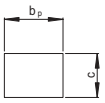
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.89	5.15
E	—	3.90	—
A_2	—	—	—
A_1	0.102	0.14	0.254
A	—	—	1.73
b_p	0.35	0.40	0.45
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.84	6.02	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
Z	—	—	0.69
L	0.406	0.60	0.889
L_1	—	1.06	—

R1EX25032ATA00A/R1EX25064ATA00A (PTSP0008JC-B / Previous Code: TTP-8DAV)

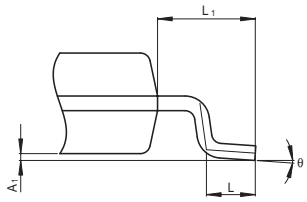
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L_1	—	1.00	—

Revision History	R1EX25032Axx00A/R1EX25064Axx00A Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Jan.25, 2008	—	Initial issue
0.02	Jan.14, 2009	P1	Features
			Endurance cycles change 10^6 cycles to 1,000k cycles @25°C.
			Data retentions years change 10 years to 100 years @25°C.
		P3	Capacitance new is described.
			Memory cell characteristics new is described.
		P4	DC characteristics
			Output voltage $V_{OH1,}$ V_{OH2} test conditions change I_{oL} to $I_{oH.}$
		P5/P6	AC characteristics
			Erase/Write endurance is deleted.
			Notes1. change Not 100% tested.
			Notes3 deleted.

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Colophon .7.2

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