



**THE DATASHEET OF
PTH08T240WAD**



10-A, 4.5-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT, ADJUSTABLE POWER

MODULE WITH TurboTrans™ POLA™

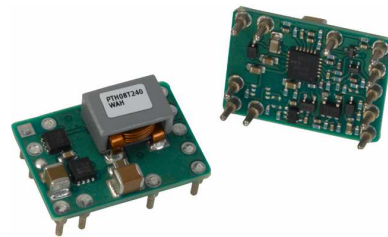
FEATURES

- Up to 10-A Output Current
- 4.5-V to 14-V Input Voltage
- Wide-Output Voltage Adjust (0.69 V to 5.5 V)
- $\pm 1.5\%$ Total Output Voltage Variation
- Efficiencies up to 96%
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Operating Temperature: -40°C to 85°C
- Safety Agency Approvals:
 - UL/IEC/CSA-C22.2 60950-1
- Prebias Startup
- On/Off Inhibit
- Differential Output Voltage Remote Sense
- Adjustable Undervoltage Lockout
- Auto-Track™ Sequencing
- Ceramic Capacitor Version (PTH08T241W)
- POLA™ Compatible

- TurboTrans™ Technology
- Designed to meet Ultra-Fast Transient Requirements up to 300 A/ μs
- SmartSync Technology

APPLICATIONS

- Complex Multi-Voltage Systems
- Microprocessors
- Bus Drivers



DESCRIPTION

The PTH08T240/241W is a high-performance 10-A rated, non-isolated power module. These modules represent the 2nd generation of the popular PTH series power modules and include a reduced footprint and additional features. The PTH08T241W is optimized to be used with all ceramic capacitors.

Operating from an input voltage range of 4.5 V to 14 V, the PTH08T240/241W requires a single resistor to set the output voltage to any value over the range, 0.69 V to 5.5 V. The wide input voltage range makes the PTH08T240/241W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V to 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V, 8-V, or 12-V intermediate bus architectures.

The module incorporates a comprehensive list of features. Output over-current and over-temperature shutdown protects against most load faults. A differential remote sense ensures tight load regulation. An adjustable under-voltage lockout allows the turn-on voltage threshold to be customized. Auto-Track™ sequencing is a popular feature that greatly simplifies the simultaneous power-up and power-down of multiple modules in a power system.

The PTH08T240/241W includes new patent pending technologies, **TurboTrans™** and **SmartSync**. The TurboTrans feature optimizes the transient response of the regulator while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification. Additionally, for a target output capacitor bank, TurboTrans can be used to significantly improve the regulators transient response by reducing the peak voltage deviation. SmartSync allows for switching frequency synchronization of multiple modules, thus simplifying EMI noise suppression tasks and reducing input capacitor RMS current requirements. The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include through-hole and surface mount configurations that are Pb - free and RoHS compatible.



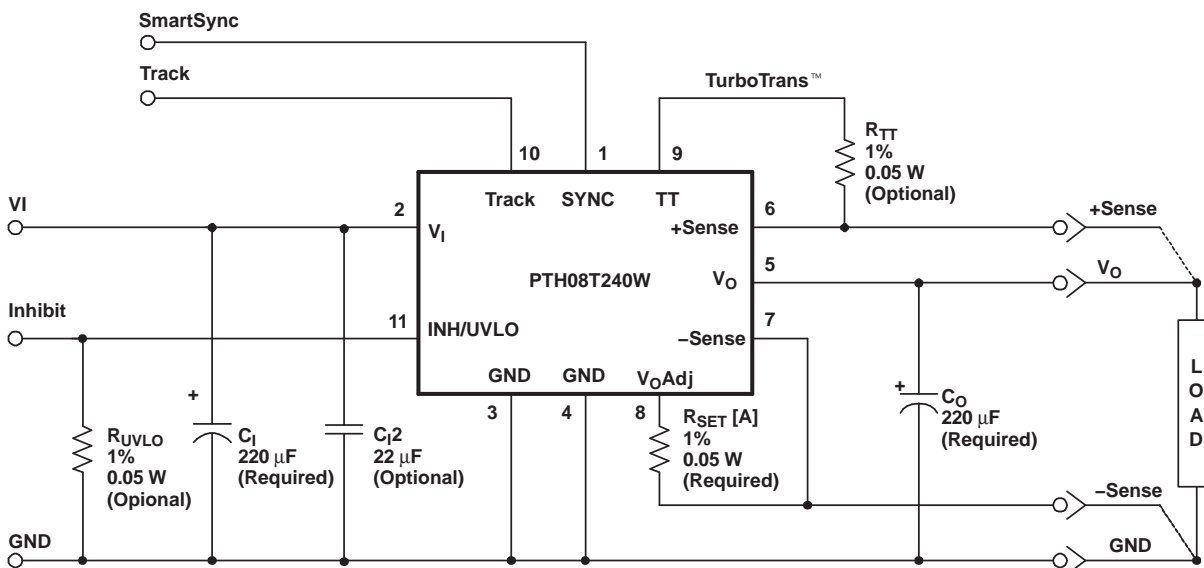
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

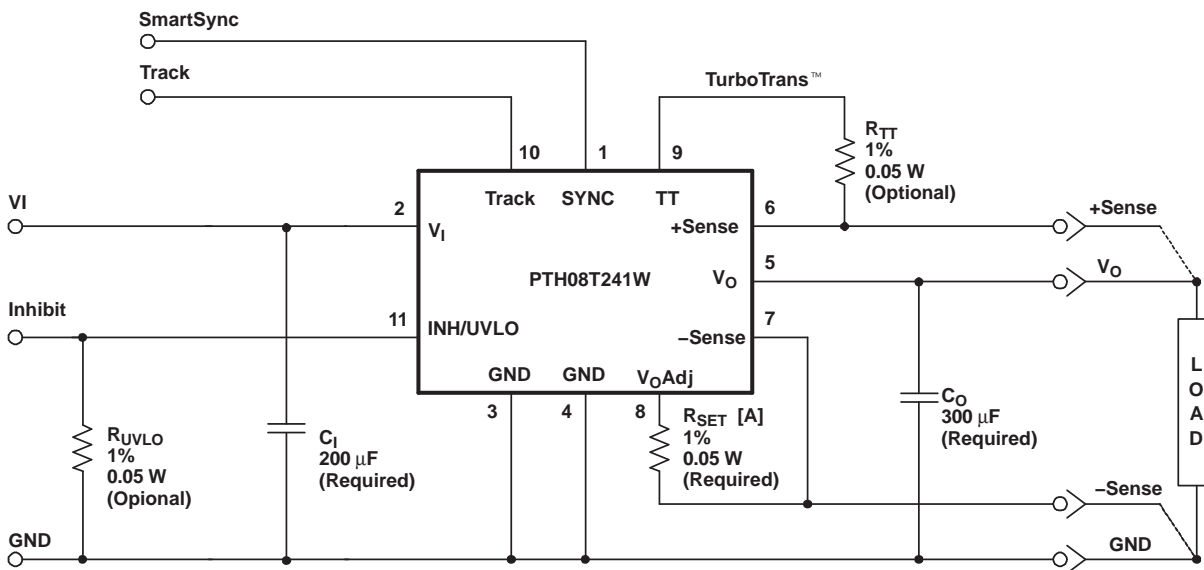
PTH08T240W



UDG–06005

A. R_{SET} required to set the output voltage to a value higher than 0.69 V. See *Electrical Characteristics* table.

PTH08T241W - Ceramic Capacitor Version



UDG–06005

A. R_{SET} required to set the output voltage to a value higher than 0.69 V. See *Electrical Characteristics* table.

B. 200 μF of ceramic or 220 μF of electrolytic input capacitance is required for proper operation.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

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ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT	
V_{Track}	Track pin voltage		-0.3 to $V_I + 0.3$	V	
T_A	Operating temperature range	Over V_I range	-40 to 85	°C	
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins for 5 seconds maximum.	suffix AH		260
			suffix AD		
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	suffix AS		235 ⁽¹⁾
			suffix AZ		260 ⁽¹⁾
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package	-55 to 125		
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature	45		
	Mechanical shock	Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 sine, mounted	suffix AH & AD	500	
			suffix AS & AZ	250	
	Mechanical vibration	Mil-STD-883D, Method 2007.2 20-2000 Hz	15	G	
	Weight		5		
	Flammability	Meets UL94V-O			grams

(1) During reflow of surface mount package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS

PTH08T240W

T_A = 25°C, V_I = 5 V, V_O = 3.3 V, C_I = 220 μF, C_O = 220 μF, and I_O = I_O max (unless otherwise stated)

PARAMETER	TEST CONDITIONS	PTH08T240W			UNIT
		MIN	TYP	MAX	
I _O Output current	Over V _O range 25°C, natural convection	0		10	A
V _I Input voltage range	Over I _O range	0.69 ≤ V _O ≤ 1.2		4.5	14 ⁽¹⁾
		1.2 < V _O ≤ 3.6		4.5	14
		3.6 < V _O ≤ 5.5		V _O + 2	14
V _O ADJ Output voltage adjust range	Over I _O range	0.69		5.5	V
V _O	Set-point voltage tolerance		±0.5	±1 ⁽²⁾	%V _O
	Temperature variation	−40°C < T _A < 85°C	±0.3		%V _O
	Line regulation	Over V _I range	±3		mV
	Load regulation	Over I _O range	±2		mV
	Total output variation	Includes set-point, line, load, −40°C ≤ T _A ≤ 85°C			±1.5 ⁽²⁾
η Efficiency	I _O = 10 A	R _{SET} = 171 Ω, V _I = 8 V, V _O = 5.0 V		95%	
		R _{SET} = 1.21 kΩ, V _O = 3.3 V		94%	
		R _{SET} = 2.38 kΩ, V _O = 2.5 V		92%	
		R _{SET} = 4.78 kΩ, V _O = 1.8 V		90%	
		R _{SET} = 7.09 kΩ, V _O = 1.5 V		88%	
		R _{SET} = 12.1 kΩ, V _O = 1.2 V		87%	
		R _{SET} = 20.8 kΩ, V _O = 1.0 V		85%	
V _O Ripple (peak-to-peak)	20-MHz bandwidth		10 ⁽¹⁾		mV _{PP}
I _{LIM} Overcurrent threshold	Reset, followed by auto-recovery		20		A
t _{tr} ΔV _{tr} t _{trTT} ΔV _{trTT} Transient response	2.5 A/μs load step 50 to 100% I _O max V _O = 2.5 V	w/o TurboTrans C _O = 220 μF, TypeC	Recovery time	35	μs
		w/ TurboTrans C _O = 2000 μF, TypeC, R _{TT} = 0 Ω	V _O over/undershoot	165	mV
			Recovery time	130	μs
		V _O over/undershoot	30	mV	
I _{IL} Track input current (pin 10)	Pin to GND			−130 ⁽³⁾	μA
dV _{track} /dt Track slew rate capability	C _O ≤ C _O (max)			1	V/ms
UVLO _{ADJ} Adjustable Under-voltage lockout (pin 11)	V _I increasing, R _{UVLO} = OPEN		4.3	4.45	V
	V _I decreasing, R _{UVLO} = OPEN		3.7	4.2	
	Hysteresis, R _{UVLO} ≤ 52.3 kΩ		0.5		
Inhibit control (pin 11)	Input high voltage (V _{IH})			Open ⁽⁴⁾	V
	Input low voltage (V _{IL})		−0.2	0.8	
	Input low current (I _{IL}), Pin 11 to GND		−235		
I _{in} Input standby current	Inhibit (pin 11) to GND, Track (pin 10) open		5		mA
f _s Switching frequency	Over V _I and I _O ranges, SmartSync (pin 1) to GND		300		kHz
f _{SYNC} Synchronization (SYNC) frequency		240		400	kHz
V _{SYNCH} SYNC High-Level Input Voltage		2		5.5	V
V _{SYNCL} SYNC Low-Level Input Voltage				0.8	V
t _{SYNC} SYNC Minimum Pulse Width		200			nSec

- (1) For output voltages ≤ 1.2 V, at nominal operating frequency, the output ripple may increase (typically 2x) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature to adjust the switching frequency, see the SmartSync Considerations section of the datasheet for further guidance.
- (2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/C or better temperature stability.
- (3) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 10. The open-circuit voltage is less than 8 V_{dc}.
- (4) This control pin has an internal pull-up. Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the related application information section.

ELECTRICAL CHARACTERISTICS (continued)
PTH08T240W
 $T_A = 25^\circ\text{C}$, $V_I = 5\text{ V}$, $V_O = 3.3\text{ V}$, $C_I = 220\ \mu\text{F}$, $C_O = 220\ \mu\text{F}$, and $I_O = I_O\ \text{max}$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		PTH08T240W			UNIT
			MIN	TYP	MAX	
C_I External input capacitance	Nonceramic		220 ⁽⁵⁾			μF
	Ceramic		22 ⁽⁵⁾			
C_O External output capacitance	w/o TurboTrans	Capacitance Value	Nonceramic	220 ⁽⁶⁾	5000 ⁽⁷⁾	μF
			Ceramic		500	
		Equivalent series resistance (non-ceramic)		7		$\text{m}\Omega$
	w/ TurboTrans	Capacitance Value	see table ⁽⁶⁾ ⁽⁸⁾			μF
Capacitance \times ESR product ($C_O \times \text{ESR}$)		1000	10000 ⁽⁸⁾		$\mu\text{F}\times\text{m}\Omega$	
MTBF Reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign		6.1			$10^6\ \text{Hr}$

- (5) A 220 μF electrolytic input capacitor is required for proper operation. The electrolytic capacitor must be rated for a minimum of 500 mA rms of ripple current.
- (6) For $V_O \leq 3.45\text{V}$, a 220 μF external output capacitor is required for basic operation. When $V_O > 3.45\text{V}$ the minimum output capacitance increase to 330 μF . The minimum output capacitance requirement increases when *TurboTrans*TM (TT) technology is utilized. See related Application Information for more guidance.
- (7) This is the calculated maximum disregarding *TurboTrans*TM technology. When the *TurboTrans*TM feature is utilized, the minimum output capacitance must be increased.
- (8) When using *TurboTrans*TM technology, a minimum value of output capacitance is required for proper operation. Additionally, low ESR capacitors are required for proper operation. See the application notes for further guidance.

ELECTRICAL CHARACTERISTICS

PTH08T241W (Ceramic Capacitors)

$T_A = 25^\circ\text{C}$, $V_I = 5\text{ V}$, $V_O = 3.3\text{ V}$, $C_I = 200\ \mu\text{F}$ ceramic, $C_O = 300\ \mu\text{F}$ ceramic, and $I_O = I_O\ \text{max}$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		PTH08T241W			UNIT
			MIN	TYP	MAX	
I_O Output current	Over V_O range	25°C, natural convection	0		10	A
V_I Input voltage range	Over I_O range	$0.69 \leq V_O \leq 1.2$	4.5		14 ⁽¹⁾	V
		$1.2 < V_O \leq 3.6$	4.5		14	
		$3.6 < V_O \leq 5.5$	$V_O + 2$		14	
$V_{O\text{ADJ}}$ Output voltage adjust range	Over I_O range		0.69		5.5	V
V_O	Set-point voltage tolerance			± 0.5	± 1 ⁽²⁾	$\%V_O$
	Temperature variation	$-40^\circ\text{C} < T_A < 85^\circ\text{C}$		± 0.3		$\%V_O$
	Line regulation	Over V_I range		± 3		mV
	Load regulation	Over I_O range		± 2		mV
	Total output variation	Includes set-point, line, load, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$				± 1.5 ⁽²⁾
η Efficiency	$I_O = 10\text{ A}$	$R_{\text{SET}} = 171\ \Omega$, $V_I = 8\text{ V}$, $V_O = 5.0\text{ V}$			95%	
		$R_{\text{SET}} = 1.21\ \text{k}\Omega$, $V_O = 3.3\text{ V}$			94%	
		$R_{\text{SET}} = 2.38\ \text{k}\Omega$, $V_O = 2.5\text{ V}$			92%	
		$R_{\text{SET}} = 4.78\ \text{k}\Omega$, $V_O = 1.8\text{ V}$			90%	
		$R_{\text{SET}} = 7.09\ \text{k}\Omega$, $V_O = 1.5\text{ V}$			88%	
		$R_{\text{SET}} = 12.1\ \text{k}\Omega$, $V_O = 1.2\text{ V}$			87%	
		$R_{\text{SET}} = 20.8\ \text{k}\Omega$, $V_O = 1.0\text{ V}$			85%	
V_O Ripple (peak-to-peak)	20-MHz bandwidth		10 ⁽¹⁾			mV _{PP}
I_{LIM} Overcurrent threshold	Reset, followed by auto-recovery		20			A
t_{tr} ΔV_{tr} t_{rTT} ΔV_{rTT} Transient response	2.5 A/ μs load step 50 to 100% $I_{O\text{max}}$ $V_O = 2.5\text{ V}$	w/o TurboTrans $C_O = 200\ \mu\text{F}$, TypeA	Recovery time	35		μs
		w/ TurboTrans $C_O = 1500\ \mu\text{F}$, TypeA $R_{\text{TT}} = \text{short}$	V_O over/undershoot	165		mV
			Recovery time	130		μs
		V_O over/undershoot	30		mV	
I_{IL} Track input current (pin 10)	Pin to GND				-130 ⁽³⁾	μA
dV_{track}/dt Track slew rate capability	$C_O \leq C_O\ (\text{max})$				1	V/ms
$UVLO_{\text{ADJ}}$ Adjustable Under-voltage lockout (pin 11)	V_I increasing, $R_{\text{UVLO}} = \text{OPEN}$		4.3		4.45	V
	V_I decreasing, $R_{\text{UVLO}} = \text{OPEN}$		3.7		4.2	
	Hysteresis, $R_{\text{UVLO}} \leq 52.3\ \text{k}\Omega$			0.5		
Inhibit control (pin 11)	Input high voltage (V_{IH})				Open ⁽⁴⁾	V
	Input low voltage (V_{IL})		-0.2		0.8	
	Input low current (I_{IL}), Pin 11 to GND			-235		
I_{in} Input standby current	Inhibit (pin 11) to GND, Track (pin 10) open		5			mA
f_s Switching frequency	Over V_I and I_O ranges, SmartSync (pin 1) to GND		300			kHz
f_{SYNC} Synchronization (SYNC) frequency			240		400	kHz
V_{SYNCH} SYNC High-Level Input Voltage			2		5.5	V
V_{SYNCL} SYNC Low-Level Input Voltage					0.8	V
t_{SYNC} SYNC Minimum Pulse Width			200			nSec

- (1) For output voltages $\leq 1.2\text{ V}$, at nominal operating frequency, the output ripple may increase (typically 2x) when operating at input voltages greater than $(V_O \times 11)$. When using the SmartSync feature to adjust the switching frequency, see the SmartSync Considerations section of the datasheet for further guidance.
- (2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET} . The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/C or better temperature stability.
- (3) A low-leakage ($<100\ \text{nA}$), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 10. The open-circuit voltage is less than $8\ V_{\text{dc}}$.
- (4) This control pin has an internal pull-up. Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage ($<100\ \text{nA}$) MOSFET is recommended for control. For additional information, see the related application note.

ELECTRICAL CHARACTERISTICS (continued)
PTH08T241W (Ceramic Capacitors)
 $T_A = 25^\circ\text{C}$, $V_I = 5\text{ V}$, $V_O = 3.3\text{ V}$, $C_I = 200\ \mu\text{F}$ ceramic, $C_O = 300\ \mu\text{F}$ ceramic, and $I_O = I_O\ \text{max}$ (unless otherwise stated)

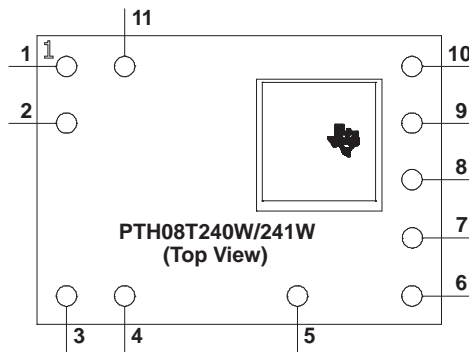
PARAMETER	TEST CONDITIONS		PTH08T241W			UNIT
			MIN	TYP	MAX	
C_I External input capacitance			200 ⁽⁵⁾			μF
C_O External output capacitance	w/o TurboTrans	Capacitance Value Ceramic	300 ⁽⁶⁾		3000 ⁽⁷⁾	μF
	w/ TurboTrans	Capacitance Value	see table ⁽⁶⁾		5000	μF
		Capacitance \times ESR product ($C_O \times \text{ESR}$)	100		1000	$\mu\text{F}\times\text{m}\Omega$
MTBF Reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign		6.1			$10^6\ \text{Hr}$

- (5) 200 μF of input capacitance is required for proper operation. 200 μF of ceramic or 220 μF of electrolytic input capacitance can be used. Electrolytic capacitance must be rated for a minimum of 500 mA rms of ripple current. An additional 22- μF ceramic input capacitor is recommended to reduce rms ripple current.
- (6) 300 μF of ceramic output capacitance is required for basic operation. The minimum output capacitance requirement increases when *TurboTrans™* (TT) technology is utilized. Additionally, low ESR capacitors are required for proper operation. See related Application Information for more guidance.
- (7) This is the calculated maximum disregarding *TurboTrans™* technology.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V _I	2	The positive input voltage power node to the module, which is referenced to common GND.
V _O	5	The regulated positive power output with respect to GND.
GND	3, 4	This is the common ground connection for the V _I and V _O power connections. It is also the 0 V _{dc} reference for the control inputs.
Inhibit ⁽¹⁾ and UVLO	11	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to GND (pin 3) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see the Application Information section.
V _O Adjust	8	A 0.05 W 1% resistor must be directly connected between this pin and pin7 (–Sense) to set the output voltage to a value higher than 0.69V. The temperature stability of the resistor should be 100 ppm/°C (or better). The setpoint range for the output voltage is from 0.69V to 5.5V. If left open circuit, the output voltage will default to its lowest value. For further information, on output voltage adjustment see the related application note. The specification table gives the preferred resistor values for a number of standard output voltages.
+ Sense	6	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense must be connected to V _O , very close to the load.
– Sense	7	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy –Sense must be connected to GND (pin4) very close to the module (within 10cm).
Track	10	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V _I . NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
TurboTrans™	9	This input pin adjusts the transient response of the regulator. To activate the TurboTrans™ feature, a 1%, 50mW resistor must be connected between this pin and pin 6 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by utilizing this feature. If unused, this pin must be left open-circuit. The resistance requirement can be selected from the TurboTrans™ resistor table in the Application Information section. External capacitance must never be connected to this pin unless the TurboTrans resistor value is a short, 0Ω.
SmartSync	1	This input pin synchronizes the switching frequency of the module to an external clock frequency. The SmartSync feature can be used to synchronize the switching frequency of multiple PTH08T240/241W modules, aiding EMI noise suppression efforts. If unused, this pin should be connected to GND (pin3). For more information, please review the Application Information section.

(1) Denotes negative logic: Open = Normal operation, Ground = Function active



TYPICAL CHARACTERISTICS⁽¹⁾⁽²⁾

CHARACTERISTIC DATA ($V_I = 12\text{ V}$)

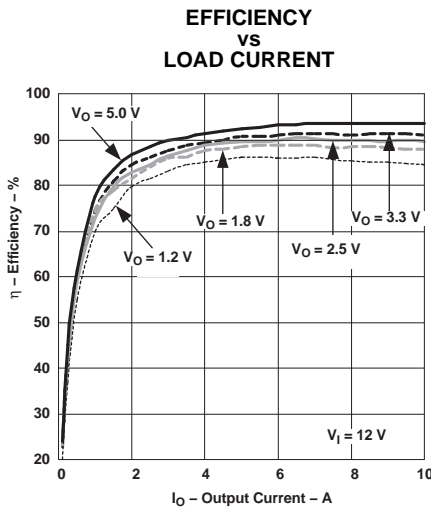


Figure 1.

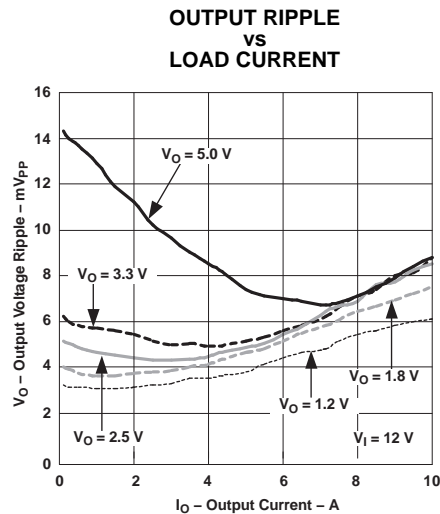


Figure 2.

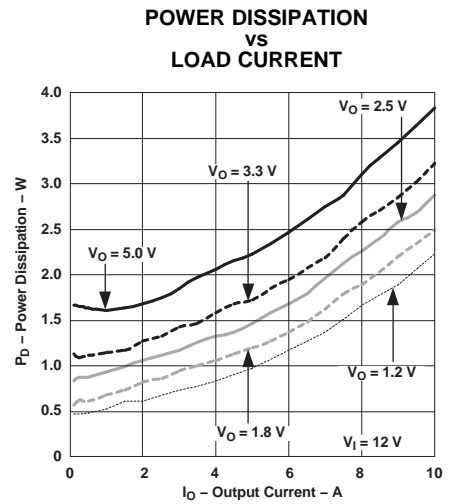


Figure 3.

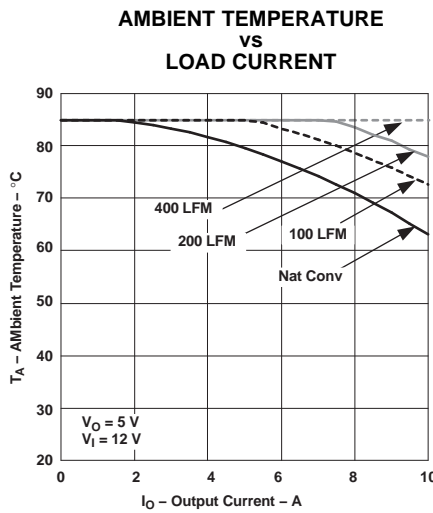


Figure 4. Safe Operating Area

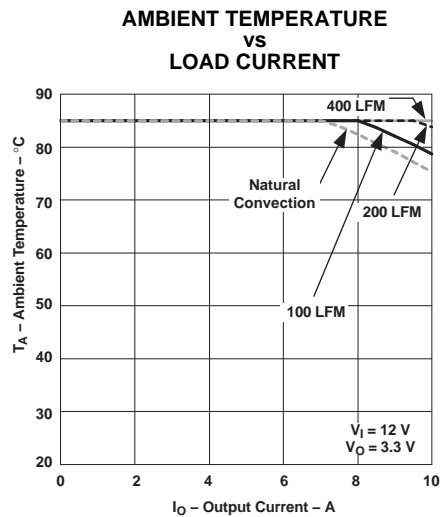


Figure 5. Safe Operating Area

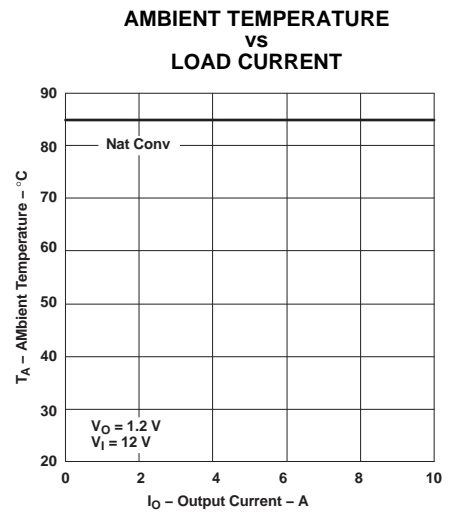


Figure 6. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 4, Figure 5, and Figure 6.

TYPICAL CHARACTERISTICS⁽¹⁾⁽²⁾

CHARACTERISTIC DATA ($V_I = 5\text{ V}$)

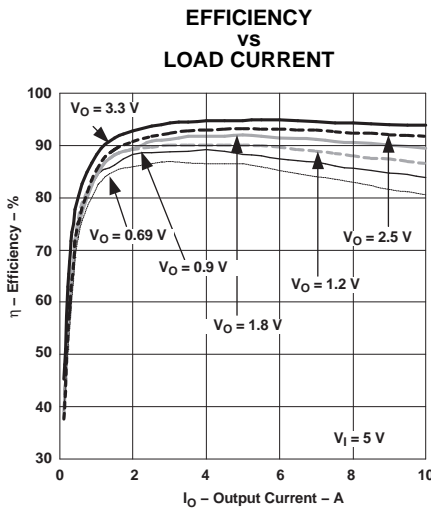


Figure 7.

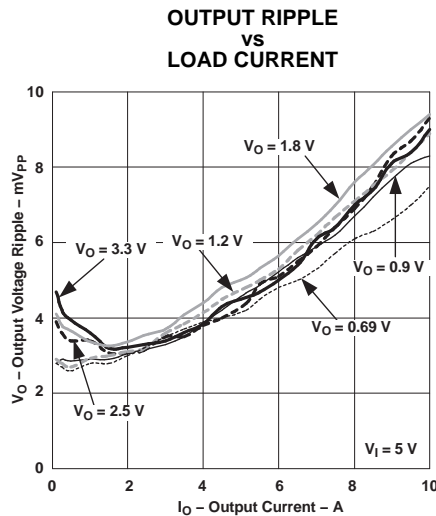


Figure 8.

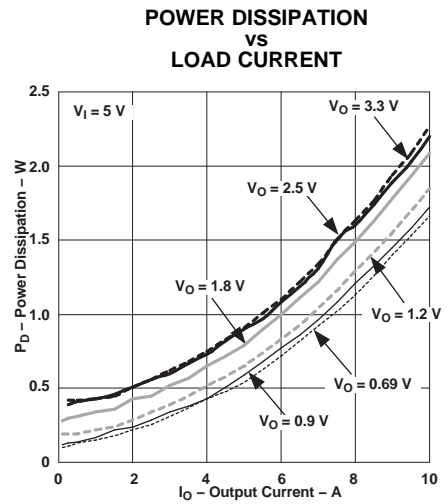


Figure 9.

AMBIENT TEMPERATURE
vs
LOAD CURRENT

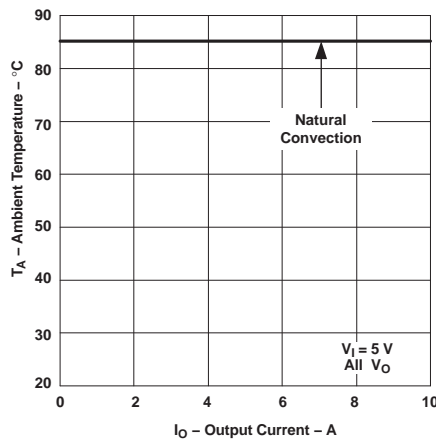


Figure 10. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25C. This data is considered typical for the converter. Applies to [Figure 7](#), [Figure 8](#), and [Figure 9](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to [Figure 10](#).

APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The V_O Adjust control (pin 8) sets the output voltage of the PTH08T240/241W. The adjustment range is 0.69 V to 5.5 V. The adjustment method requires the addition of a single external resistor, R_{SET} , that must be connected directly between the V_O Adjust and – Sense pins. Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

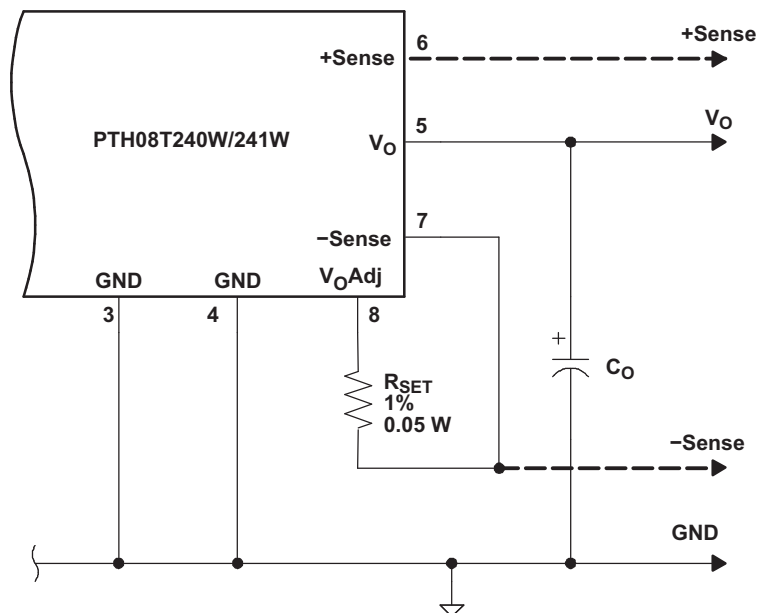
For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 11 shows the placement of the required resistor.

$$R_{SET} = 10 \text{ k}\Omega \times \frac{0.69}{V_O - 0.69} - 1.43 \text{ k}\Omega \quad (1)$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard) (V)	R_{SET} (Standard Value) (k Ω)	V_O (Actual) (V)
5.0 ⁽¹⁾	0.169	5.005
3.3	1.21	3.304
2.5	2.37	2.506
1.8	4.75	1.807
1.5	6.98	1.510
1.2 ⁽²⁾	12.1	1.200
1 ⁽²⁾	20.5	1.004
0.7 ⁽²⁾	681	0.700

- (1) For $V_O > 3.6$ V, the minimum input voltage is $(V_O + 2)$ V.
- (2) For output voltages ≤ 1.2 V, at nominal operating frequency, the output ripple may increase (typically 2x) when operating at input voltages greater than $(V_O \times 11)$. When using the SmartSync feature, review the SmartSync application section for further guidance.



- (1) R_{SET} : Use a 0.05 W resistor with a tolerance of 1% and temperature stability of 100 ppm/ $^{\circ}$ C (or better). Connect the resistor directly between pins 8 and 7, as close to the regulator as possible, using dedicated PCB traces.
- (2) Never connect capacitors from V_O Adjust to either + Sense, GND, or V_O . Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

Figure 11. V_O Adjust Resistor Placement

Table 2. Output Voltage Set-Point Resistor Values (Standard Values)

V _O Required (V)	R _{SET} (kΩ)	V _O Required (V)	R _{SET} (Ω)
0.70 ⁽¹⁾	681	2.50	2.37 k
0.75 ⁽¹⁾	113	2.60	2.15 k
0.80 ⁽¹⁾	61.9	2.70	2.00 k
0.85 ⁽¹⁾	41.2	2.80	1.82 k
0.90 ⁽¹⁾	31.6	2.90	1.69 k
0.95 ⁽¹⁾	24.9	3.00	1.54 k
1.00 ⁽¹⁾	20.5	3.10	1.43 k
1.05 ⁽¹⁾	17.8	3.20	1.33 k
1.10 ⁽¹⁾	15.4	3.30	1.21 k
1.15 ⁽¹⁾	13.3	3.40	1.10 k
1.20 ⁽¹⁾	12.1	3.50	1.02 k
1.25	10.7	3.60	931
1.30	9.88	3.70 ⁽²⁾	866
1.35	9.09	3.80 ⁽²⁾	787
1.40	8.25	3.90 ⁽²⁾	715
1.45	7.68	4.00 ⁽²⁾	649
1.50	6.98	4.10 ⁽²⁾	590
1.55	6.49	4.20 ⁽²⁾	536
1.60	6.04	4.30 ⁽²⁾	475
1.65	5.76	4.40 ⁽²⁾	432
1.70	5.36	4.50 ⁽²⁾	383
1.75	5.11	4.60 ⁽²⁾	332
1.80	4.75	4.70 ⁽²⁾	287
1.85	4.53	4.80 ⁽²⁾	249
1.90	4.22	4.90 ⁽²⁾	210
1.95	4.02	5.00 ⁽²⁾	169
2.00	3.83	5.10 ⁽²⁾	133
2.10	3.40	5.20 ⁽²⁾	100
2.20	3.09	5.30 ⁽²⁾	66.5
2.30	2.87	5.40 ⁽²⁾	34.8
2.40	2.61	5.50 ⁽²⁾	4.99

(1) For output voltages $\leq 1.2\text{V}$, at nominal operating frequency, the output ripple may increase (typically 2 \times) when operating at input voltages greater than $(V_O \times 11)$. When using the SmartSync feature, review the SmartSync application section for further guidance.

(2) For $V_O > 3.6\text{V}$, the minimum input voltage is $(V_O + 2)\text{V}$.

CAPACITOR RECOMMENDATIONS FOR THE PTH08T240/241W POWER MODULE

Capacitor Technologies

Electrolytic Capacitors

When using electrolytic capacitors, high quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or OS-CON type capacitors are required.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors may only be used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their lower ESR, higher rated surge, power dissipation, and ripple current capability. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor (Required)

The PTH08T241W requires a minimum input capacitance of 200µF of ceramic type.

The PTH08T240W requires a minimum input capacitance of 220µF electrolytic type. The ripple current rating of the electrolytic capacitor must be at least 700mA_{rms} when $V_O \geq 3V$. The ripple current rating must be at least 450mA_{rms} when $V_O < 3V$. An optional 22µF X5R/X7R ceramic is recommended to reduce the RMS ripple current.

Input Capacitor Information

The size and value of the input capacitor is determined by the converter's transient performance capability. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1.3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This will reduce the magnitude of the ripple current through the electrolytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

Increasing the minimum input capacitance to 680µF is recommended for high-performance applications, or wherever the input source performance is degraded.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of $2 \times$ (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

Output Capacitor (Required)

The PTH08T241W requires a minimum output capacitance of 300 μ F of ceramic type.

The PTH08T240W requires a minimum output capacitance of 220 μ F of aluminum, polymer-aluminum, tantulum, or polymer-tantalum type.

The required capacitance above the minimum will be determined by actual transient deviation requirements. See the TurboTrans Technology application section within this document for specific capacitance selection.

Output Capacitor Information

When selecting output capacitors, the main considerations are capacitor type, temperature stability, and ESR. When using the TurboTrans feature, the capacitance X ESR product should also be considered (see the following section).

Ceramic output capacitors added for high-frequency bypassing should be located as close as possible to the load to be effective. Ceramic capacitor values below 10 μ F should not be included when calculating the total output capacitance value.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

TurboTrans Output Capacitance

TurboTrans allows the designer to optimize the output capacitance according to the system transient design requirement. High quality, ultra-low ESR capacitors are required to maximize TurboTrans effectiveness. When using TurboTrans, the capacitor's capacitance (μ F) \times ESR (m Ω) product determines its capacitor type; Type A, B, or C. These three types are defined as follows:

Type A = (100 \leq capacitance \times ESR \leq 1000) (e.g. ceramic)

Type B = (1000 < capacitance \times ESR \leq 5000) (e.g. polymer-tantalum)

Type C = (5000 < capacitance \times ESR \leq 10,000) (e.g. OS-CON)

When using more than one type of output capacitor, select the capacitor type that makes up the majority of your total output capacitance. When calculating the C \times ESR product, use the maximum ESR value from the capacitor manufacturer's datasheet.

The PTH08T241W should be used when only Type A (ceramic) capacitors are used on the output.

Working Examples:

A capacitor with a capacitance of 330 μ F and an ESR of 5m Ω , has a C \times ESR product of 1650 μ F \times m Ω (330 μ F \times 5m Ω). This is a Type B capacitor. A capacitor with a capacitance of 1000 μ F and an ESR of 8m Ω , has a C \times ESR product of 8000 μ F \times m Ω (1000 μ F \times 8m Ω). This is a Type C capacitor.

See the TurboTrans Technology application section within this document for specific capacitance selection.

[Table 3](#) includes a preferred list of capacitors by type and vendor. See the Output Bus / TurboTrans column.

Non-TurboTrans Output Capacitance

If the TurboTrans feature is not used, minimum ESR and maximum capacitor limits must be followed. System stability may be effected and increased output capacitance may be required without TurboTrans.

When using the PTH08T240W, observe the minimum ESR of the entire output capacitor bank. The minimum ESR limit of the output capacitor bank is 7m Ω . A list of preferred low-ESR type capacitors, are identified in [Table 3](#).

When using the PTH08T241W without the TurboTrans feature, the maximum amount of capacitance is 3000 μ F of ceramic type. Large amounts of capacitance may reduce system stability.

Utilizing the TurboTrans feature improves system stability, improves transient response, and reduces the amount of output capacitance required to meet system transient design requirements.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5A/μs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with load steps greater than 100A/μs, adding multiple 10μF ceramic capacitors plus 10x1μF, and numerous high frequency ceramics (≤0.1μF) is all that is required to soften the transient higher frequency edges. The PCB location of these capacitors in relation to the load is critical. DSP, FPGA and ASIC vendors identify types, location and amount of capacitance required for optimum performance. Low impedance buses, unbroken PCB copper planes, and components located as close as possible to the high frequency devices are essential for optimizing transient performance.

Table 3. Input/Output Capacitors⁽¹⁾

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage (V)	Value (μF)	Max. ESR at 100 kHz (mΩ)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus		
							No Turbo-Trans	Turbo-Trans (Cap Type) ⁽²⁾	
Panasonic									
FC (Radial)	25	270	90	755	10 x 12,5	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	EEUFC1E271
FC (Radial)	25	560	65	1205	12,5 x 15	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	EEUFC1E561S
FC(SMD)	25	470	65	1200	12,5 x 16,5	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	EEVFC1E471LQ
FK(SMD)	25	470	80	850	10 x10,2	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	EEVFK1E471P
United Chemi-Con									
PTB(SMD) Poly-Tantalum	6.3	330	25	2600	7,3x4,3x2.8	N/R ⁽⁶⁾	1 ~ 4 ⁽⁴⁾	C ≥ 2 ⁽²⁾	4PTB337MD6TER (V _O ≤ 5.1V) ⁽⁷⁾
LXZ, Aluminum (Radial)	25	330	90	760	10 x 12,5	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	LXZ25VB331M10X12LL
PS, Poly-Alum(Radial)	16	330	14	5060	10 x 12,5	≥1 ⁽³⁾	1 ~ 3	B ≥ 2 ⁽²⁾	16PS330MJ12
PXA, Poly-Alum(SMD)	16	330	14	5050	10 x 12,2	≥1 ⁽³⁾	1 ~ 3	B ≥ 2 ⁽²⁾	PXA16VC331MJ12TP
PS, Poly-Alum(Radial)	10	270	14	4420	8 x 11,5	N/R ⁽⁶⁾	1 ~ 2	B ≥ 2 ⁽²⁾	10PS270MH11
PXA, Poly-Alum(Radial)	10	330	14	4420	8 x 12	N/R ⁽⁶⁾	1 ~ 2	B ≥ 2 ⁽²⁾	PXA10VC331MH12
Nichicon, Aluminum									
HD (Radial)	25	220	72	760	8 x 11,5	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	UHD1E221MPR
PM (Radial)	25	330	95	750	10 x 15	≥1 ⁽³⁾	≥ 1 ⁽⁴⁾	N/R ⁽⁵⁾	UPM1E331MPH6
PM (Radial)	35	560	48	1360	16 x 15	≥1 ⁽³⁾	≥ 2 ⁽⁴⁾	N/R ⁽⁵⁾	UPM1V561MHH6
Panasonic, Poly-Aluminum	2.0	390	5	4000	7,3x4,3x4,2	N/R ⁽⁶⁾	N/R ⁽⁶⁾	B ≥ 2 ⁽²⁾	EEFSE0J391R (V _O ≤ 1.6V) ⁽⁸⁾

(1) Capacitor Supplier Verification

Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products.

RoHS, Lead-free and Material Details

See the capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection

Capacitor Types:

- Type A = (100 ≤ capacitance × ESR ≤ 1000)
- Type B = (1,000 < capacitance × ESR ≤ 5,000)
- Type C = (5,000 < capacitance × ESR ≤ 10,000)

(3) In addition to the required input electrolytic capacitance, ≥ 20 μF of ceramic capacitance is required to reduce the high-frequency reflected ripple current.

(4) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 μF of ceramic capacitance.

(5) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher capacitance × ESR products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.

(6) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

(7) The voltage rating and derating of this capacitor only allows it to be used for voltages that are equal or less than 5.1 V.

(8) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.

Table 3. Input/Output Capacitors (continued)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage (V)	Value (µF)	Max. ESR at 100 kHz (mΩ)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus		
							No Turbo-Trans	Turbo-Trans (Cap Type) ⁽²⁾	
Sanyo									
TPE, Poscap (SMD)	10	330	25	3000	7,3 × 4,3	N/R ⁽⁶⁾	1 ~ 3	C ≥ 2 ⁽²⁾	10TPE330MF
TPE Poscap(SMD)	2.5	470	7	4400	7,3 × 4,3	N/R ⁽⁶⁾	1 ~ 2	B ≥ 2 ⁽²⁾	2R5TPE470M7 (V _O ≤ 1.8V) ⁽⁸⁾
TPD Poscap (SMD)	2.5	1000	5	6100	7,3 × 4,3	N/R ⁽⁶⁾	1	B ≥ 1 ⁽²⁾	2R5TPD1000M5 (V _O ≤ 1.8V) ⁽⁸⁾
SEP, OS-CON (Radial)	16	330	16	4700	10 × 13	≥ 1 ⁽³⁾	1 ~ 3	B ≥ 2 ⁽²⁾	16SEP330M
SP OS-CON (Radial)	16	270	18	4400	10 × 11,5	≥ 1 ⁽³⁾	1 ~ 3	B ≥ 2 ⁽²⁾	16SP270M
SEPC, OS-CON (Radial)	16	270	11	5000	8 × 13	≥ 1 ⁽³⁾	1 ~ 2	B ≥ 2 ⁽²⁾	16SEPC270M
SVP, OS-CON (SMD)	16	330	16	4700	10 × 12,6	≥ 1 ⁽³⁾	1 ~ 3 ⁽⁴⁾	B ≥ 2 ⁽²⁾⁽⁴⁾	16SVP330M
AVX, Tantalum									
Series III	10	330	40	1828	7,3×4,3×4,1	N/R ⁽⁶⁾	1 ~ 6 ⁽⁴⁾	N/R ⁽⁵⁾	TPSE337M010R0040 (V _O ≤ 5.1V) ⁽⁷⁾
TPM Multianode	10	330	23	3000	7,3×4,3×4,1	N/R ⁽⁶⁾	1 ~ 3 ⁽⁴⁾	C ≥ 2 ⁽⁴⁾⁽²⁾	TPME337M010#0023 (V _O ≤ 5.1V) ⁽⁷⁾
TPS Series III (SMD)	4	1000	35	2405	7,3 × 5,7	N/R ⁽⁶⁾	1 ~ 5 ⁽⁴⁾	N/R ⁽⁵⁾	TPSV108K004R0035 (V _O ≤ 2.1V) ⁽⁸⁾
Kemet, Poly-Tantalum									
T520 (SMD)	10	330	25	2600	7,3×4,3×4,1	N/R ⁽⁶⁾	1 ~ 4 ⁽⁴⁾	C ≥ 2 ⁽²⁾	T520X337M010ASE025
T530 (SMD)	6.3	330	15	3800	7,3×4,3×4,1	N/R ⁽⁶⁾	2 ~ 3	B ≥ 2 ⁽²⁾	T530X337M006ASE015 (V _O ≤ 5.1V) ⁽⁸⁾
T530 (SMD)	4	680	5	7300	7,3×4,3×4,1	N/R ⁽⁶⁾	1	B ≥ 1 ⁽²⁾	T530X687M004ASE005 (V _O ≤ 3.5V) ⁽⁸⁾
T530 (SMD)	2.5	1000	5	7300	7,3 × 4,3	N/R ⁽⁶⁾	1	B ≥ 1 ⁽²⁾	T530X108M2R5ASE005 (V _O ≤ 2.0V) ⁽⁸⁾
Vishay-Sprague									
597D, Tantalum (SMD)	16	220	40	2300	7,2×5,7×4,1	N/R ⁽⁶⁾	1 ~ 5	C ≥ 2 ⁽²⁾	597D227X16E2T
94SP, OS-CON (Radial)	16	270	18	4400	10 × 10,5	≥ 1 ⁽³⁾	1 ~ 3	C ≥ 2 ⁽²⁾	94SP277X0016FBP
94SVP OS-CON(SMD)	16	330	17	4500	10 × 12,7	≥ 1 ⁽³⁾	1 ~ 3	B ≥ 2 ⁽²⁾	94SVP337X016F12
Kemet, Ceramic X5R									
(SMD)	16	10	2	–	3225	≥ 2 ⁽³⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	C1210C106M4PAC
	6.3	47	2	–	3225	N/R ⁽⁶⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	C1210C476K9PAC
Murata, Ceramic X5R									
(SMD)	6.3	100	2	–	3225	N/R ⁽⁶⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	GRM32ER60J107M
	6.3	47	2	–	3225	N/R ⁽⁶⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	GRM32ER60J476M
	25	22	2	–	3225	≥ 1 ⁽³⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	GRM32ER61E226K
	16	10	2	–	3225	≥ 2 ⁽³⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	GRM32DR61C106K
TDK, Ceramic X5R									
(SMD)	6.3	100	2	–	3225	N/R ⁽⁶⁾	≥ 1 ⁽⁹⁾	A ⁽²⁾	C3225X5R0J107MT
	6.3	47	2	–	3225	N/R ⁽¹⁰⁾	≥ 1 ⁽¹¹⁾	A ⁽¹²⁾	C3225X5R0J476MT
	16	10	2	–	3225	≥ 2 ⁽¹³⁾	≥ 1 ⁽¹¹⁾	A ⁽¹²⁾	C3225X5R1C106MT0
	16	22	2	–	3225	≥ 1 ⁽¹³⁾	≥ 1 ⁽¹¹⁾	A ⁽¹²⁾	C3225X5R1C226MT

(9) Any combination of ceramic capacitor values is limited to 500 µF for PTH08T240W and 5000 µF for PTH08T241W. The total capacitance for PTH08T240W is limited to 10,000 µF which includes all ceramic and non-ceramic types.

(10) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

(11) Any combination of ceramic capacitor values is limited to 500 µF for PTH08T240W and 5000 µF for PTH08T241W. The total capacitance for PTH08T240W is limited to 10,000 µF which includes all ceramic and non-ceramic types.

(12) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection Capacitor Types:

- a. Type A = (100 ≤ capacitance × ESR ≤ 1000)
- b. Type B = (1,000 < capacitance × ESR ≤ 5,000)
- c. Type C = (5,000 < capacitance × ESR ≤ 10,000)

(13) In addition to the required input electrolytic capacitance, ≥ 20 µF of ceramic capacitance is required to reduce the high-frequency reflected ripple current.

TurboTrans™ Technology

TurboTrans technology is a feature introduced in the T2 generation of the PTH/PTV family of power modules. TurboTrans optimizes the transient response of the regulator with added external capacitance using a single external resistor. Benefits of this technology include reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amount of output capacitance required to meet a target output voltage deviation will be reduced with TurboTrans activated. Likewise, for a given amount of output capacitance, with TurboTrans engaged, the amplitude of the voltage deviation following a load transient will be reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area will benefit greatly from this technology.

TurboTrans™ Selection

Utilizing TurboTrans requires connecting a resistor, R_{TT} , between the +Sense pin (pin6) and the TurboTrans pin (pin9). The value of the resistor directly corresponds to the amount of output capacitance required. All T2 products require a minimum value of output capacitance whether or not TurboTrans is utilized. For the PTH08T240W, the minimum required capacitance is 220 μ F. The minimum required capacitance for the PTH08T241W is 300 μ F of ceramic type. When using TurboTrans, capacitors with a capacitance \times ESR product below 10,000 μ F \times m Ω are required. (Multiply the capacitance (in μ F) by the ESR (in m Ω) to determine the capacitance \times ESR product.) See the Capacitor Selection section of the datasheet for a variety of capacitors that meet this criteria.

Figure 12 thru Figure 17 show the amount of output capacitance required to meet a desired transient voltage deviation with and without TurboTrans for several capacitor types; TypeA (e.g. ceramic), TypeB (e.g. polymer-tantalum), and TypeC (e.g. OS-CON). To calculate the proper value of R_{TT} , first determine your required transient voltage deviation limits and magnitude of your transient load step. Next, determine what type of output capacitors will be used. (If more than one type of output capacitor is used, select the capacitor type that makes up the majority of your total output capacitance.) Knowing this information, use the chart in Figure 12 thru Figure 17 that corresponds to the capacitor type selected. To use the chart, begin by dividing the maximum voltage deviation limit (in mV) by the magnitude of your load step (in Amps). This gives a mV/A value. Find this value on the Y-axis of the appropriate chart. Read across the graph to the 'With TurboTrans' plot. From this point, read down to the X-axis which lists the minimum required capacitance, C_O , to meet that transient voltage deviation. The required R_{TT} resistor value can then be calculated using the equation or selected from the TurboTrans table. The TurboTrans tables include both the required output capacitance and the corresponding R_{TT} values to meet several values of transient voltage deviation for 25%(2.5A), 50%(5A), and 75%(7.5A) output load steps.

The chart can also be used to determine the achievable transient voltage deviation for a given amount of output capacitance. By selecting the amount of output capacitance along the X-axis, reading up to the desired 'With TurboTrans' curve, and then over to the Y-axis, gives the transient voltage deviation limit for that value of output capacitance. The required R_{TT} resistor value can be calculated using the equation or selected from the TurboTrans table.

As an example, let's look at a 12-V application requiring a 50 mV deviation during an 5A, 50% load transient. A majority of 330 μ F, 10 m Ω output capacitors will be used. Use the 12-V, Type B capacitor chart, Figure 14. Dividing 50mV by 5A gives 10mV/A transient voltage deviation per amp of transient load step. Select 10mV/A on the Y-axis and read across to the 'With TurboTrans' plot. Following this point down to the X-axis gives a minimum required output capacitance of approximately 680 μ F. The required R_{TT} resistor value for 680 μ F can then be calculated or selected from Table 5. The required R_{TT} resistor is approximately 7.32k Ω .

To see the benefit of TurboTrans, follow the 10mV/A marking across to the 'Without TurboTrans' plot. Following that point down shows that you would need a minimum of 3000 μ F of output capacitance to meet the same transient deviation limit. This is the benefit of TurboTrans.

PTH08T241W - Type A Ceramic Capacitors

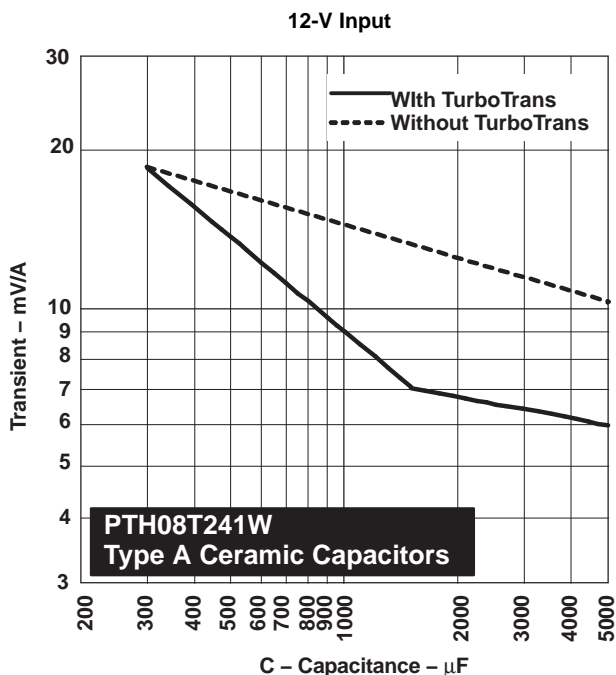


Figure 12. Capacitor Type A, $100 \leq C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 1000$ (e.g. Ceramic)

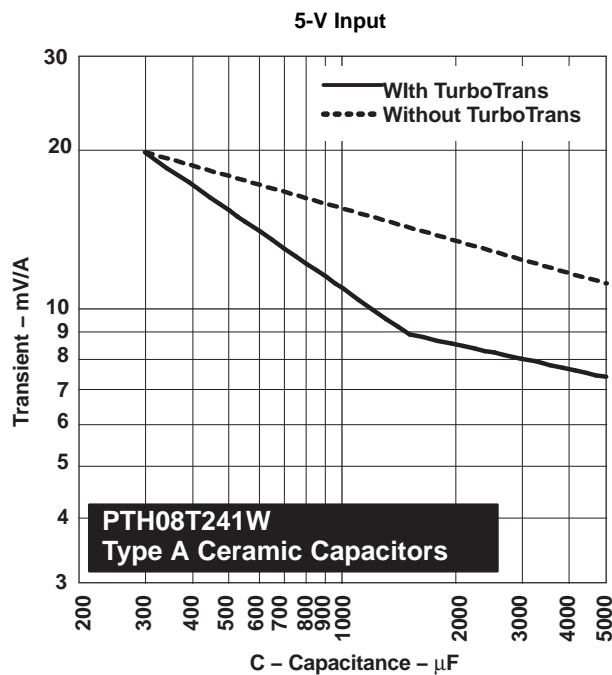


Figure 13. Capacitor Type A, $100 \leq C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 1000$ (e.g. Ceramic)

Table 4. Type A TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12-V Input		5-V Input	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)
50	100	150	300	open	300	open
45	90	135	310	1180	370	140
40	80	120	380	118	470	49.9
35	70	105	470	47.5	610	23.2
30	60	90	610	22.6	830	10.0
25	50	75	830	10.0	1200	2.61
20	40	60	1220	2.49	3050	short

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see [Equation 2](#)

$$R_{TT} = 40 \times \frac{[1 - (C_O/1500)]}{[(5 \times C_O/1500) - 1]} \text{ (k}\Omega\text{)} \tag{2}$$

Where C_O is the total output capacitance in μF . C_O values greater than or equal to 1500 μF require R_{TT} to be a short, 0 Ω .

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

PTH08T240W Type B Capacitors

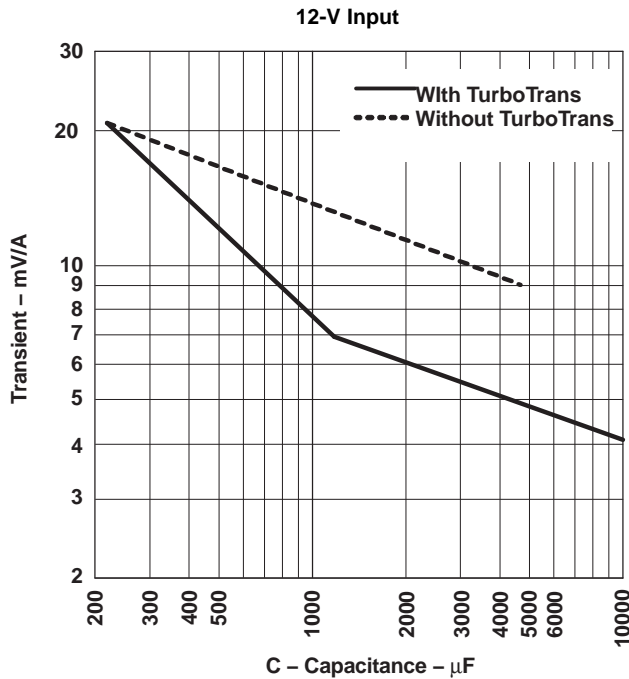


Figure 14. Cap Type B, $1000 < C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 5000$ (e.g. Polymer-Tantalum)

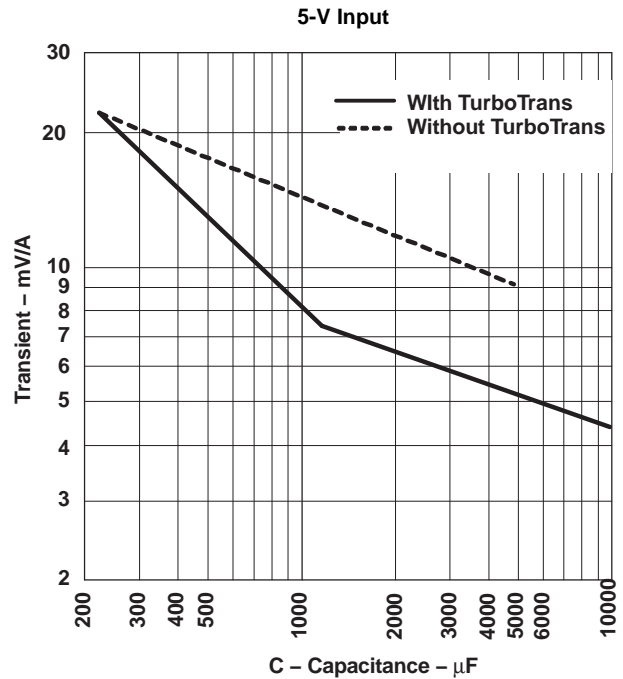


Figure 15. Cap Type B, $1000 < C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 5000$ (e.g. Polymer-Tantalum)

Table 5. Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12-V Input		5-V Input	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)
55	110	165	220	open	220	open
40	80	120	330	57.6	360	42.2
35	70	105	400	30.9	450	23.7
30	60	90	510	16.2	560	12.7
25	50	75	680	7.32	750	5.49
20	40	60	1000	1.58	1050	0.536
15	30	45	2100	short	2600	short
10	20	30	10500	short	exceeds limit	—

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 3. For $V_O > 3.45\text{V}$ please contact TI for C_O and R_{TT} values.

$$R_{TT} = \frac{40 \times [1 - (C_O/1100)]}{[(C_O/220) - 1]} \text{ (k}\Omega\text{)} \tag{3}$$

Where C_O is the total output capacitance in μF . C_O values greater than or equal to $1100 \mu\text{F}$ require R_{TT} to be a short, 0Ω . (R_{TT} results in a negative value when $C_O > 1100\mu\text{F}$).

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

PTH08T240W Type C Capacitors

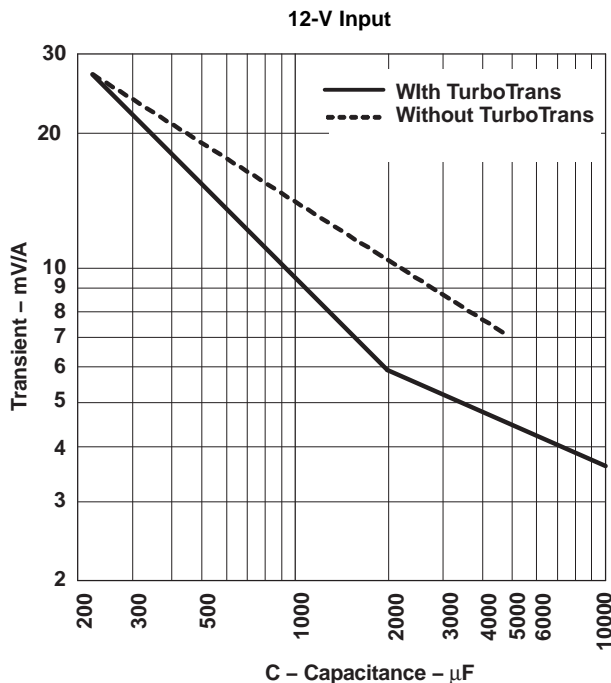


Figure 16. Cap Type C, $5000 < C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 10,000$ (e.g. OS-CON)

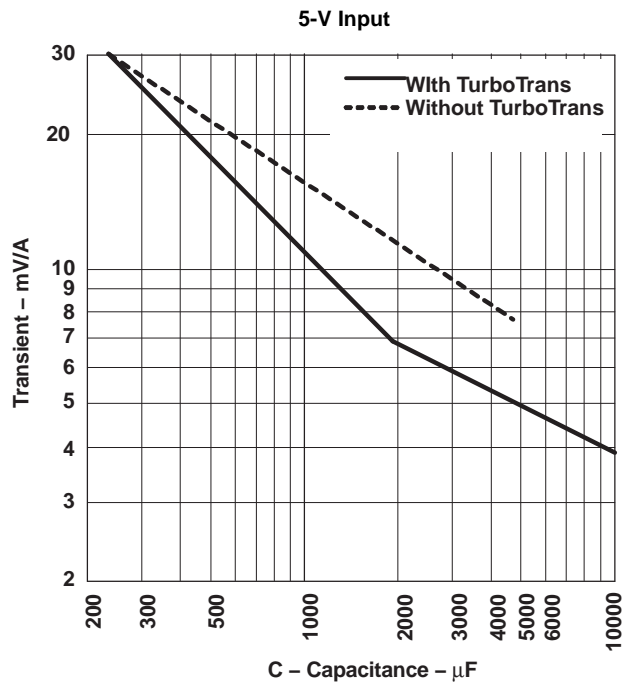


Figure 17. Cap Type C, $5000 < C(\mu\text{F}) \times \text{ESR}(\text{m}\Omega) \leq 10,000$ (e.g. OS-CON)

Table 6. Type C TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12-V Input		5-V Input	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)	C_O Minimum Required Output Capacitance (μF)	R_{TT} Required TurboTrans Resistor ($\text{k}\Omega$)
75	150	225	220	open	250	1300
60	120	180	270	294	330	133
45	90	135	400	68.1	480	45.3
35	70	105	580	31.6	700	21.5
30	60	90	720	20.0	860	13.7
25	50	75	950	11.8	1150	7.68
20	40	60	1300	5.23	1550	2.61
15	30	45	2000	short	2800	short
10	20	30	7400	short	exceeds limit	—

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 4. For $V_O > 3.45\text{V}$ please contact TI for C_O and R_{TT} values.

$$R_{TT} = \frac{40 \times [1 - (C_O/1980)]}{\left[\left(\frac{5 \times C_O + 880}{1980} \right) - 1 \right]} \text{ (k}\Omega\text{)} \tag{4}$$

Where C_O is the total output capacitance in μF . C_O values greater than or equal to $1980 \mu\text{F}$ require R_{TT} to be a short, 0Ω . (R_{TT} results in a negative value when $C_O > 1980\mu\text{F}$).

To ensure stability, the value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

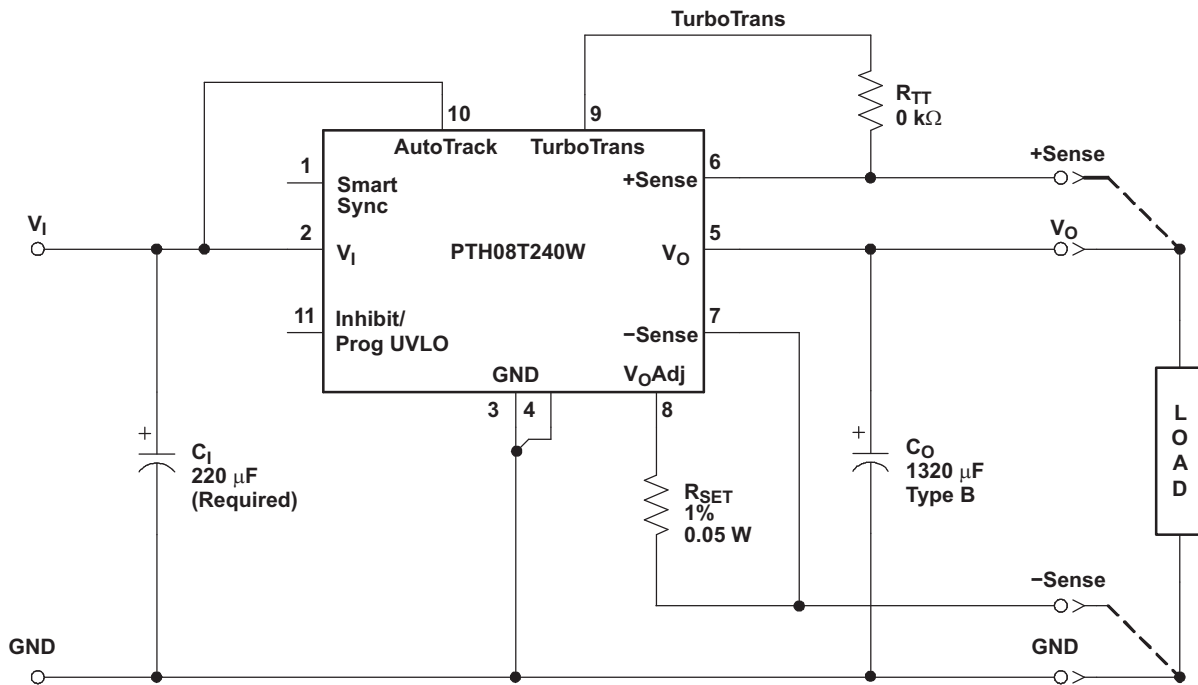


Figure 18. Typical TurboTrans™ Application

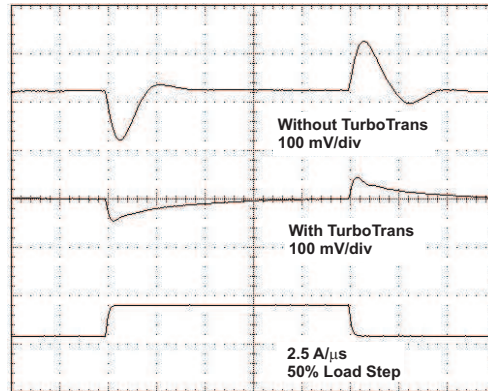


Figure 19. Typical TurboTrans Waveforms

UNDERVOLTAGE LOCKOUT (UVLO)

The PTH08T240/241W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator’s input source during the power-up sequence.

The UVLO characteristic is defined by the ON threshold (V_{THD}) voltage. Below the ON threshold, the Inhibit control is overridden, and the module does not produce an output. The hysteresis voltage, which is the difference between the ON and OFF threshold voltages, is set at 500 mV. The hysteresis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

The UVLO feature of the PTH08T240/241W module allows for limited adjustment of the ON threshold voltage. The adjustment is made via the *Inhibit/UVLO Prog* control pin (pin 11) using a single resistor (see Figure 20). When pin 11 is left open circuit, the ON threshold voltage is internally set to its default value, which is 4.3 volts. The ON threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. Adjusting the threshold prevents the module from operating if the input bus fails to completely rise to its specified regulation voltage.

Equation 5 determines the value of R_{UVLO} required to adjust V_{THD} to a new value. The default value is 4.3 V, and it may only be adjusted to a higher value.

$$R_{UVLO} = \frac{9690 - (137 \times V_I)}{(137 \times V_I) - 585} \text{ (k}\Omega\text{)} \tag{5}$$

Table 7 shows a chart of standard resistor values for R_{UVLO} for different options of the on-threshold (V_{THD}) voltage.

Table 7. Standard R_{UVLO} values for Various V_{THD} values

V_{THD} (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0
R_{UVLO} (k Ω)	88.7	52.3	37.4	28.7	23.2	19.6	16.9	14.7	13.0	11.8	10.5	9.76	8.87

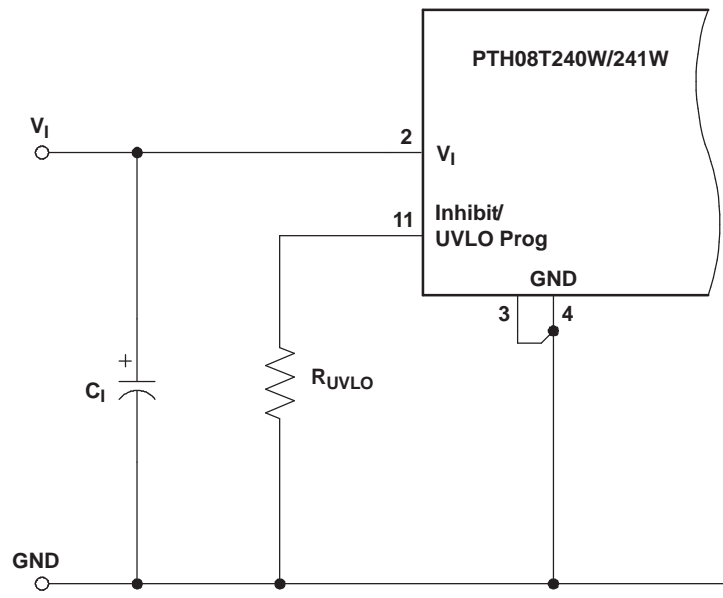


Figure 20. Undervoltage Lockout Adjustment Resistor Placement

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I (see Figure 21).

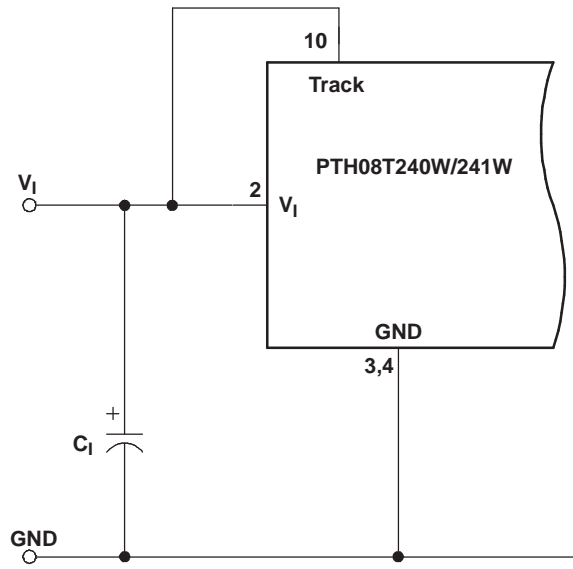


Figure 21. Defeating the Auto-Track Function

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 2 ms–10 ms) before allowing the output voltage to rise.

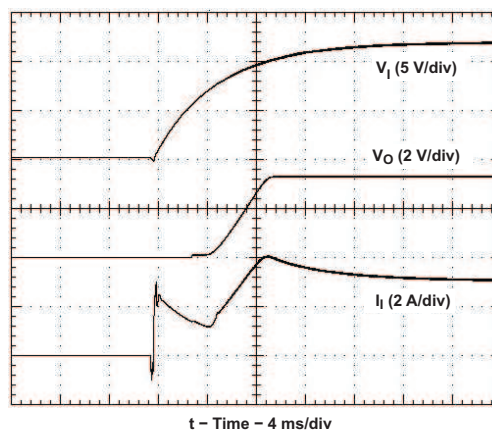


Figure 22. Power-Up Waveform

The output then progressively rises to the module's setpoint voltage. Figure 22 shows the soft-start power-up characteristic of the PTH08T240/241W operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 10-A constant current load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 15 ms.

On/Off Inhibit

For applications requiring output voltage on/off control, the PTH08T240/241W incorporates an Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 23 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up. An external pull-up resistor should never be used with the inhibit pin. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

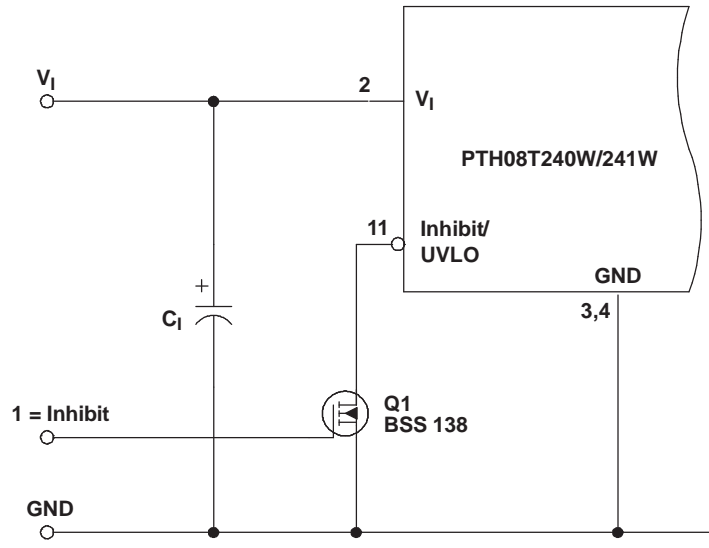


Figure 23. On/Off Inhibit Control Circuit

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 15 ms. Figure 24 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH} . The waveforms were measured with a 10-A constant current load.

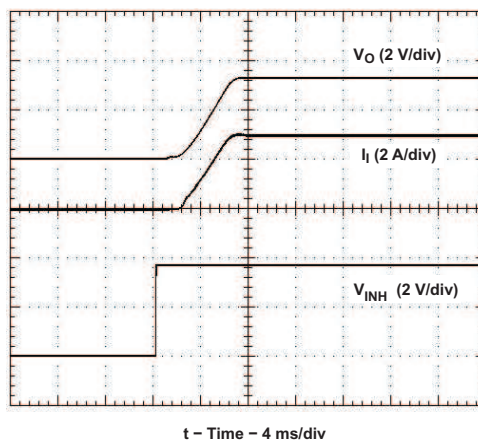


Figure 24. Power-Up Response from Inhibit Control

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Differential Output Voltage Remote Sense

Differential remote sense improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load in either the positive or return path. An IR drop is caused by the output current flowing through the small amount of pin and trace resistance. With the sense pins connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3V. Connecting the +Sense (pin 6) to the positive load terminal improves the load regulation at the connection point. For optimal behavior the –Sense (pin 7) must be connected to GND (pin 4) close to the module (within 10 cm).

If the remote sense feature is not used at the load, connect the +Sense pin to V_O (pin5) and connect the –Sense pin to the module GND (pin 4).

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Smart Sync

Smart Sync is a feature that allows multiple power modules to be synchronized to a common frequency. Driving the Smart Sync pins with an external oscillator set to the desired frequency, synchronizes all connected modules to the selected frequency. The synchronization frequency can be higher or lower than the nominal switching frequency of the modules within the range of 240 kHz to 400 kHz (see Electrical Specifications table for frequency limits). Synchronizing modules powered from the same bus, eliminates beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the low beat frequencies (usually < 10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Power modules can also be synchronized out of phase to minimize source current loading and minimize input capacitance requirements. Figure 25 shows a standard circuit with two modules synchronized 180° out of phase using a D flip-flop.

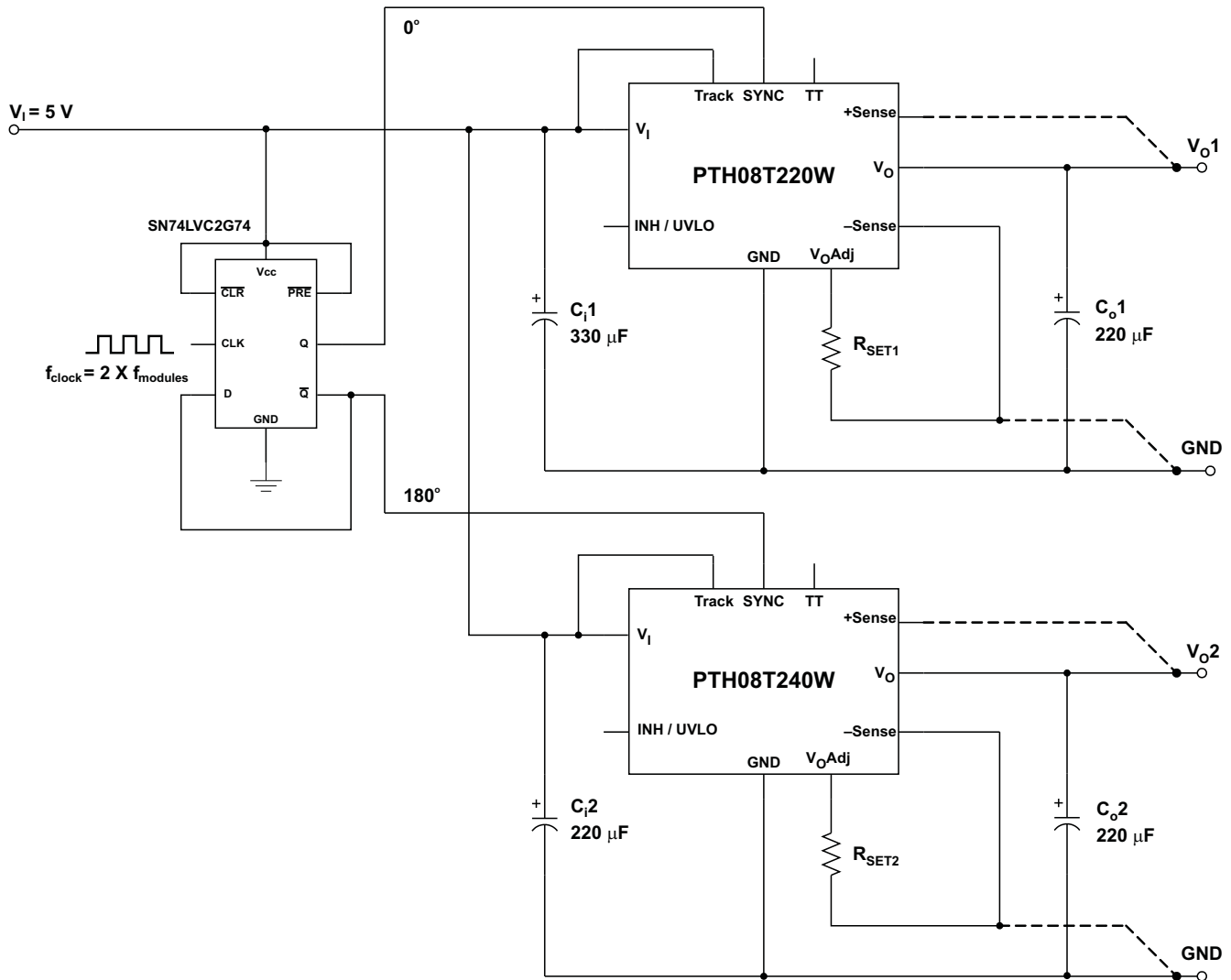


Figure 25. Smart Sync Schematic

Smart Sync Considerations

Operating the PTH08T240W with a low duty cycle may increase the output voltage ripple due to pulse skipping of the PWM controller. When operating at the nominal switching frequency, input voltages greater than ($V_O \times 11$) may cause the output voltage ripple to increase (typically $2\times$).

Synchronizing to a higher frequency and operating with a low duty cycle may impact output voltage ripple. When operating at 300 kHz, [Figure 26](#) shows the operating region where the output voltage ripple meets the electrical specifications and the operating region where the output voltage ripple may increase. [Figure 27](#) shows the operating regions for several switching frequencies. For example, a module operating at 400 kHz and an output voltage of 1.2 V, the maximum input voltage that meets the output voltage ripple specification is 10 V. Exceeding 10 V may cause in an increase in output voltage ripple. As shown in [Figure 27](#), operating below 6V allows operation down to the minimum output voltage over the entire synchronization frequency range without affecting the output voltage ripple. See the *Electrical Characteristics* table for the synchronization frequency range limits.

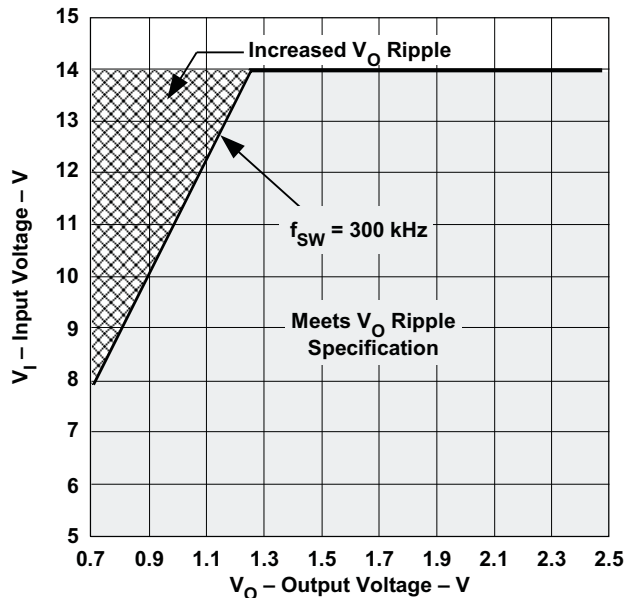


Figure 26. V_O Ripple Regions at 300 kHz ⁽¹⁾⁽²⁾

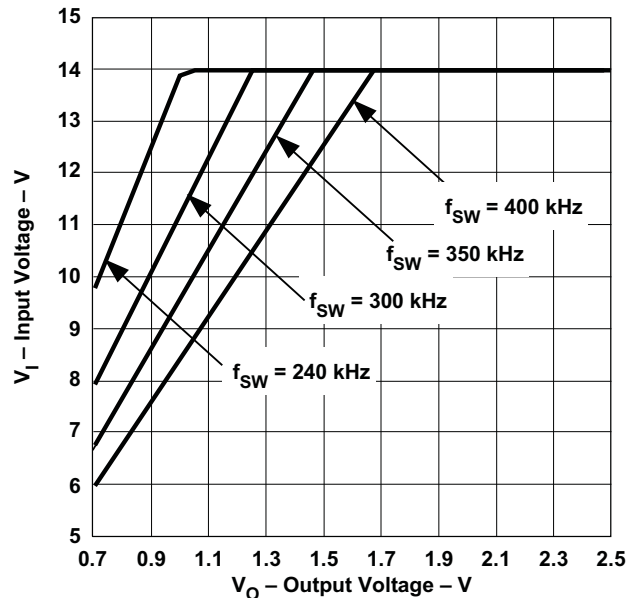


Figure 27. V_O Ripple Regions ⁽¹⁾⁽²⁾

- (1) Operation above a given curve may cause the output voltage ripple to increase (typically $2\times$).
- (2) When operating at the nominal switching frequency refer to the 300 kHz plot.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin ⁽¹⁾. This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point ⁽²⁾. As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a

volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit⁽³⁾. For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Sequencing Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in [Figure 28](#).

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization⁽⁴⁾, enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

[Figure 28](#) shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of PTH08T240/241W modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 4.3 V. The 28-ms time period is controlled by the capacitor C_T . The value of 2.2 μF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

[Figure 29](#) shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms, V_{O1} and V_{O2} , represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK} , V_{O1} , and V_{O2} are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in [Figure 30](#). Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I .
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises according to its softstart rate after input power has been applied.
6. The Auto-Track pin should never be used to regulate the module's output voltage for long-term, steady-state operation.

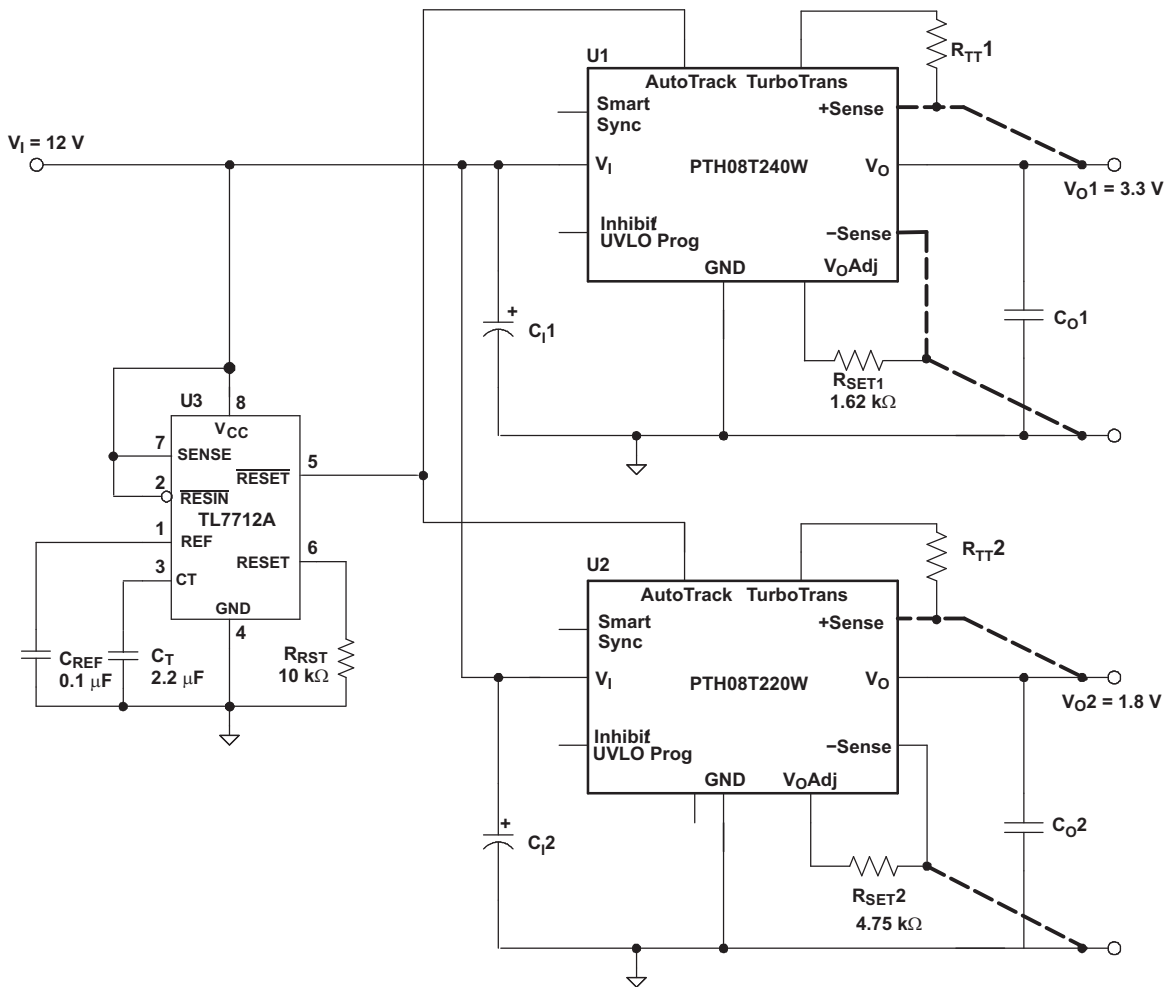


Figure 28. Sequenced Power Up and Power Down Using Auto-Track

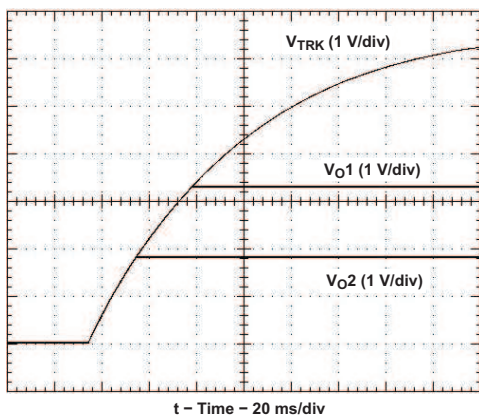


Figure 29. Simultaneous Power Up With Auto-Track Control

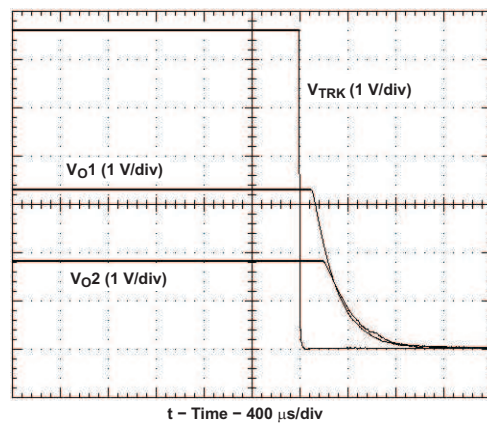


Figure 30. Simultaneous Power Down With Auto-Track Control

Prebias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH family of power modules incorporate synchronous rectifiers, but does not sink current during startup⁽¹⁾, or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained⁽²⁾. Figure 31 shows an application demonstrating the prebias startup capability. The startup waveforms are shown in Figure 32. Note that the output current (I_o) is negligible until the output voltage rises above the voltage backfed through the intrinsic diodes.

The prebias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it sinks current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled⁽³⁾, or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

1. Startup includes the short delay (approximately 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the Track pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the output voltage *throughout* the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by connecting the Track pin to V_I .

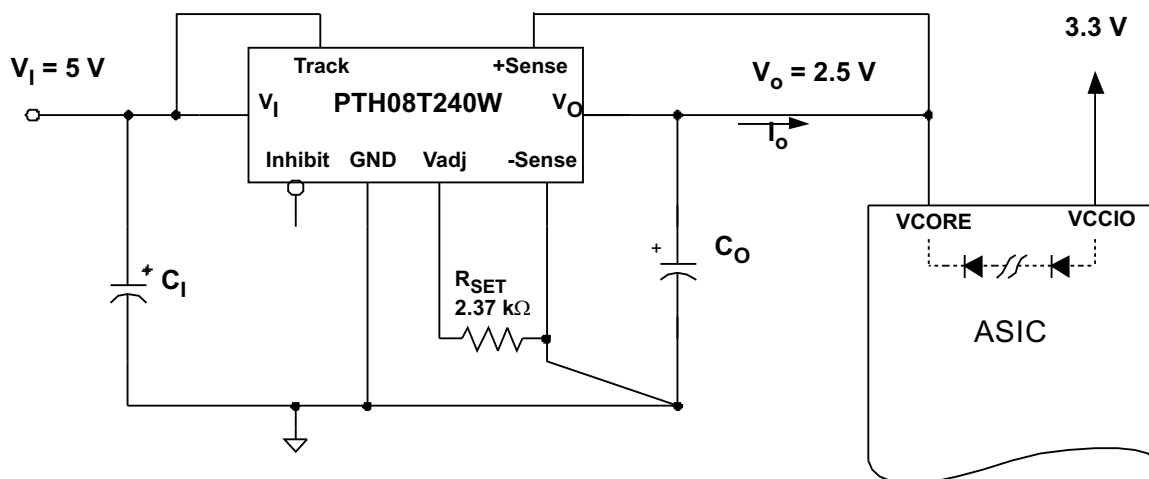


Figure 31. PreBias Startup Application Circuit

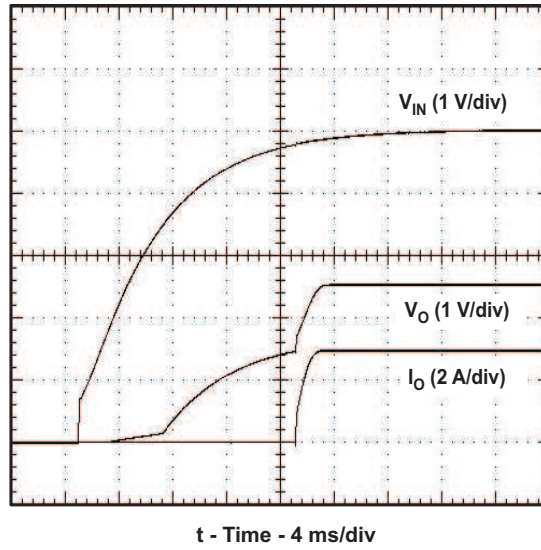
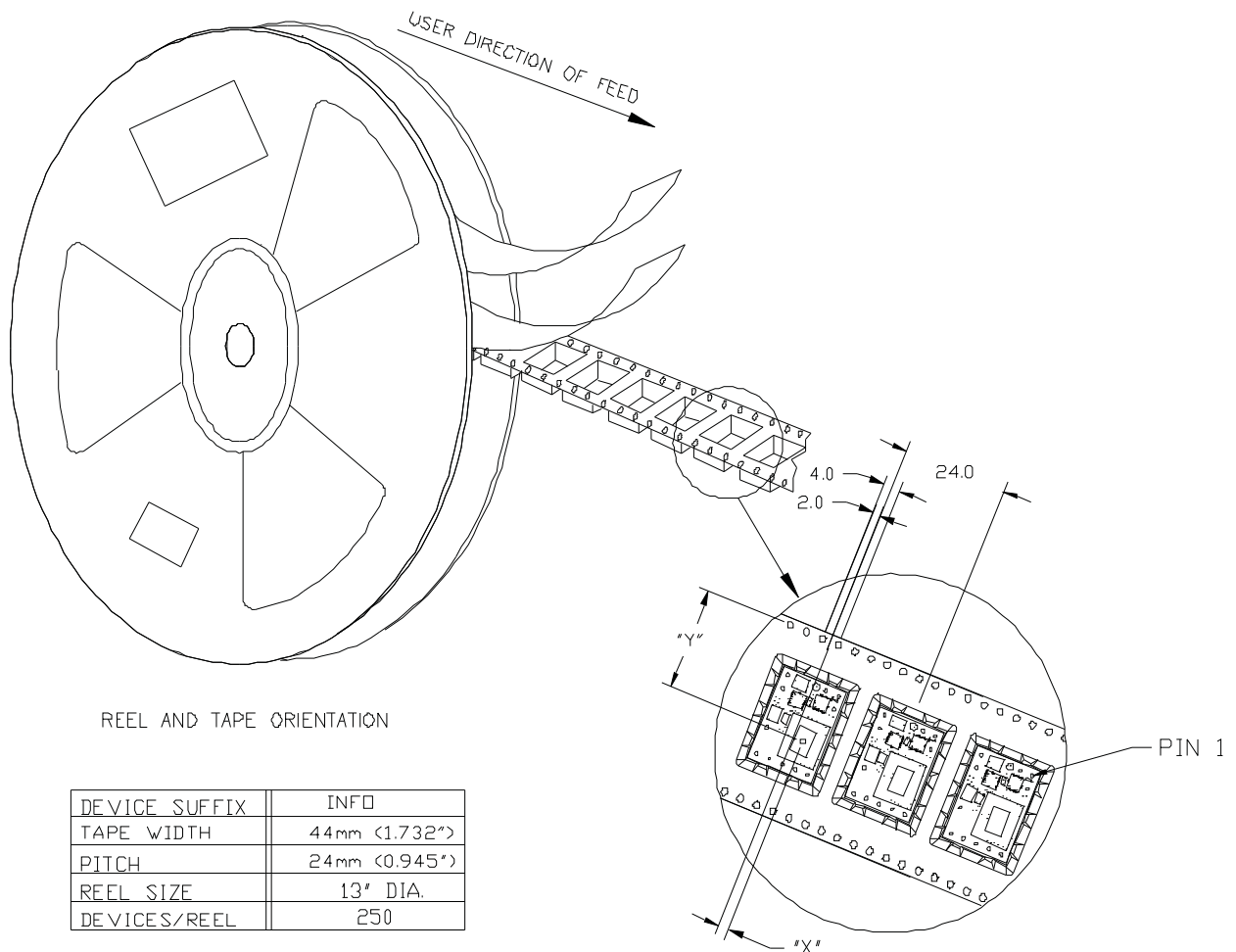


Figure 32. Prebias Startup Waveforms

TAPE AND REEL

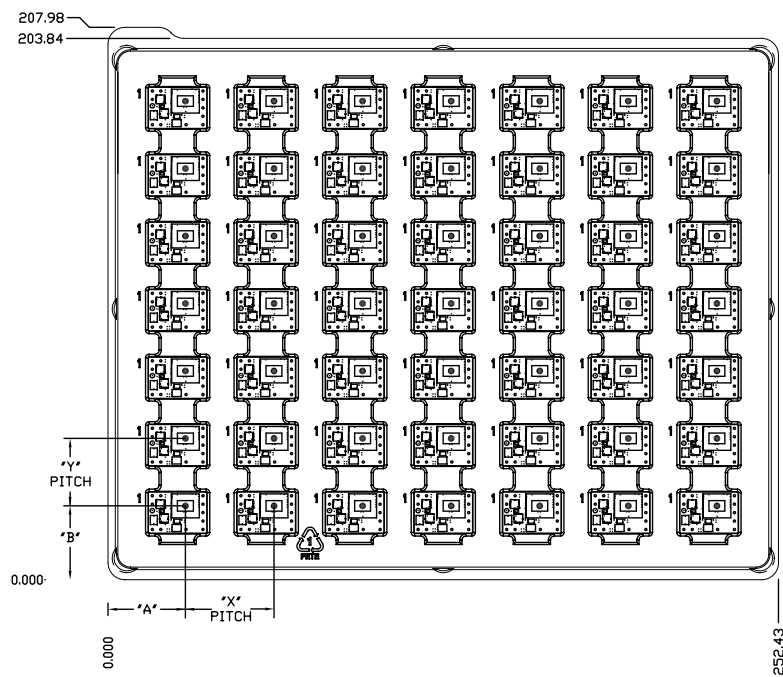


REEL AND TAPE ORIENTATION

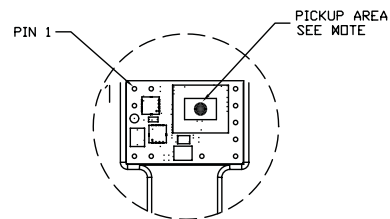
DEVICE SUFFIX	INFO
TAPE WIDTH	44mm (1.732")
PITCH	24mm (0.945")
REEL SIZE	13" DIA.
DEVICES/REEL	250

PTXXX0X	"X"	"Y"
PTH08T240	2.54mm	23.12mm

TRAY



0.375 (9.52)



NOTE: THE INDUCTOR IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

PTXXX6X	'A'	'B'	'X'	'Y'
PTH08T240	29.12	27.81	33.35	25.40

ALL DIMENSIONS ARE IN MILLIMETER.

DEVICES/TRAY	49
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTH08T240WAD	ACTIVE	Through-Hole Module	EBS	11	49	RoHS (In Work) & Green (In Work)	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T240WAH	ACTIVE	Through-Hole Module	EBS	11	49	RoHS (In Work) & Green (In Work)	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T240WAS	ACTIVE	Surface Mount Module	EBT	11	49	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T240WAST	ACTIVE	Surface Mount Module	EBT	11	250	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T240WAZ	ACTIVE	Surface Mount Module	BBT	11	49	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T240WAZT	ACTIVE	Surface Mount Module	BBT	11	250	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T241WAD	ACTIVE	Through-Hole Module	EBS	11	49	RoHS (In Work) & Green (In Work)	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T241WAS	ACTIVE	Surface Mount Module	EBT	11	49	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T241WAST	ACTIVE	Surface Mount Module	EBT	11	250	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T241WAZ	ACTIVE	Surface Mount Module	BBT	11	49	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T241WAZT	ACTIVE	Surface Mount Module	BBT	11	250	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

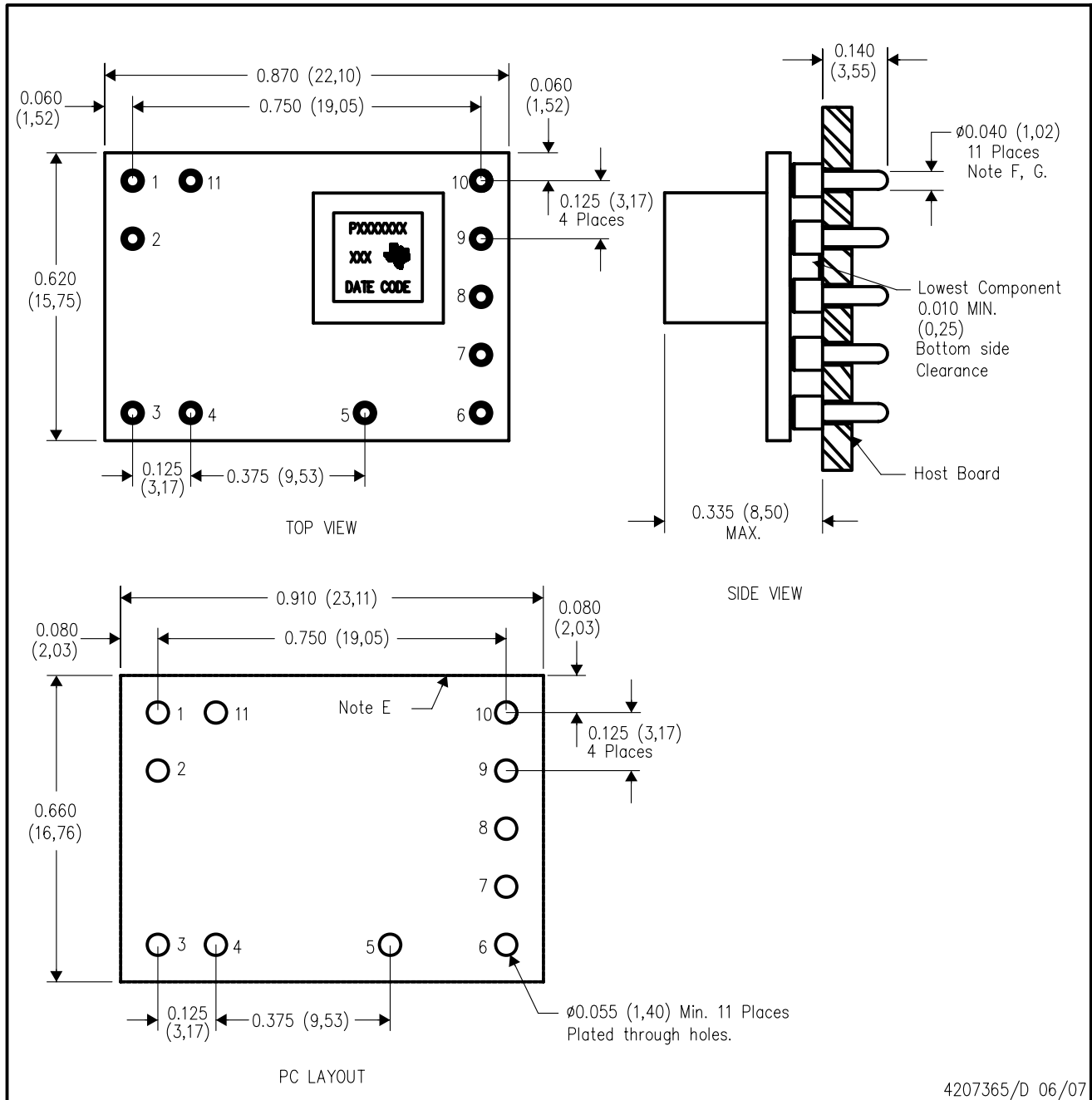
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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EBS (R-PDSS-T11)

DOUBLE SIDED MODULE



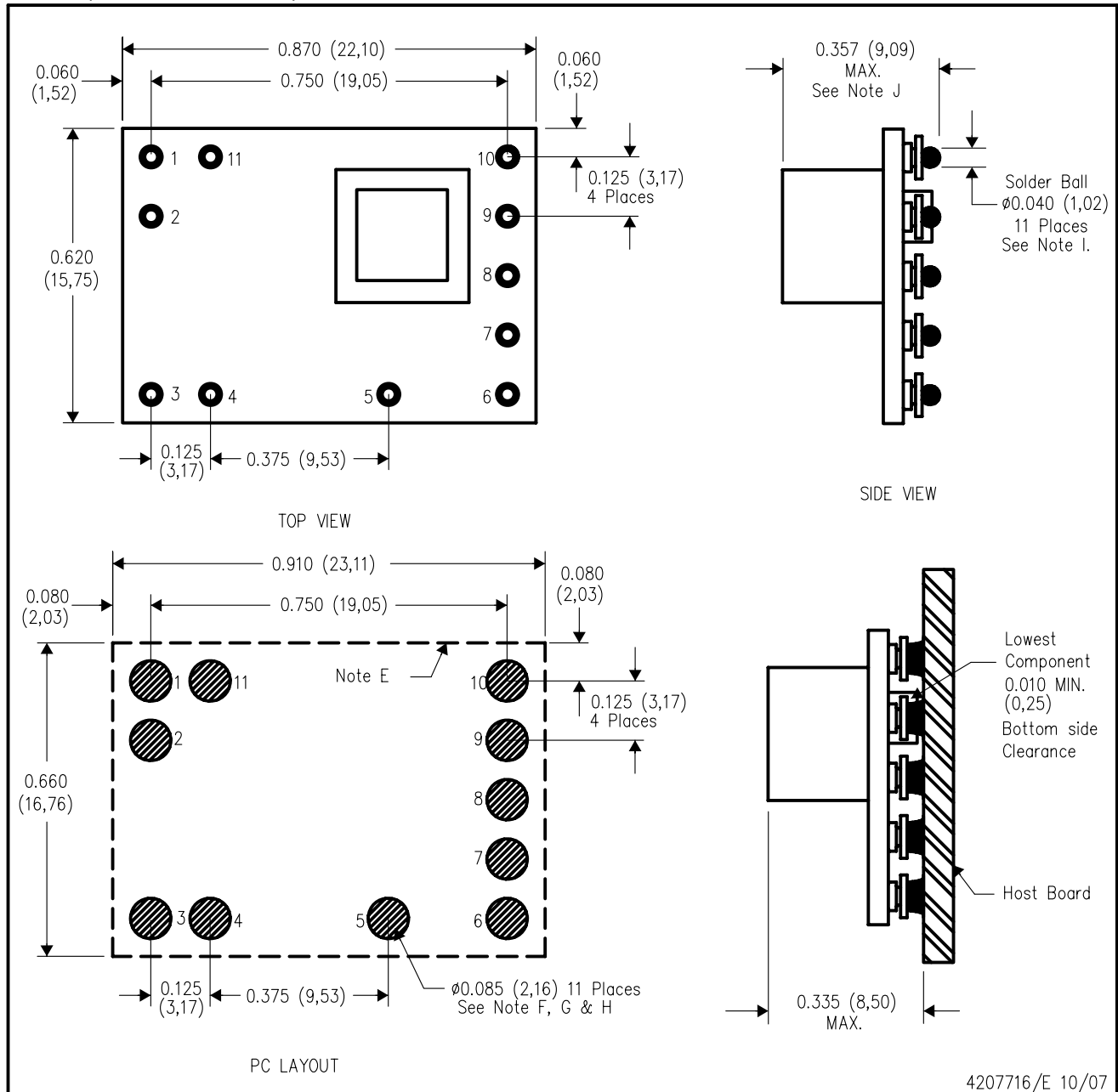
4207365/D 06/07

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.

- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

BBT (R-PDSS-B11)

DOUBLE SIDED MODULE

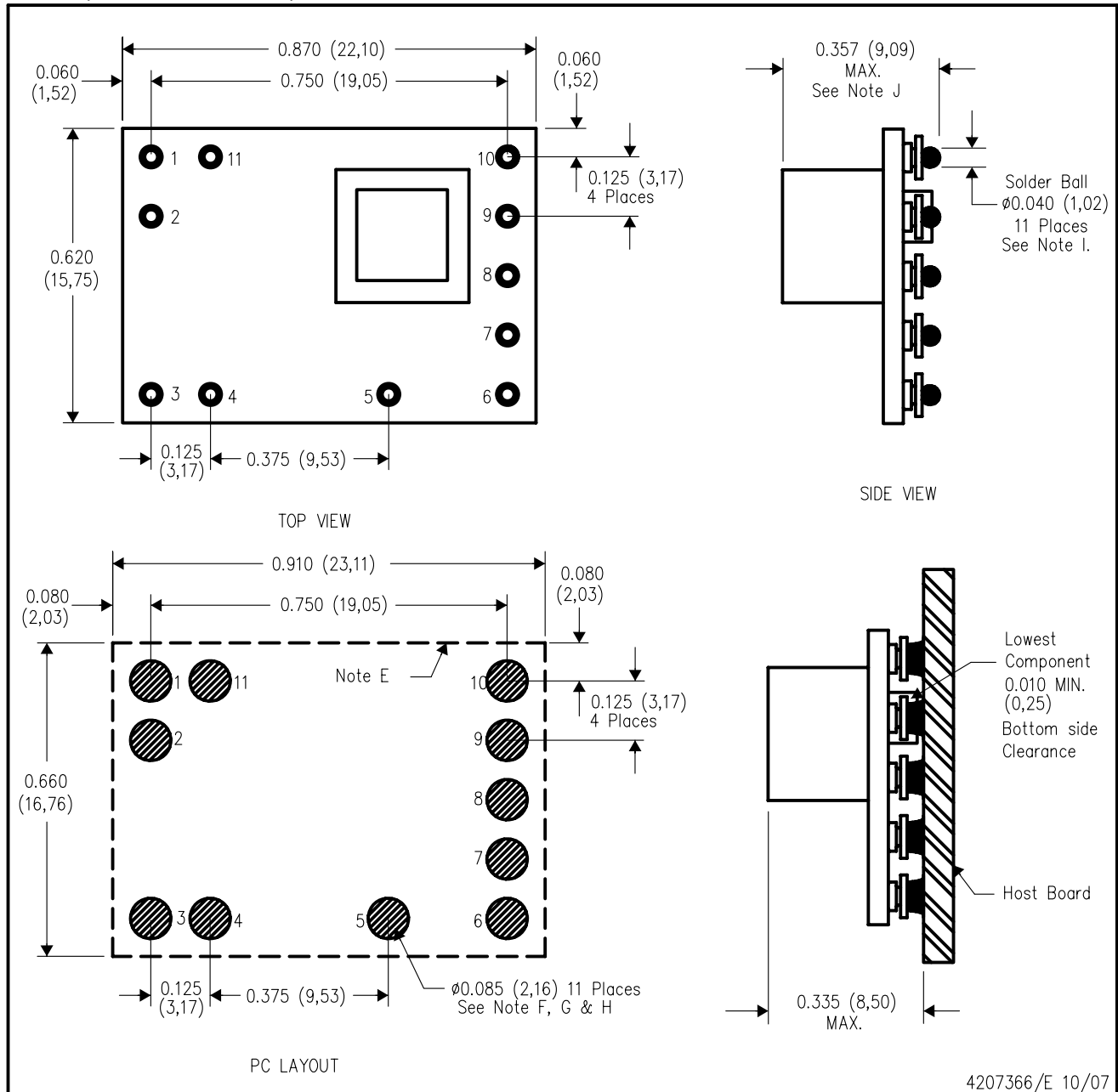


- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).

- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – 96.5 Sn/3.0 Ag/0.5 Cu
- J. Dimension prior to reflow solder.

EBT (R-PDSS-B11)

DOUBLE SIDED MODULE



- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).

- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
- J. Dimension prior to reflow solder.

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