PIC16(L)F1934/1936/1937 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1934/1936/1937 family devices that you have received conform functionally to the current Device Data Sheet (DS41364**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1934/1936/1937 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A9**).

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1934/1936/1937 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)							
	DEV<8:0>	Revision ID for Silicon Revision						
		A2	A3	A5	A6	A7	A8	A9
PIC16F1934	10 0011 010	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001
PIC16LF1934	10 0100 010	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001
PIC16F1936	10 0011 011	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001
PIC16LF1936	10 0100 011	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001
PIC16F1937	10 0011 100	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001
PIC16LF1937	10 0100 100	0 0010	0 0011	0 0101	0 0110	0 0111	0 1000	0 1001

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16F193X/LF193X/PIC16F194X/LF194X/PIC16LF190X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A2	A3	A5	A6	A7	A8	A9
Data EE Memory	Memory Endurance	1.1	Erase/Write Endurance limited.	X	X	X				
Data EE Memory	Writes	1.2	Min. VDD for writes.	X	X	X	X	X	X	X
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write Endurance limited.	X	X	X				
Program Flash Memory (PFM)	Writes	2.2	Min. VDD for writes.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	PWM Dead-Band Delay	3.1	Unpredictable waveforms.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	ECCP2 Switching	3.2	PWM outputs.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	ECCP2 Changing Direction	3.3	Outputs will improperly go active.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	Capture mode	3.4	Capture will be triggered.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	ECCPx Dead-Time Delay	3.5	Dead-band delay.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	PWM with Pulse Steering	3.6	PWM output.	X	X	X	X	X	X	X
Capture Compare PWM (CCP)	Capture mode	3.7	Capture will be triggered.	X	X	X	X	X	X	X
Brown-Out Reset (BOR)	Threshold	4.1	Voltage level.	X						
ADC	ADC Conversion	5.1	ADC conversion may not complete.	X	X	X				
Oscillator	HS Oscillator	6.1	HS oscillator min. VDD.	X	X	X				
Oscillator	Oscillator Start-up Timer	6.2	OSTS bit remains set.	X	X	X	X	X	X	
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	7.1	PWM 0% duty-cycle direction change.	X	X	X	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	7.2	PWM 0% duty-cycle port steering.	X	X	X	X	X	X	X
Timer1	Timer0 Gate Source	8.1	Toggle mode works improperly.	X	X	X	X	X	X	X
Timer1	Timer1 Gate Toggle mode	8.2	T1 gate flip-flop does not clear.	X	X	X	X	X	X	X
LDO	Minimum VDD above 85°C	9.1	Minimum operating VDD for the PIC16F193X devices at TA > 85°C.	X	X	X	X	X	X	X
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	Auto-Baud Detect	10.1	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	X	X	X	X		
Reset	RESET instruction	11.1	Extended Reset if clock selection is MFINTOSC or HFINTOSC	X	X	X	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A2	A3	A5	A6	A7	A8	A9
MSSP (Master Synchronous Serial Port)	SPI Master mode	12.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A9**).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the data EE memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X					

1.2 Data EE Write at Min. VDD

The minimum voltage required for a data EE write operation is 2.0 volts.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when VDD is above 3.0 volts. Endurance degrades when VDD is below 3V.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X					

2.2 Program Flash Memory Writes at Min. VDD

The minimum voltage required for a PFM write operation is 2.0V.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3. Module: Capture Compare PWM (CCP)

3.1 Dead-Band Delay

With the ECCP configured for PWM Half-Bridge mode and a dead-band delay greater than or equal to the PWM duty cycle; unpredictable waveforms will result.

Work around

Make sure the dead-band delay is always less than the PWM duty cycle.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.2 ECCP2 Switching Between Single, Half-Bridge and Full-Bridge PWM modes

Switching PWM mode during the current PWM cycle by modifying the P2M<1:0> bits in the CCP2CON register will cause the PWM outputs to switch immediately and not on the start of the next PWM cycle.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.3 ECCP2 Changing Direction in Full-Bridge PWM modes

When changing direction, the active and modulated outputs will improperly go active at the same time and the dead time does not occur, which can lead to large shoot-through currents.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.4 Capture mode Selected while CCPx Pin is Held High

If the module is configured to capture on the first rising edge and the CCPx pin is high at this time, a capture will be triggered.

Work around

Clear the CCP interrupt flag (`CCPxIF = 0`) immediately after configuring the module for a capture event.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.5 ECCPx Dead-Time Delay in Half-Bridge mode

In Half-Bridge mode, the dead-band delay is 1 TOSC longer than calculated for the first PWM cycle and 1.5 TOSC for following cycles.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.6 PWM with Pulse Steering

Disabling a PWM output during a PWM cycle will cause the output to end 1 TOSC time earlier than expected.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

3.7 Capture mode Selected while CCPx Pin is Held Low

If the module is configured to capture on the first falling edge and the CCPx pin is low at this time, a capture will be triggered.

Work around

Clear the CCP interrupt flag (`CCPxIF = 0`) immediately after configuring the module for a capture event.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

4. Module: Brown-Out Reset (BOR)

4.1 Brown-Out Threshold

Configuring the BOR for 2.5V operation, the Reset will typically occur at 2.7V.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X							

5. Module: ADC

5.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/$\overline{\text{DONE}}$ bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

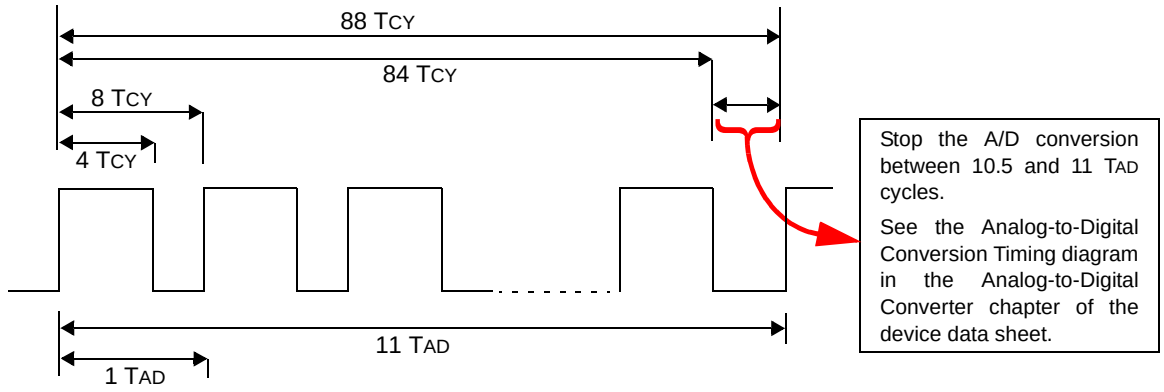
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/$\overline{\text{DONE}}$ bit in software. The GO/$\overline{\text{DONE}}$ bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter chapter of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF     ADCON0, ADGO    ; Start ADC conversion
                        ; Provide 86
                          instruction cycle
                          delay here
BCF     ADCON0, ADGO    ; Terminate the
                          conversion manually
MOVF    ADRESH, W       ; Read conversion
                          result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X					

6. Module: Oscillator

6.1 HS Oscillator

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X					

6.2 Oscillator Start-up Timer

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X		

7. Module: Enhanced Capture Compare PWM (ECCP)

7.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

7.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/ disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

8. Module: Timer1

8.1 Timer1 Gate Toggle mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

8.2 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

9. Module: LDO

9.1 Minimum VDD above 85°C

The minimum voltage required for the PIC16F193X devices is 3.5 volts for temperatures above 85°C.

Note:	This issue only applies to the PIC16F193X devices operating in the Extended temperature range. The PIC16LF193X devices are not affected.

Work around

None.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

10. Module: Enhanced Universal Synchronous Asynchronous Receiver (EUSART)

10.1 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, see Technical Brief TB3069*, "Use of Auto-Baud for Reception of LIN Serial Communications* Devices: *Mid-Range and Enhanced Mid-Range"*.

EXAMPLE 2: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);                     // if out of spec, use DEFAULT_BAUD
}
   •                                                // if in spec, continue using the
   •                                                // Auto-Baud value in SPBRG
   •
```

EXAMPLE 3: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit

int Average_Baud;                                    // Define Average_Baud variable
int Integrator;                                      // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;                         // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;                        // The running 16 count average
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Check if value is within limits
    SPBRG_16BIT = Average_Baud;                      // If out of spec, use previous average
}
else                                                 // If in spec, calculate the running
{                                                    // average but continue using the
    Integrator+ = SPBRG_16BIT;                       // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X			

11. Module: Reset

11.1 RESET Instruction

When using either the MFINTOSC or HFINTOSC as the primary clock source, and after executing a RESET instruction or when the device executes a Stack Overflow/ Underflow Reset, the device might remain in Reset.

Work around

Method 1: Use the Watchdog Timer (WDT) to recover from this issue.

Method 2: In place of the RESET instruction, use GOTO 0x0000.

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X		

12. Module: MSSP (Master Synchronous Serial Port)

12.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A5	A6	A7	A8	A9	
X	X	X	X	X	X	X	

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41364**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Oscillator

5.5 Fail-Safe Clock Monitor

5.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared **after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware**.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2009)

Initial release of this document.

Rev B Document (1/2010)

Added Silicon Revision A5.

Rev C Document (5/2010)

Added Modules 5, 6, 7 and 8.

Data Sheet Clarifications: Added Modules 1 and 2.

Rev D Document (6/2010)

Added Silicon Revision A6.

Rev E Document (7/2010)

Revised Module 5.1; Added Module 8.2; Other minor corrections.

Rev F Document (9/2010)

Added Module 9, LDO.

Rev G Document (9/2011)

Added Silicon Revision A7.

Data Sheet Clarifications: Removed Modules 1 and 2.

Rev H Document (2/2012)

Updated Table 1; Added Module 6.2, 6.3 and 6.4; Added Module 10, EUSART; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev J Document (7/2012)

Added MPLAB X IDE; Removed the Clock Switching module.

Rev K Document (7/2012)

Added Silicon Revision A8; Removed Modules 6.2 and 6.3.

Rev L Document (11/2013)

Added Silicon Revision A9; Added Modules 6.2 and 11.1; Other minor corrections

Rev M Document (11/2014)

Added module 12, MSSP; Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-63276-774-5

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