PIC16(L)F1933 Silicon Errata and Data Sheet Clarification

The PIC16(L)F1933 family devices that you have received conform functionally to the current Device Data Sheet (DS41575**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1933 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A9**).

Data Sheet clarifications and corrections start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1933 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)								
	DEV<8:0>	Revision ID for Silicon Revision							
		A1	A2	A3	A4	A6	A7	A8	A9
PIC16F1933	10 0011 001	0 0001	0 0010	0 0011	0 0100	0 0110	0 0111	0 1000	0 1001
PIC16LF1933	10 0100 001	0 0001	0 0010	0 0011	0 0100	0 0110	0 0111	0 1000	0 1001

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16F193X/LF193X/PIC16F194X/LF194X/PIC16LF190X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: PIC16F1933 SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)							
				A1	A2	A3	A4	A6	A7	A8	A9
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X							
Data EE Memory	Writes	1.2	Min. VDD for writes.	X	X	X	X	X	X	X	X
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X							
Program Flash Memory (PFM)	Writes	2.2	Min. VDD for writes.	X	X	X	X	X	X	X	X
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X						
Timer1	Timer1 Gate Toggle mode	3.2	T1 Gate flip-flop does not clear.	X	X	X					
Electrical Specifications	RA6/OSC2 Pin Input Leakage Current	4.1	Input leakage current ranges.	X	X	X					
EUSART	16-Bit High-Speed Asynchronous mode	5.1	Works improperly at maximum rate.	X	X	X	X	X	X	X	X
EUSART	Auto-Baud Detect	5.2	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	X	X	X	X	X		
Resets	Power-on Reset (POR)	6.1	Reset under low-power conditions.	X	X						
ADC	ADC Conversion	7.1	ADC conversion may not complete.	X	X	X					
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.1	PWM 0% duty cycle direction change.	X	X	X	X				
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.2	PWM 0% duty cycle port steering.	X	X	X	X				
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	9.1	Bulk Erase not available with LVP.	X	X	X					
LDO	Minimum VDD above 85°C	10.1	Minimum operating VDD for the PIC16F1933 devices at TA > 85°C.	X	X	X	X	X	X	X	X
Oscillator	Oscillator Start-up Timer (OST) bit	12.1	OST bit remains set.	X	X	X	X	X	X	X	
MSSP (Master Synchronous Serial Port)	SPI Master mode	13.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 3: PIC16LF1933 SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]							
				A1	A2	A3	A4	A6	A7	A8	A9
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X							
Data EE Memory	Writes	1.2	Min. VDD for writes.	X	X	X	X	X	X	X	X
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X							
Program Flash Memory (PFM)	Writes	2.2	Min. VDD for writes.	X	X	X	X	X	X	X	X
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X						
Timer1	Timer1 Gate Toggle mode	3.2	T1 Gate flip-flop does not clear.	X	X	X					
Electrical Specifications	RA6/OSC2 Pin Input Leakage Current	4.1	Input leakage current ranges.	X	X	X					
EUSART	16-Bit High-Speed Asynchronous mode	5.1	Works improperly at maximum rate.	X	X	X	X	X	X	X	X
EUSART	Auto-Baud Detect	5.2	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	X	X	X	X	X		
ADC	ADC Conversion	7.1	ADC conversion may not complete.	X	X	X					
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.1	PWM 0% duty cycle direction change.	X	X	X	X				
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	8.2	PWM 0% duty cycle port steering.	X	X	X	X				
In-Circuit Serial Programming™ (ICSP™)	Low-Voltage Programming	9.1	Bulk Erase not available with LVP.	X	X	X					
BOR	Wake-up from Sleep	11.1	Device resets on wake-up from Sleep (PIC16LF1933 device only).	X	X	X	X				
Oscillator	Oscillator Start-up Timer (OST) bit	12.1	OST bit remains set.	X	X	X	X	X	X	X	
MSSP (Master Synchronous Serial Port)	SPI Master mode	13.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A9**).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the Data EE Memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X							

1.2 Data EE Write at Min. VDD

The minimum voltage required for a Data EE write operation is 2.0 volts.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	X

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when VDD is above 3.0 volts.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X							

2.2 Program Flash Memory writes at Min. VDD

The minimum voltage required for a PFM write operation is 2.0V.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	X

3. Module: Timer1

3.1 Timer1 Gate Toggle mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X						

3.2 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X					

4. Module: Electrical Specifications

4.1 RA6/OSC2 Pin Leakage Range

The Input Leakage Currents on the RA6/OSC2 pin are as follows:

Characteristic	Min.	Typ.†	Max.	Units	Conditions	Operating Temperature
RA6/OSC2 Input Leakage Current	—	±5	1500	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at High-Impedance	$-40°C \le T_A \le +85°C$
RA6/OSC2 Input Leakage Current	—	±5	5000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at High-Impedance	$-40°C \le T_A \le +125°C$

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X					

5. Module: EUSART

5.1 16-Bit High-Speed Asynchronous Mode

The EUSART provides unexpected operation when the 16-Bit High-Speed Asynchronous mode is selected and the Baud Rate Generator Data Register values are loaded with zero (0). We do not recommend using this configuration for EUSART communication. The configuration is shown below in the following table:

Configuration Bits			BRG Data Registers	
SYNC	BRG16	BRGH	SPBRGH Value	SPBRGL Value
0	1	1	00000000	00000000

Work around

Ensure that the SPBRGH or the SPBRGL register is loaded with a non-zero value.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	X

5.2 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, see Technical Brief TB3069*, "Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range"*.

EXAMPLE 1: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);                     // if out of spec, use DEFAULT_BAUD
}
   •                                                // if in spec, continue using the
   •                                                // Auto-Baud value in SPBRG
   •
```

EXAMPLE 2: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit

int Average_Baud;                                    // Define Average_Baud variable
int Integrator;                                      // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;                         // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;                        // The running 16 count average
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Check if value is within limits
    SPBRG_16BIT = Average_Baud;                      // If out of spec, use previous average
}
else                                                 // If in spec, calculate the running
{                                                    // average but continue using the
    Integrator+ = SPBRG_16BIT;                       // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X		

6. Module: Resets

6.1 Reset under Low-Power Conditions

This issue pertains to the PIC16F1933 product only. The PIC16LF1933 product is not affected by this issue in any way.

When employing any one of the low-power oscillators, (ECL mode, LP Mode, LFINTOSC, or Timer1 Oscillator) while, at the same time, the source voltage supplied to the VDD pin drops below 2.7 volts, the device will experience a Power-on Reset (POR).

Also, when the source voltage supplied to the VDD pin is below 2.7 volts and a SLEEP instruction is executed, the device will experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are three separate work-arounds available to avoid this Reset condition. Employing any one of these work-arounds will avoid this Reset condition.

- Enabling the Brown-out Reset (BOR) circuitry.
- Enabling the Fixed Voltage Reference (FVR) module.
- Maintaining a source voltage (VDD) to the device above 2.7 volts.

The 'Affected Silicon Revisions' below refers only to PIC16F1933.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X						

7. Module: ADC

7.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

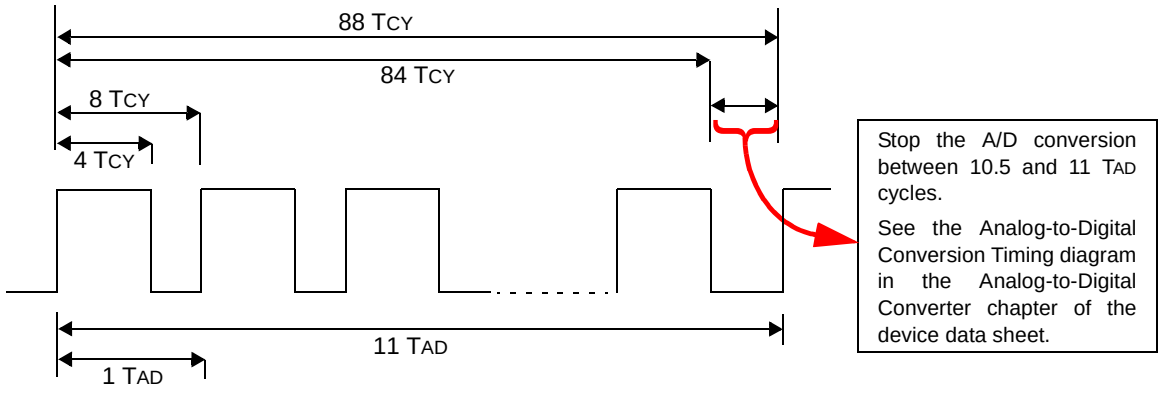
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 4 for the required delay counts for other configurations.

EXAMPLE 3: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 4.

TABLE 4: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X					

8. Module: Enhanced Capture Compare PWM (ECCP)

8.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

On the A4 revision products only, ECCP1 no longer exhibits this problem.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X				

8.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/ disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X				

9. Module: In-Circuit Serial Programming™ (ICSP™)

9.1 Bulk Erase Feature not available with Low-Voltage Programming mode

A bulk erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be over-written with the desired values.

Method 2: Use ICSP High-Voltage Programming mode if a bulk erase is required.

Note: Only the bulk erase feature will erase program or data memory if code or data protection is enabled. Method 2 must be used if code or data protection is enabled.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X					

10. Module: LDO

10.1 Minimum V_{DD} above 85°C

The minimum voltage required for the PIC16F1933 devices is 3.5 volts for temperatures above 85°C.

Note: This issue only applies to the PIC16F1933 devices operating in the Extended temperature range. The PIC16LF1933 devices are not affected.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	X

11. Module: BOR

11.1 BOR Reset

This issue affects only the PIC16LF1933 device. The device may undergo a BOR Reset when waking-up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions and when either SBODEN or BOR_NSLEEP is selected, the devices may occasionally reset when waking-up from Sleep or BOR is enabled.

Work around

Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.

Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.

Method 3: When BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after wake-up:

a. Wake-up event occurs;

b. Turn on FVR (FVREN bit of the FVRCON register);

c. Wait until FVRRDY bit is set;

d. Wait 15 µs after the FVR Ready bit is set;

e. Manually turn on the BOR.

Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:

a. Switch to internal 32 kHz oscillator immediately before Sleep;

b. Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);

c. Manually turn on the BOR;

d. Switch the clock back to the preferred clock source.

Note:	When using the software BOR follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X				

12. Module: Oscillator

12.1 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	

13. Module: MSSP (Master Synchronous Serial Port)

13.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A1	A2	A3	A4	A6	A7	A8	A9
X	X	X	X	X	X	X	X

Data Sheet Clarifications

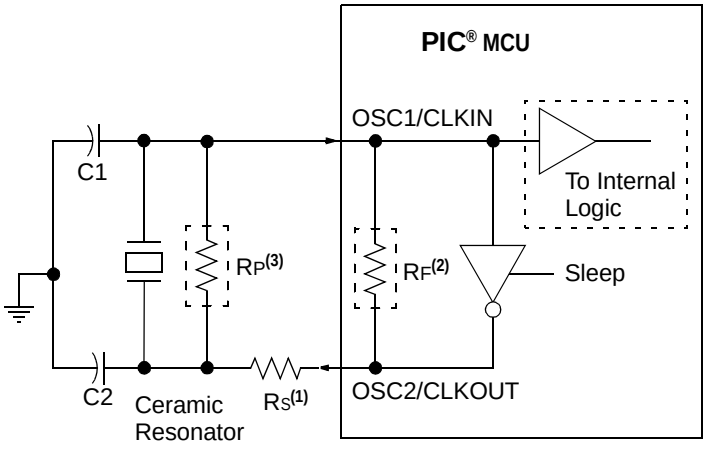
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41575**C**).

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Oscillator Module

In Figure 5-4, note 4 is added as following:

FIGURE 5-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

4: Ceramic resonators with frequencies between 3.0 MHz and 4.0 MHz may require HS mode if operated at temperatures below 0°C.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document.

Rev B Document (02/2010)

Added PIC16F1933 device to this errata; Added Rev. A2 for PIC16F/LF1933 (Table 2); Added Table 3.

Added Module 6 to Silicon Errata Issues section.

Data Sheet Clarifications: Added Modules 1 and 2.

Rev C Document (05/2010)

Added Revision A3 to Tables 1, 2 and 3; Added Modules 7, 8.

Data Sheet Clarifications: Added Modules 3 and 4.

Rev D Document (07/2010)

Added Module 3.2; Revised Module 7.1; Added Module 9.1; Other minor corrections.

Rev E Document (08/2010)

Updated errata to the new format; Revised Table below Module 4.1, changing the Max. values; Updated Table 4; Revised Note above Example 1; Other minor corrections.

Rev F Document (10/2010)

Added Silicon Revision A4; Added Module 10: LDO, to Table 2.

Rev G Document (06/2011)

Added Module 11.1, BOR; Remove Data Sheet Clarifications; Add Rev. A6 Silicon.

Rev H Document (11/2011)

Added Rev. A7 Silicon.

Rev J Document (02/2012)

Updated Table 1; Added Modules 5.2 and 12; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev K Document (03/2012)

Added Silicon Revision A8.

Rev L Document (07/2012)

Added MPLAB X IDE; Removed the Clock Switching module.

Data Sheet Clarifications: Removed Module 1.

Rev M Document (03/2014)

Added Silicon Revision A9.

Rev N Document (05/2014)

Data Sheet Clarifications: Added Module 1.

Rev P Document (12/2014)

Added module 13, MSSP; Other minor corrections.

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