

## High Performance Differential Fanout Buffer

### Features

- 10 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVC MOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range); < 0.02 ps (typ) (differential 156.25MHz, 10kHz to 1MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 1.7ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFN-48 package

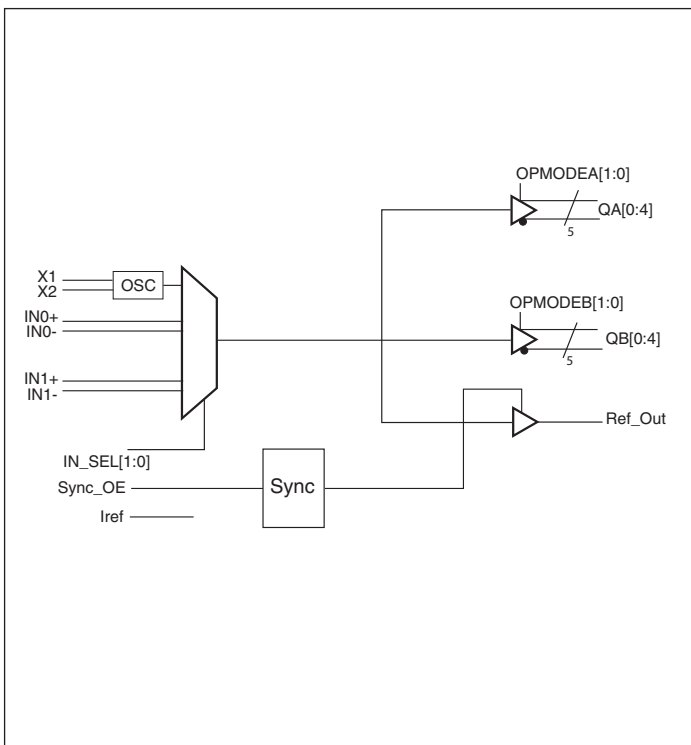
### Description

The PI6C49S1510 is a high performance fanout buffer device which supports up to 1.5GHz frequency. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibilities to users. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

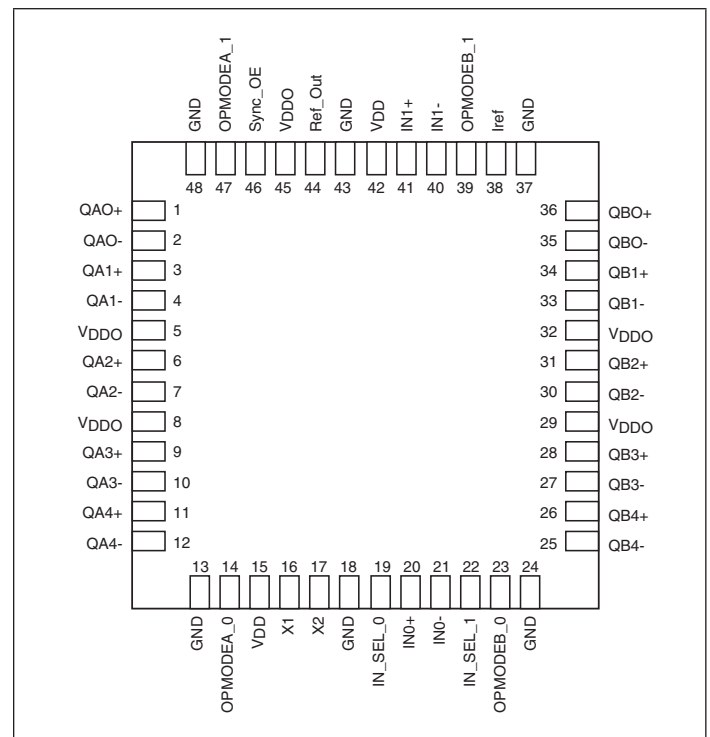
### Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

### Block Diagram



### Pin Configuration (48-Pin TQFN)



**Pinout Table**

Pin #	Pin Name	Type		Description
1,2	QA0+ QA0-	Output		Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3,4	QA1+ QA1-	Output		Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5,8,29,32,45	VDDO	Power		Power supply pins for IO
6,7	QA2+ QA2-	Output		Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
9,10	QA3+ QA3-	Output		Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11,12	QA4+ QA4-	Output		Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13,18,24,37,43,48	GND	Power		Power supply ground
14,47	OPMODEA	Input	Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels
15,42	V <sub>DD</sub>	Power		Power supply pins
16	X1	Input		XTAL input, can also be used as single ended input pin
17	X2	Output		XTAL output. If X1 is used as a single ended input pin, X2 is to be left open
19,22	IN_SEL	Input	Pulldown	Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels.
20	IN0+	Input	Pulldown	Reference input 0
21	IN0-	Input	Pull-up/ Pulldown	Inverted reference input 0, internal bias to V <sub>DD</sub> /2
23,39	OPMODEB	Input	Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels
26,25	QB4+ QB4-	Output		Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
28,27	QB3+ QB3-	Output		Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
31,30	QB2+ QB2-	Output		Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
34,33	QB1+ QB1-	Output		Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.

**Pinout Table (Continued..)**

Pin #	Pin Name	Type		Description
36,35	QB0+	Output		Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB0-			
38	Iref	Output		A fixed precision resistor (475ohm) from this pin to ground provides a reference current for HCSL mode. If LVPECL or LVDS mode chosen, pin can be left open
40	IN1-	Input	Pull-up/ Pulldown	Inverted reference input, internal bias to $V_{DD}/2$
41	IN1+	Input	Pulldown	Reference input 1
44	Ref_Out	Output		Reference output, CMOS
46	Sync_OE	Input	Pulldown	Synchronous output enable for Ref_Out, see Table 3 for functions

**Function Table**

Table 1: Input select function

IN_SEL [1]	IN_SEL [0]	Function
0	0	IN0 is the selected reference input
0	1	IN1 is the selected reference input
1	X	XTAL is the selected input

Table 2: Output Mode select function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3: Reference output enable function

Sync_OE	Ref_Out
0	Hi-Z
1	Output enabled

Table 4: Illegal input level function

Input illegal status	Output status
Input open	Logic Low
Input both high	Logic Low
Input both low	Logic Low

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential ( $V_{DD}$ ).....	-0.5 to +4.6V
Inputs (Referenced to GND) .....	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up .....	200mA
ESD Protection (Input) .....	2000 V min (HBM)
Junction Temperature .....	125 °C max

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Power Supply Characteristics and Operating Conditions**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375		3.465	V
$V_{DDO}$	Output Supply Voltage		2.375		3.465	V
$I_{DD}$	Core Power Supply Current			90	120	mA
$I_{DDO}$	Output Power Supply Current	All LVPECL outputs unloaded		110	145	
		All LVDS outputs loaded		110	125	
		All HCSL outputs unloaded		70	120	
$T_A$	Ambient Operating Temperature		-40		85	°C

**DC Electrical Specifications - Differential Inputs**

Symbol	Parameter		Min.	Typ.	Max.	Units
$I_{IH}$	Input High current	Input = $V_{DD}$			150	uA
$I_{IL}$	Input Low current	Input = GND	-150			uA
$C_{IN}$	Input capacitance			3		PF
$V_{IH}$	Input high voltage				$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage		-0.3			V
$V_{ID}$	Input Differential Amplitude PK-PK		0.15		$V_{DD}-0.85$	V
$V_{CM}$	Common mode input voltage		GND + 0.5		$V_{DD}-0.85$	V
$ISO_{MUX}$	MUX isolation			-89		dBc

### DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High current	Input = V <sub>DD</sub>			150	uA
I <sub>IL</sub>	Input Low current	Input = GND	-150			uA
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> =3.3V	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input low voltage	V <sub>DD</sub> =3.3V	-0.3		0.8	V
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> =2.5V	1.7		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input low voltage	V <sub>DD</sub> =2.5V	-0.3		0.7	V

### DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage		V <sub>DDO</sub> -1.4		V <sub>DDO</sub> -0.9	V
V <sub>OL</sub>	Output Low voltage		V <sub>DDO</sub> -2.1		V <sub>DDO</sub> -1.7	V

### DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage			1.433		V
V <sub>OL</sub>	Output Low voltage			1.064		V
V <sub>ocm</sub>	Output commode voltage			1.25		V
DV <sub>ocm</sub>	Change in V <sub>ocm</sub> between completely output states				50	mV
R <sub>o</sub>	Output impedance		85		140	Ω

### DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage		520		900	mV
V <sub>OL</sub>	Output Low voltage		-150		150	mV

**DC Electrical Specifications – LVCMOS Output**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OH</sub> = 8mA	2.3			V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OH</sub> = 8mA	1.5			V
V <sub>OL</sub>	Output Low voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OL</sub> = -8mA			0.5	V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OL</sub> = -8mA			0.4	V
V <sub>OH</sub>	Output High voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OH</sub> = 24mA	2.1			V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OH</sub> = 16mA	1.5			V
V <sub>OL</sub>	Output Low voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OL</sub> = -24mA			1	V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OL</sub> = -16mA			0.8	V
R <sub>IUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V ± 5%		17		Ω
		V <sub>DDO</sub> = 2.5V ± 5%		22		Ω

**AC Electrical Specifications – Differential Outputs**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units	
F <sub>OUT</sub>	Clock output frequency	LVPECL, LVDS			1500	MHz	
		HCSL			250		
T <sub>r</sub>	Output rise time	From 20% to 80%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	350		550	
T <sub>f</sub>	Output fall time	From 80% to 20%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	350		550	
T <sub>ODC</sub>	Output duty cycle	Frequency<650MHz	LVPECL, HCSL	48		52	%
			LVDS	47		53	
V <sub>PP</sub>	Output swing Single-ended	LVPECL outputs @ <1GHz	500		1000	mV	
		LVPECL outputs @ >1GHz	400				
		LVDS outputs	250		500		
T <sub>j</sub>	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz		0.03		ps	
		156.25MHz, 10kHz to 1MHz		0.02		ps	
V <sub>CROSS</sub>	Absolute crossing voltage	HCSL		460		mV	
DV <sub>CROSS</sub>	Total variation of crossing voltage	HCSL			140	mV	
T <sub>SK</sub>	Output Skew	10 outputs devices, outputs in same tank, with same load, at DUT.		40	70	ps	
T <sub>PD</sub>	Propagation Delay	LVPECL, LVDS @ 3.3V, 100MHz		1650		ps	
		HCSL @ 3.3V, 100MHz		2000		ps	

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T <sub>OD</sub>	Valid to HiZ			200	ns
T <sub>OE</sub>	HiZ to valid			200	ns
T <sub>P2P Skew</sub>	Part to Part Skew <sup>1</sup>		200		ps

**Notes:**

1. This parameter is guaranteed by design

**AC Electrical Specifications – CMOS**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Ref_Out frequency	XTAL input	10		50	MHz
		Reference input			200	MHz
T <sub>j</sub>	Buffer additive jitter RMS	XTAL input		0.3		ps
		Reference input		0.03		ps
t <sub>r</sub> / t <sub>f</sub>	Rise time, Fall time	C <sub>L</sub> = 10pF		1.5		ns
T <sub>ODC</sub>	Output duty cycle	C <sub>L</sub> = 10pF	45		55	%
t <sub>PD</sub>	Propagation delay	3.3V, 25MHz		2700		ps
t <sub>S</sub>	Setup time		300			ps
t <sub>SOD</sub>	Clock edge to output disable	Ref_Out	2		4	cycles
t <sub>SOE</sub>	Clock edge to output enable	Ref_Out	2		4	cycles

**Crystal Characteristics**

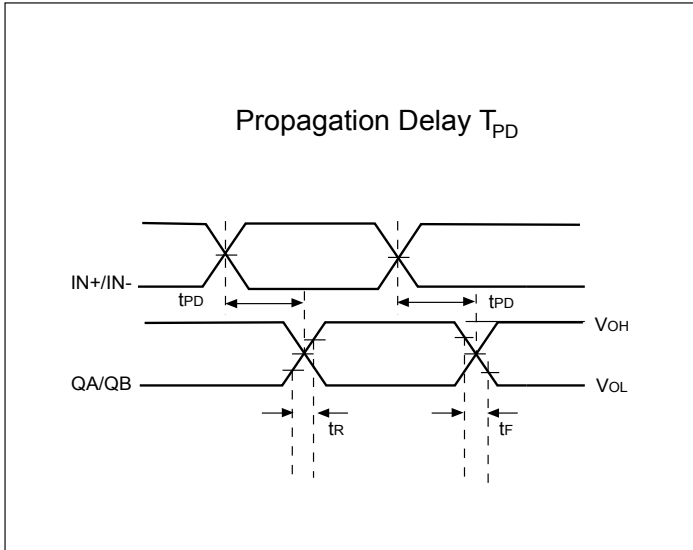
Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	10		50	MHz
Equivalent Series Resistance (ESR)			70	Ω
Shunt Capacitance			7	pF
Load Capacitance	10		18	pF
Drive Level			500	μW

**Recommended Crystals**

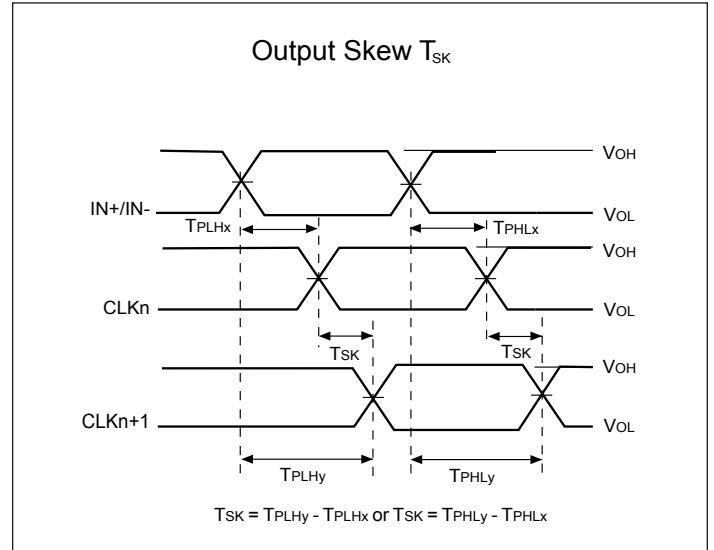
Pericom recommends:

- GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
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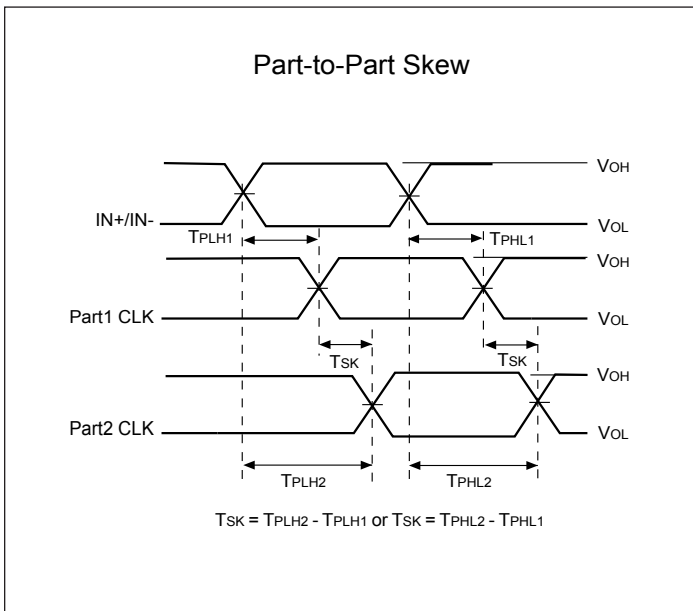
**Propagation Delay**



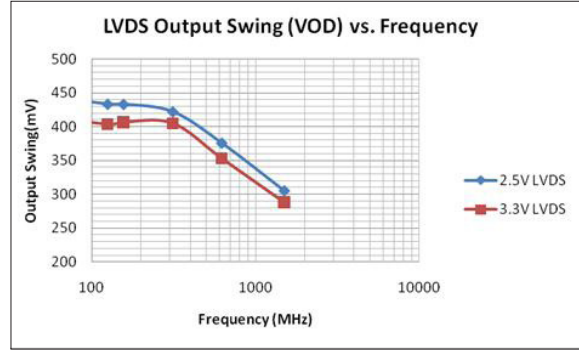
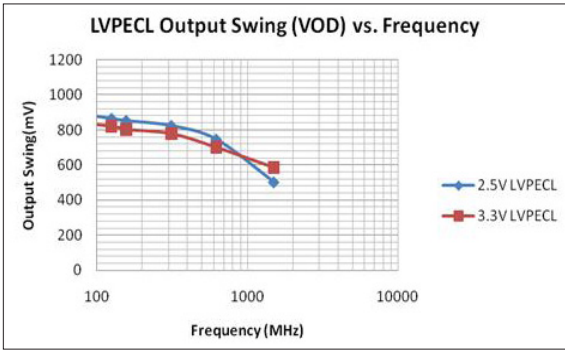
**Output Skew**



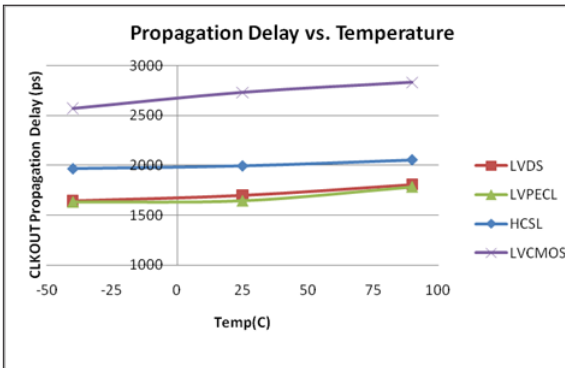
**Part to Part Skew**



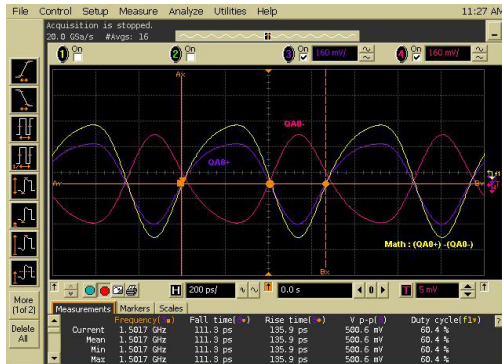
**LVPECL/ LVDS Output Swing vs. Frequency**



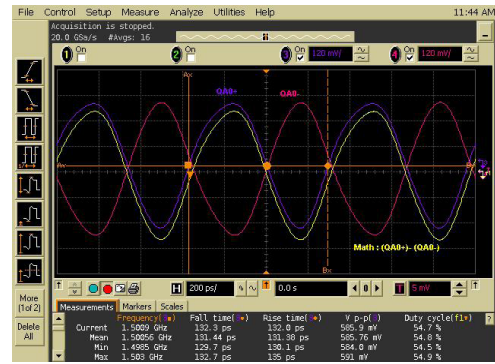
**Propagation Delay vs. Temperature**



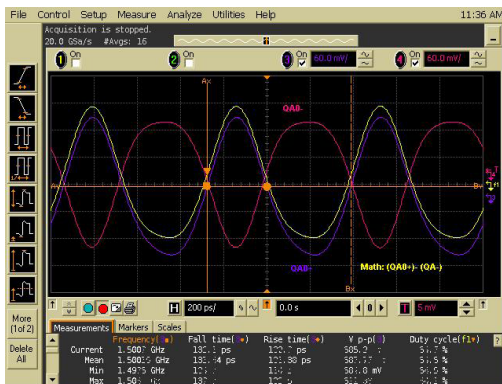
**1.5GHz LVPECL/ LVDS Waveform**



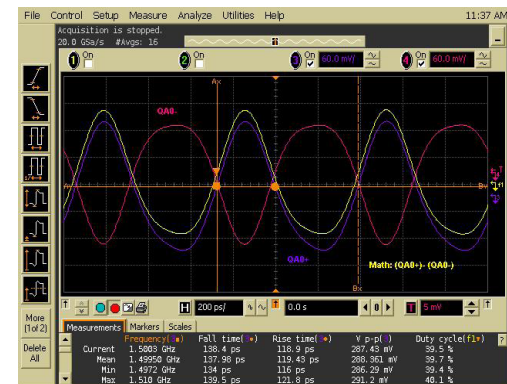
**2.5V LVPECL Waveform**



**3.3V LVPECL Waveform**



**2.5V LVDS Waveform**

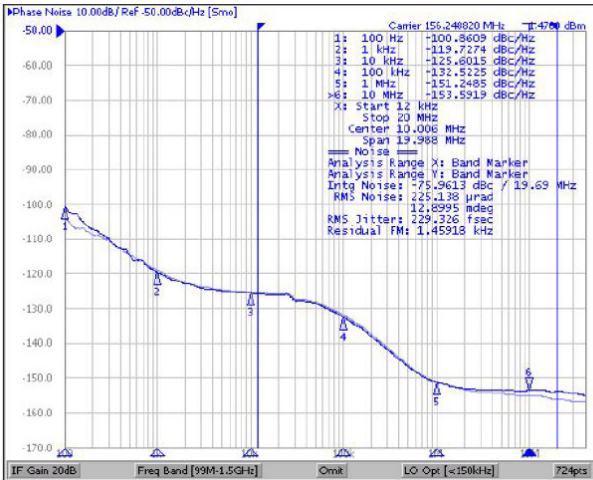


**3.3V LVDS Waveform**

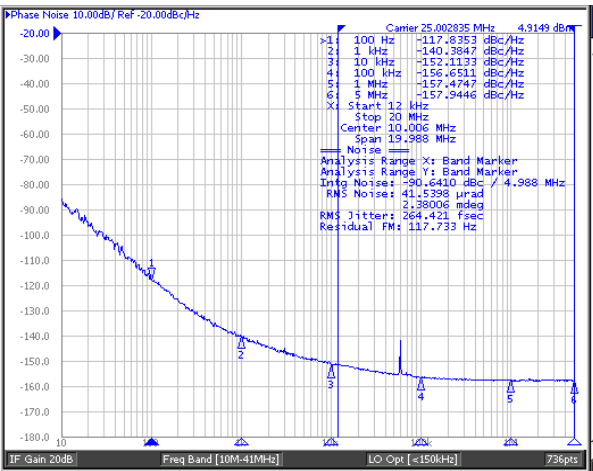
**Phase Noise and Additive Jitter**

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

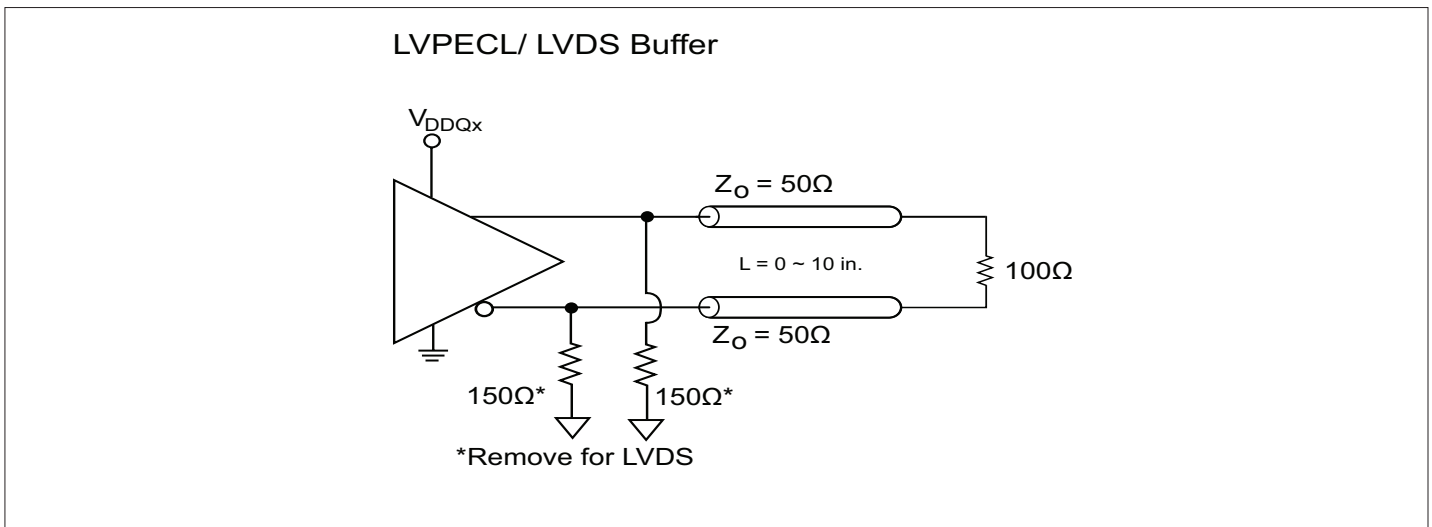
Additive jitter is calculated at 156.25MHz~27fs RMS (12kHz to 20MHz). Additive jitter =  $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



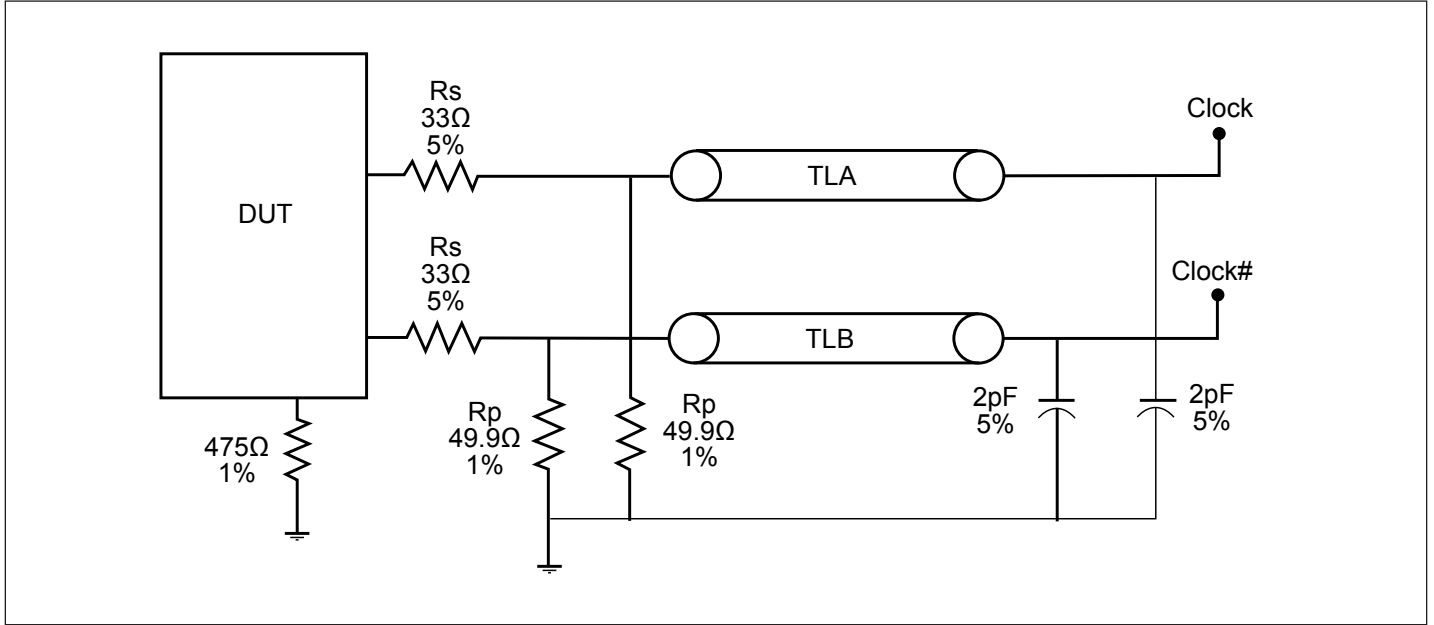
**Total phase jitter with 25MHz XTAL ~ 264fs RMS (12kHz ~20MHz)**



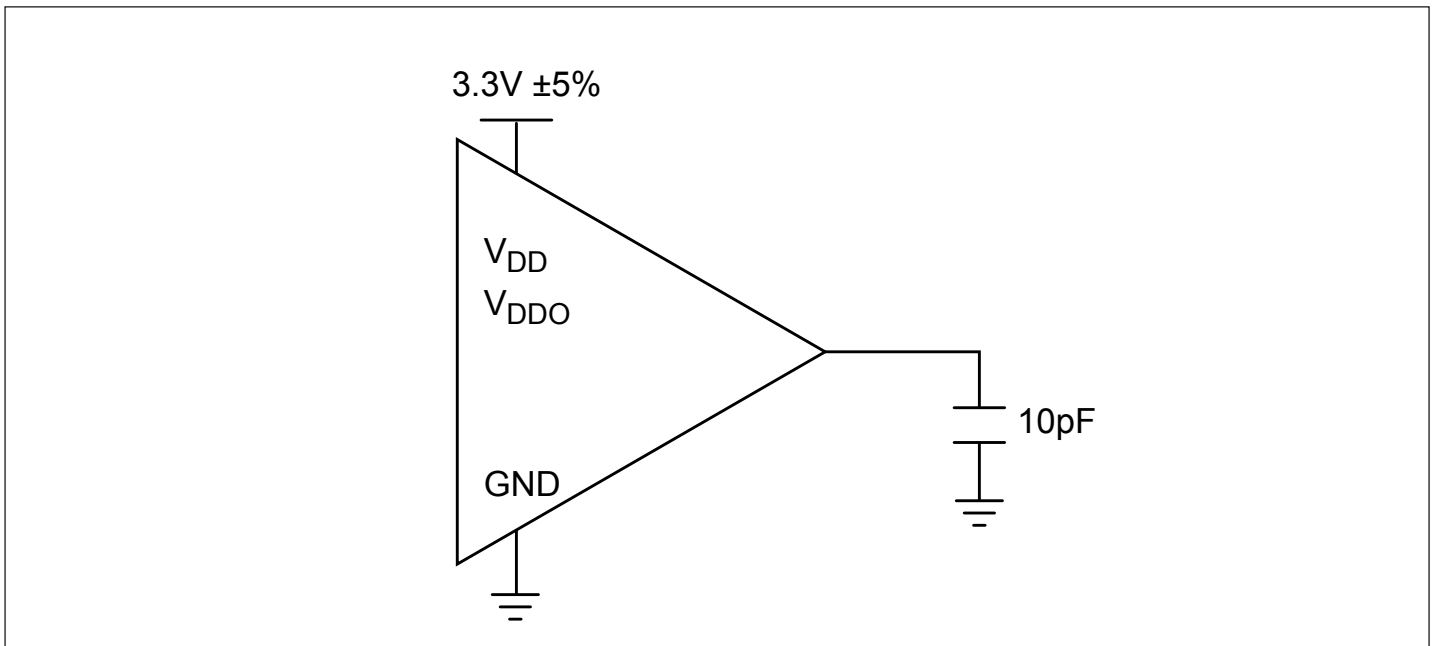
**Configuration Test Load Board Termination for LVPECL/ LVDS Outputs**



**Configuration Test Load Board Termination for HCSL Outputs**



**Configuration Test Load Board Termination for LVCMOS Outputs**



## Application Information

### Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .

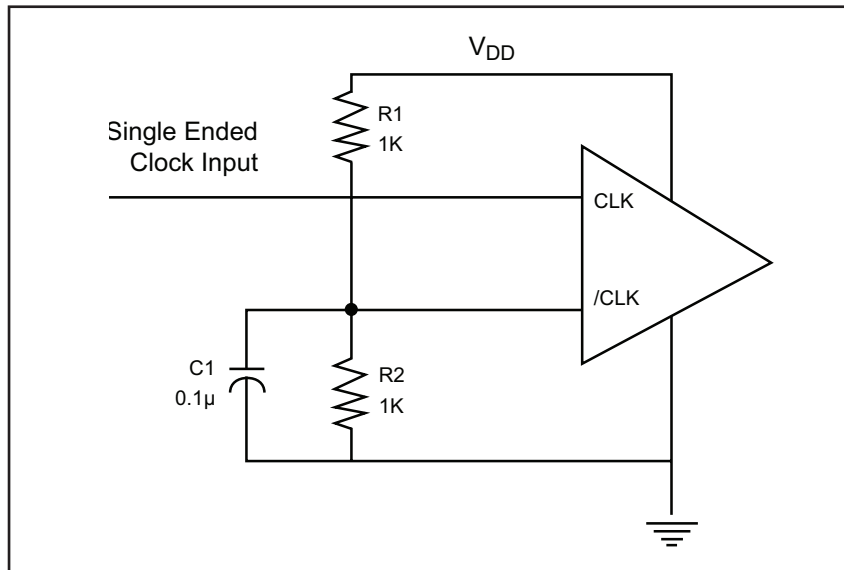
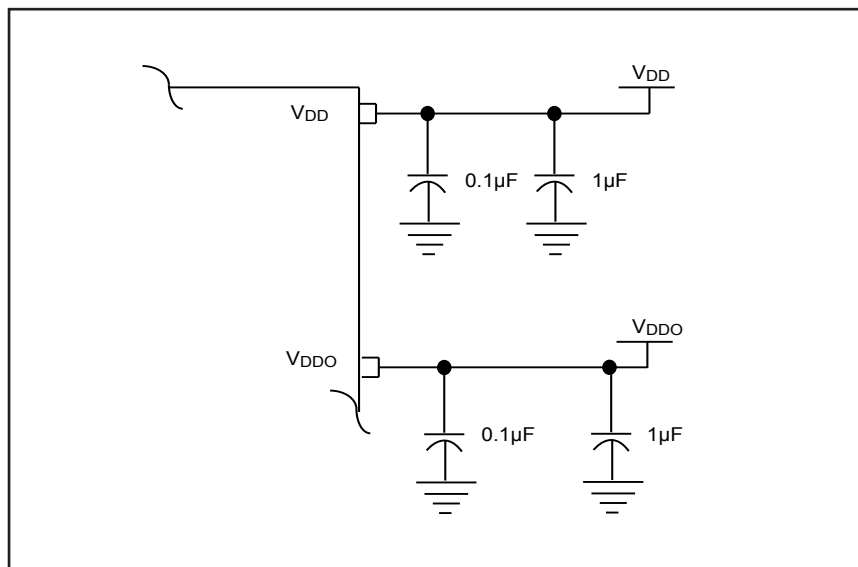


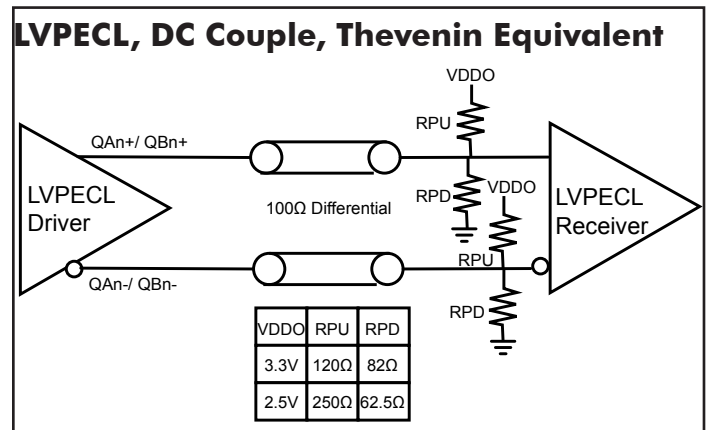
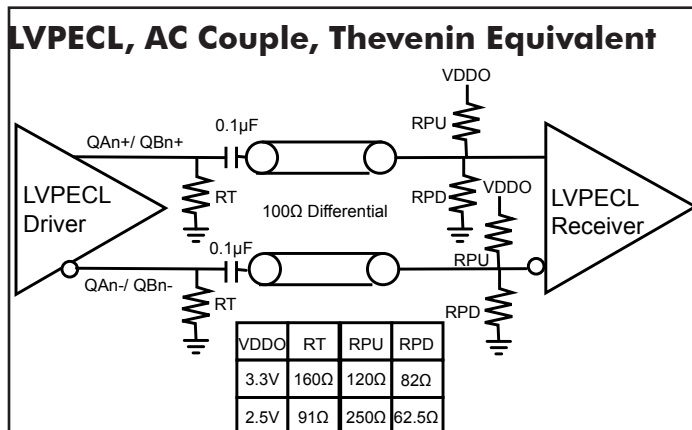
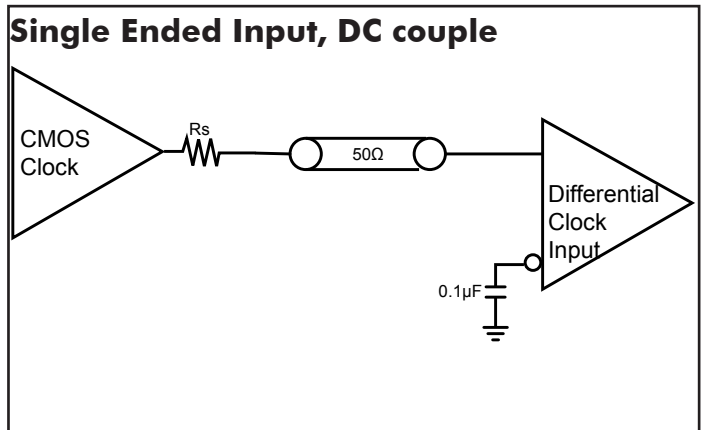
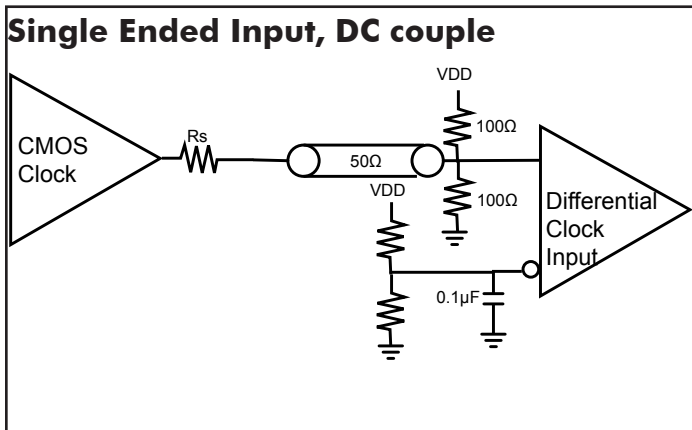
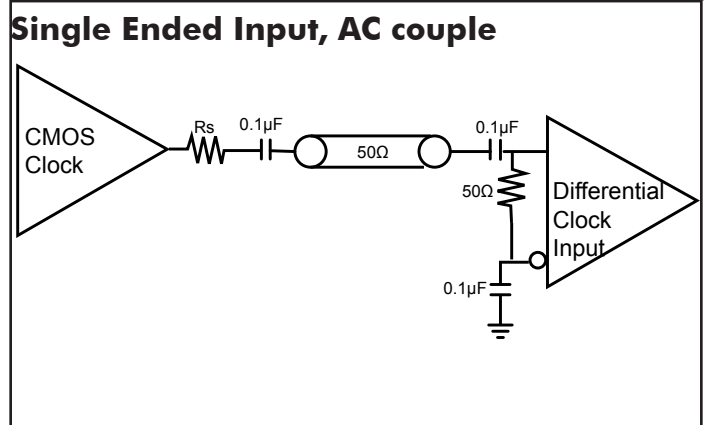
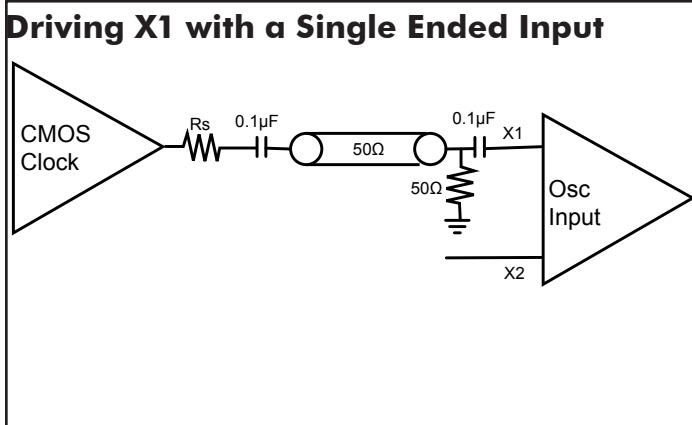
Figure 1. Single-ended input to Differential input device

## Power Supply Filtering Techniques

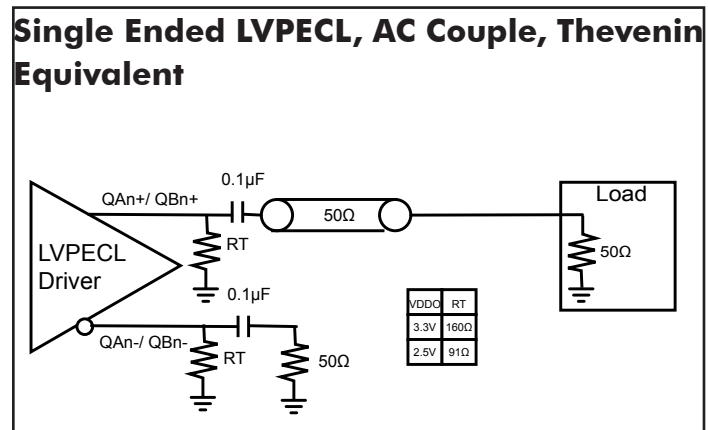
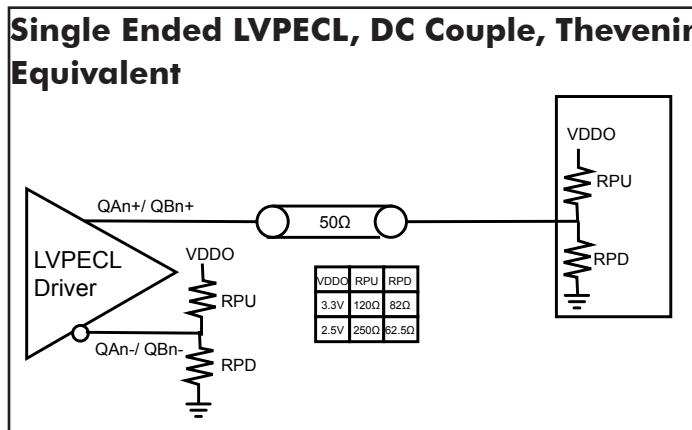
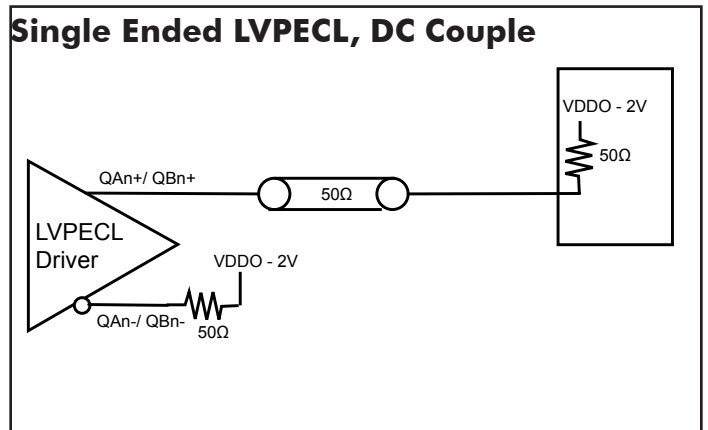
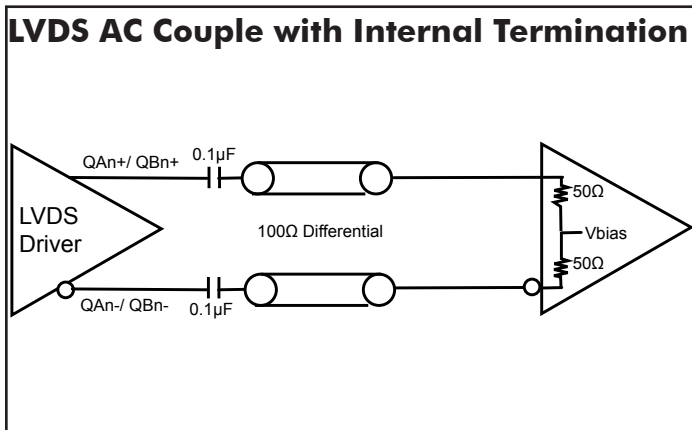
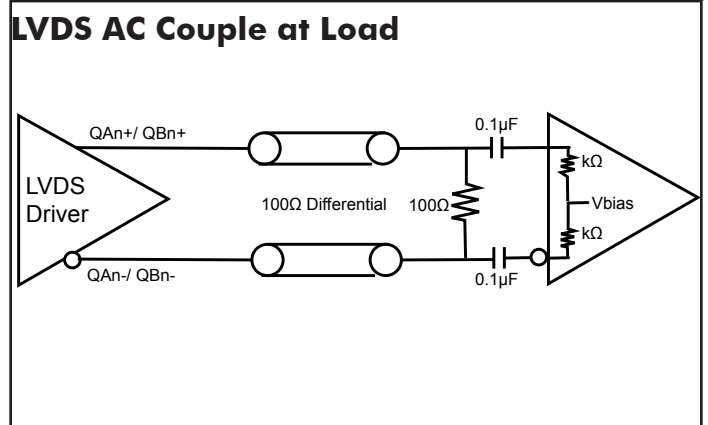
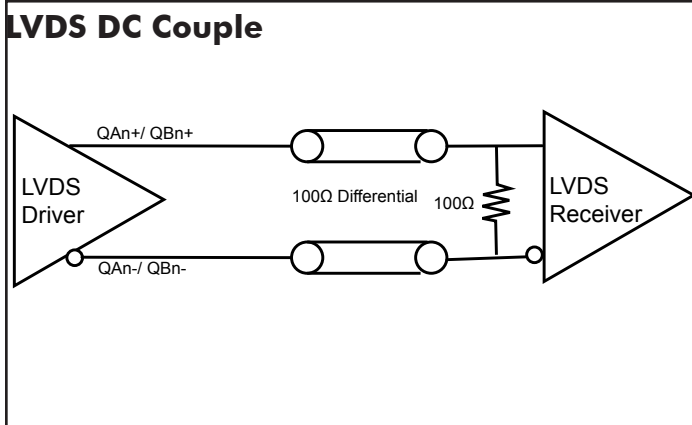
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF and 1µF bypass capacitors should be used for each pin.



**PI6C49S1510**

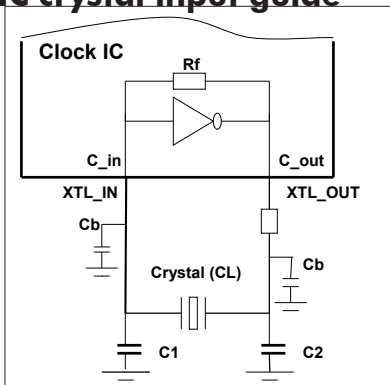


**PI6C49S1510**



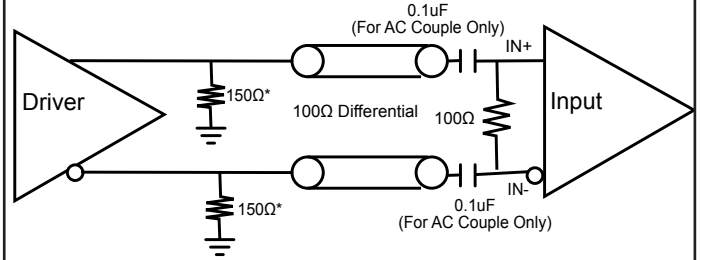
**PI6C49S1510**

**Clock IC crystal input guide**

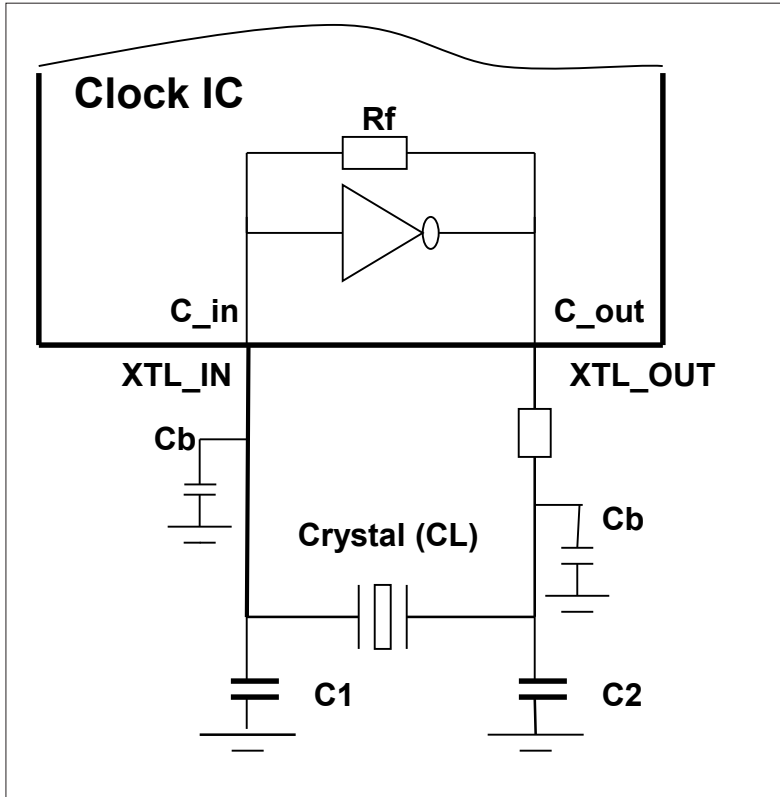


**LVPECL/ LVDS AC and DC input**

\*Remove for LVDS



**Clock IC Crystal loading cap. design guide**



CL =crystal spec. loading cap.

C\_in/out = (3~5pF) of IC pin cap.

Cb = PCB trace (2~4pF)

C1,C2 = load cap. of design

Rd = 50 to 100ohm drive level limit

Design guide:  $C1=C2=2 *CL - (Cb +C_{in/out})$  to meet target +/-ppm < 20 ppm

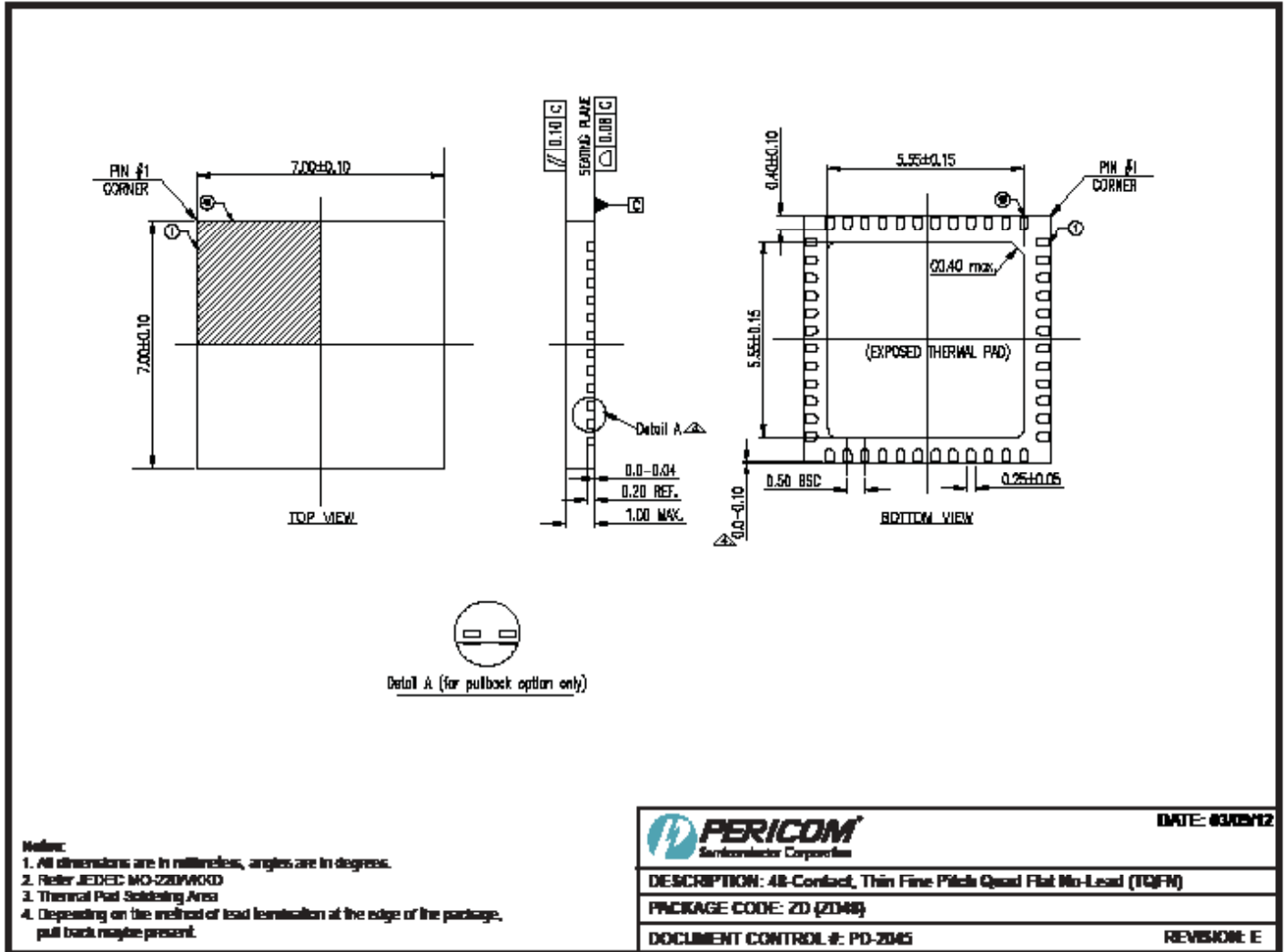
Example1: Select CL=18 pF crystal,  $C1=C2=2*(18pF) - (4pF+5pF)=27pF$ , check datasheet too

Example2: For higher frequency crystal ( $\Rightarrow 20MHz$ ), can use formula  $C1=C2=2*(CL-6)$ , can do fine tune of C1, C2 for more accurate ppm if necessary

**Thermal Information**

Symbol	Description	Condition	
$\Theta_{JA}$	Junction-to-ambient thermal resistance	Still air	23.65 °C/W
$\Theta_{JC}$	Junction-to-case thermal resistance		9.10 °C/W

**Packaging Mechanical: 48-Pin TQFN (ZD)**



**Ordering Information**

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1510ZDIE	ZD	Pb-free & Green, 48-pin TQFN	-40 °C to 85 °C
PI6C49S1510ZDIEX	ZD	Pb-free & Green, 48-pin TQFN, Tape & Reel	-40 °C to 85 °C

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and Reel packaging

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View PI6C49S1510ZDIEX on WIN SOURCE](#)

 [Diodes Incorporated](#) Information

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