



# THE DATASHEET OF 4027BCP



# MC14027B

## Dual J-K Flip-Flop

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

### Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design
- Logic State is Retained Indefinitely with Clock Level Either High or Low; Information is Transferred to the Output Only on the Positive-Going Edge of the Clock Pulse
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

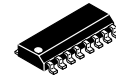
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



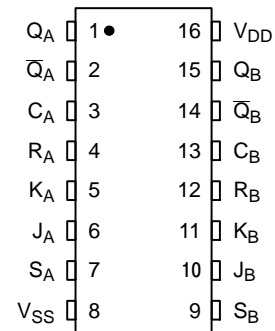
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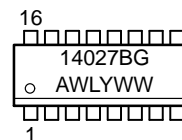


SOIC-16  
D SUFFIX  
CASE 751B

### PIN ASSIGNMENT



### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY, Y = Year  
WW = Work Week  
G = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14027B

## TRUTH TABLE

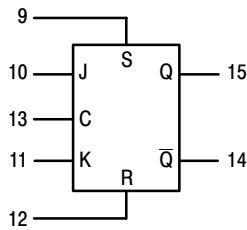
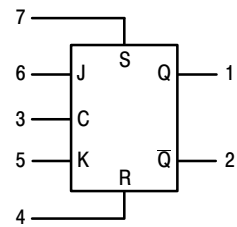
Inputs					Outputs*		
C†	J	K	S	R	Q <sub>n</sub> ‡	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
↗	1	X	0	0	0	1	0
↗	X	0	0	0	1	1	0
↗	0	X	0	0	0	0	1
↗	X	1	0	0	1	0	1
↗	1	1	0	0	Q <sub>0</sub>	Q̄ <sub>0</sub>	Q <sub>0</sub>
↘	X	X	0	0	X	Q <sub>n</sub>	Q̄ <sub>n</sub>
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = Don't Care  
† = Level Change

‡ = Present State  
\* = Next State

No  
Change

## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

## ORDERING INFORMATION

Device	Package	Shipping†
MC14027BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14027BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14027BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14027BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	“0” Level V <sub>OL</sub>	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	“1” Level V <sub>OH</sub>	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	“0” Level V <sub>IL</sub>	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“1” Level V <sub>IH</sub>	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I <sub>in</sub>	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>							μAdc
10	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>									
15	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>									

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> – V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

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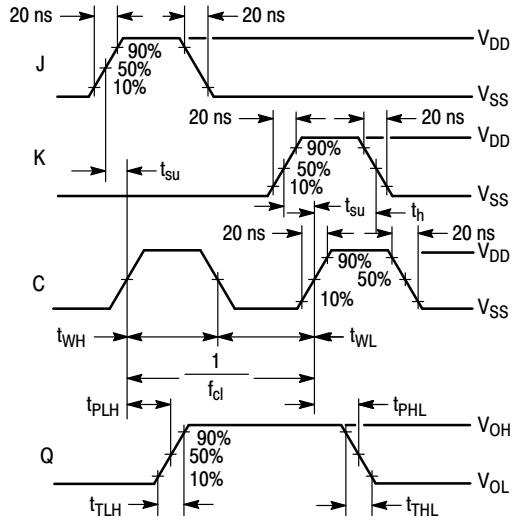
## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Times** Clock to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Set to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Reset to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	– – –  – – –  – – –	175 75 50  175 75 50  350 100 75	350 150 100  350 150 100  450 200 150	ns
Setup Times	$t_{su}$	5.0 10 15	140 50 35	70 25 17	– – –	ns
Hold Times	$t_h$	5.0 10 15	140 50 35	70 25 17	– – –	ns
Clock Pulse Width	$t_{WH}, t_{WL}$	5.0 10 15	330 110 75	165 55 38	– – –	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	– – –	3.0 9.0 13	1.5 4.5 6.5	MHz
Clock Pulse Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	– – –	– – –	15 5.0 4.0	$\mu\text{s}$
Removal Times  Set  Reset	$t_{rem}$	5 10 15  5 10 15	90 45 35  50 25 20	10 5 3  –30 –15 –10	– – –  – – –	ns
Set and Reset Pulse Width	$t_{WH}$	5.0 10 15	250 100 70	125 50 35	– – –	ns

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

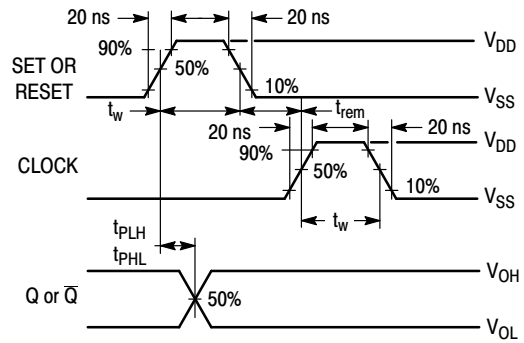
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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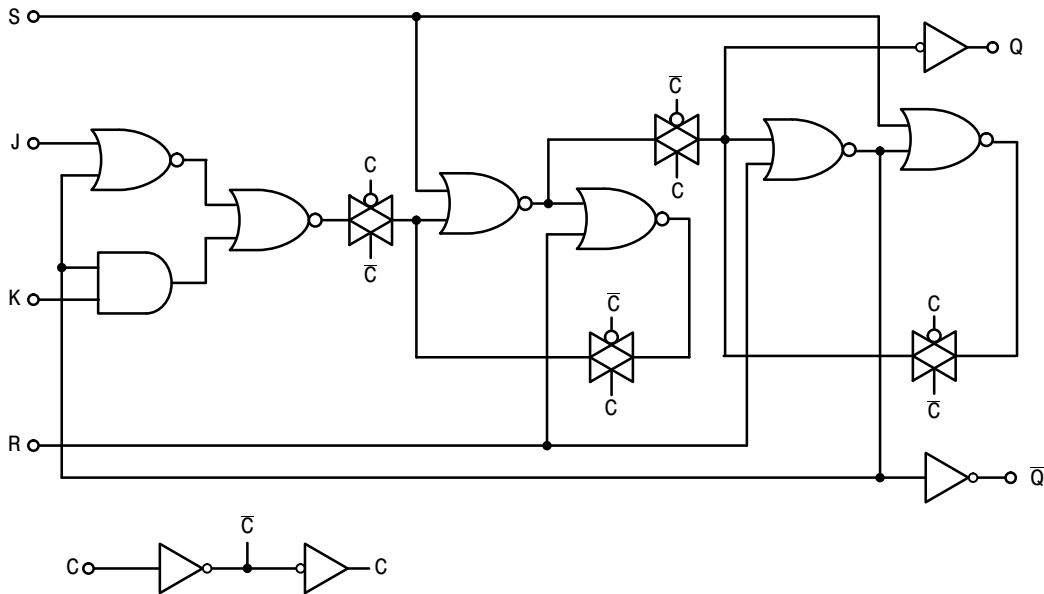
Inputs R and S low.  
 For the measurement of  $t_{WH}$ ,  $t_{WL}$ ,  $f_{cl}$ , and  $P_D$   
 the Inputs J and K are kept high.

**Figure 1. Dynamic Signal Waveforms (J, K, Clock, and Output)**



**Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)**

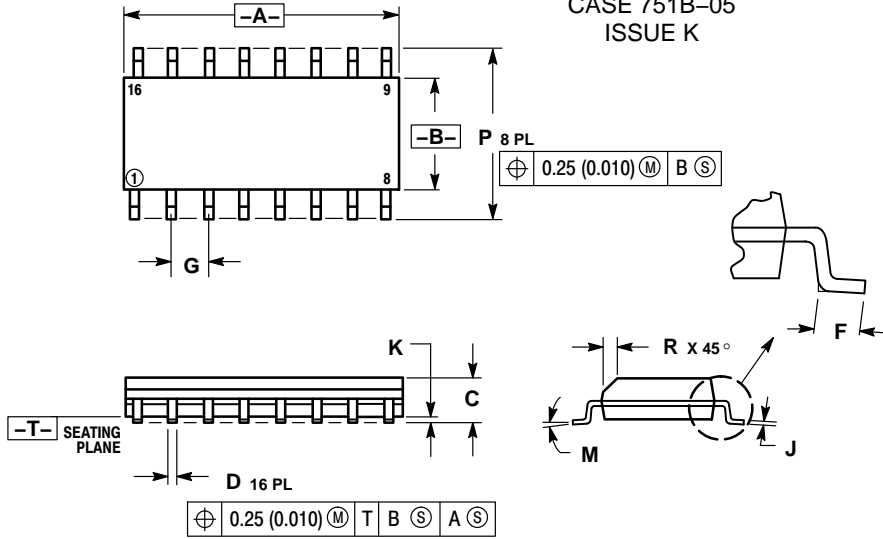
## LOGIC DIAGRAM (1/2 of Device Shown)



# MC14027B

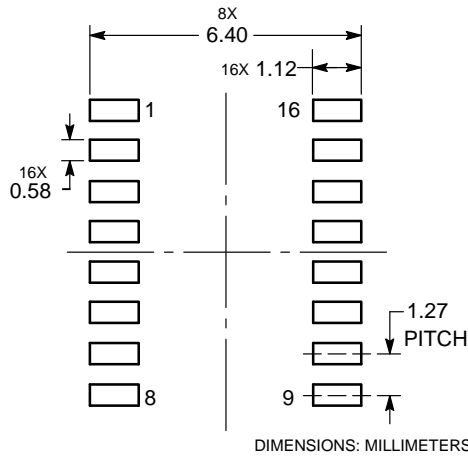
## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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