THE DATASHEET OF

PI2EQX3201BLZFEX

PI2EQX3201BL

3.0Gbps 2 Differential Channel SATA *i/m* ReDriver™ with Equalization, De-emphasis and OOB

Features

- SATA2 *i/m*, extended SATA2
- Two Pairs of 3.0Gbps differential signal
- Adjustable Transmitter Emphasis & Amplitude
- Adjustable Receiver Equalization
- 100-Ohm Differential CML I/O's
- Input signal level detect and squelch for each channel
- Low Power (100mW per Channel)
- Stand-by Mode – Power Down State
- V_{DD} Operating Range: 1.5V to 1.8V
- Packaging (Pb-free & Green):
  — 36-pad TQFN (ZF36)

Description

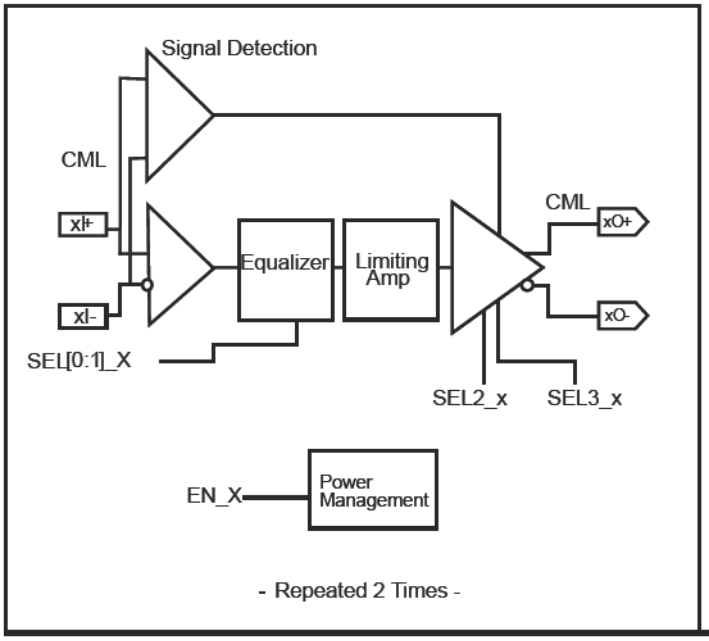
Pericom Semiconductor's PI2EQX3201BL is a low power, signal ReDriver. The device provides programmable equalization, amplification, and de-emphasis by using 4 select bits, SEL[0:3], to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX3201BL supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the re-driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the re-driver.

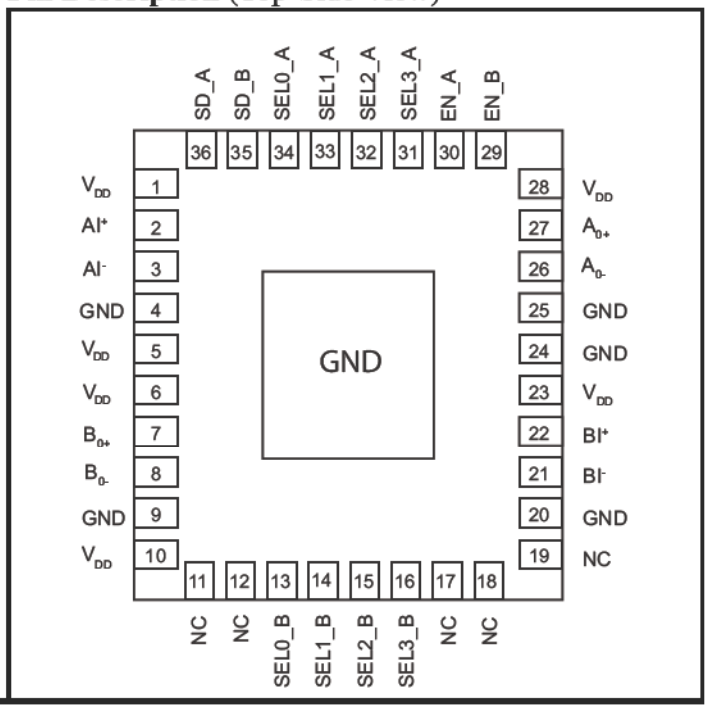
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channels input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to providing signal re-conditioning, Pericom's PI2EQX3201BL also provides power management Stand-by mode operated by a Bus Enable pin.

Block Diagram



Pin Description (Top-Side View)



Pin Description

Pin #	Pin Name	I/O	Description
2 3	AI+ AI-	I	CML Input Channel A with internal 50-Ohm pull down
27 26	AO+ AO-	O	CML Output Channel A internal 50-Ohm pull up. Drives to output common mode voltage when input is $<V_{TH-}$.
22 21	BI+ BI-	I	CML Input Channel B with internal 50-Ohm pull down
7 8	BO+ BO-	O	CML Output Channel B with internal 50-Ohm pull up. Drives to output common mode voltage when input is $<V_{TH-}$.
30 29	EN_A EN_B	I	EN_[A:B] is the enable pin. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode.
4, 9, 20, 24, 25, Center Pad	GND	PWR	Supply Ground
11, 12, 17, 18, 19	NC	-	No Connect
36 35	SD_A SD_B	O	Signal Detect, output for channels A and B. Provides a LVCMOS high output when a valid input signal is detected. When low, SD_X indicates that the input signal level is below the signal detect threshold level.
34 33	SEL0_A SEL1_A	I	Selection pins for equalizer (see Amplifier Configuration Table) w/ 25K-Ohm internal pull up
13 14	SEL0_B SEL1_B	I	
32	SEL2_A	I	Selection pins for amplifier (see Amplifier Configuration Table) w/ 25K-Ohm internal pull up
15	SEL2_B	I	
31	SEL3_A	I	Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 25K-Ohm internal pull up
16	SEL3_B	I	
1, 5, 6, 10, 23, 28	V_{DD}	PWR	1.5 to 1.8V Supply Voltage (±0.1V)

Output Swing Control

SEL2_[A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL3_[A:B]	De-emphasis
0	0dB
1	-3.5dB

Equalizer Selection

SEL0_[A:B]	SEL1_[A:B]	Compliance Channel @ 1.5GHz
0	0	no equalization
0	1	1.5dB ± 1.0dB
1	0	3.5dB ± 1.0dB
1	1	5.5dB ± 1.0dB

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	-40 to +85°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.4 to 1.9V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current				90	mA
$P_{standby}$	Power, standby	EN_[A:B] = 0			1	mW
$P_{active18}$	Power, active @ 1.8V	V_{DD}=1.8V, EN_[A:B] = 1, $V_{rx\text{-}diff\text{-}p} \geq V_{th\text{-}sd}$		125	160	mW
P_{idle18}	Power, idle @ 1.8V	V_{DD}=1.8V, EN_[A:B] = 1, $V_{rx\text{-}diff\text{-}p} < V_{th\text{-}sd}$		100		mW
$P_{active15}$	Power, active @ 1.5V	V_{DD}=1.5V, EN_[A:B] = 1, $V_{rx\text{-}diff\text{-}p} \geq V_{th\text{-}sd}$		100	130	mW
P_{idle15}	Power, idle @ 1.5V	V_{DD}=1.5V, EN_[A:B] = 1, $V_{rx\text{-}diff\text{-}p} < V_{th\text{-}sd}$		80		mW
t_{pd}	Latency	From differential input to differential output		2.0		ns
CML Receiver Input						
RL_{RX}	Return Loss	50 MHz to 1.25 GHz		12		dB
$V_{RX\text{-}DIFFP\text{-}P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX\text{-}CM\text{-}ACP}$	AC Peak Common Mode Input Voltage				150	mV
$V_{TH–SD}$	Signal Detect Threshold	EN_X = High	50		200	
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance		80	100	120	Ohm
$Z_{RX\text{-}DC}$	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.

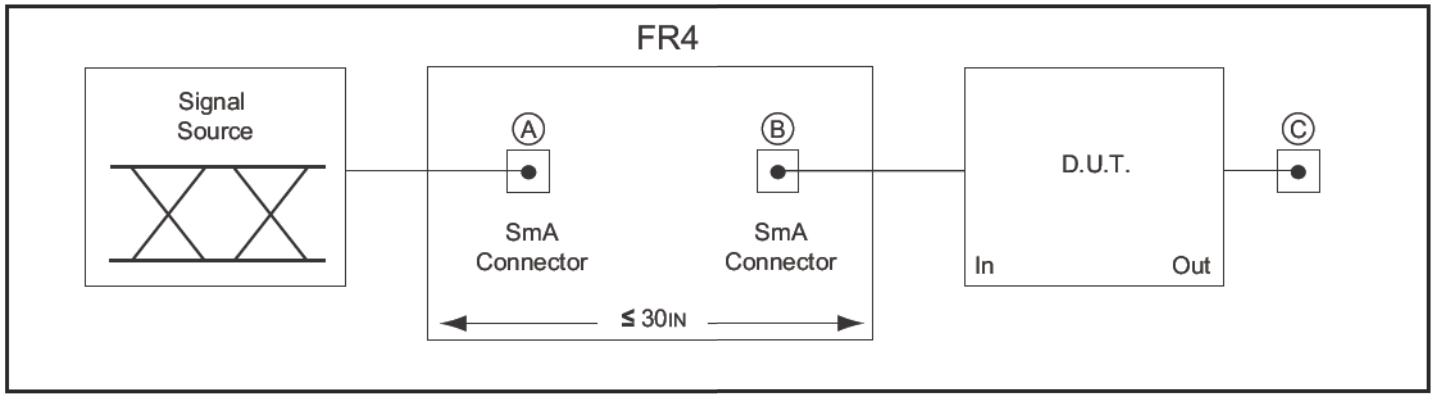


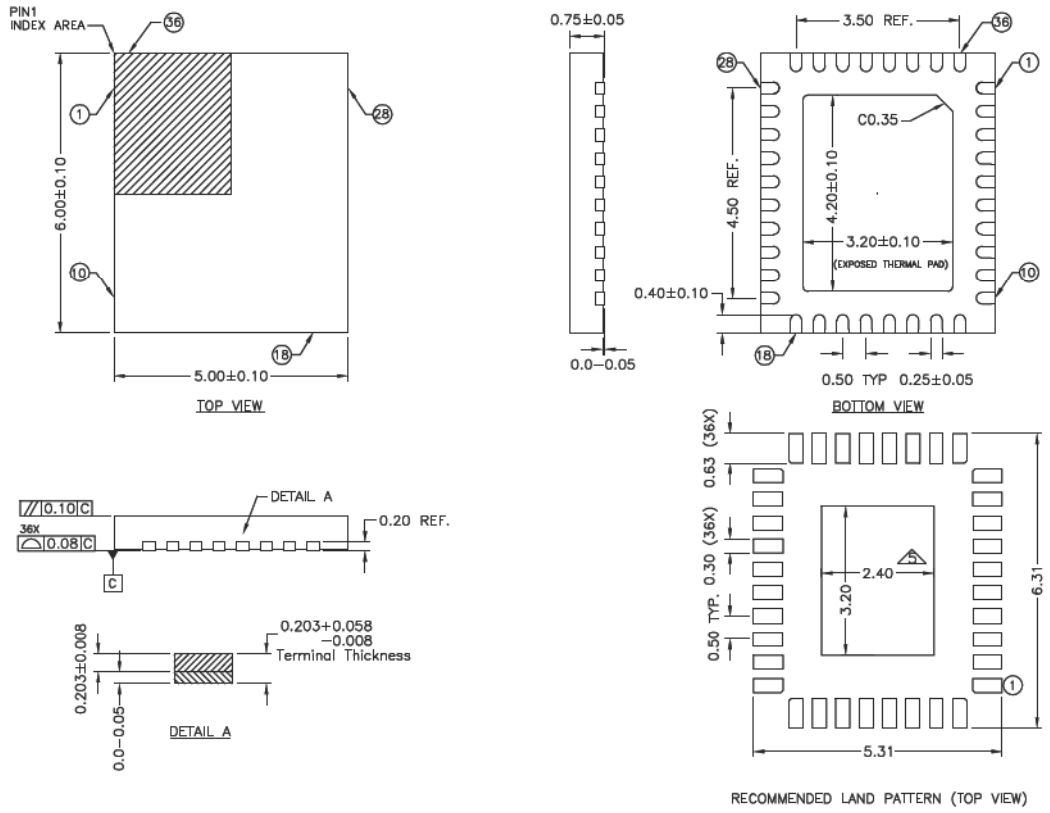
Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (V_{DD} = 1.4V to 1.9V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ohm differential)						
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage $V_{TX-DIFFP-P} = 2 * \|V_{TX-D+} - V_{TX-D-}\|$	SEL2_x = 0	400		600	p-p
		SEL2_x = 1	480		720	
V_{TX-C}	Common-Mode Voltage $\| V_{TX-D+} + V_{TX-D-} \| / 2$			V_{DD}-0.3		
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ohm
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				5	µA
I_{IL}	Input Low Current				100	
V_{OH}	DC Voltage Output High	I_{OH} = 4mA	V_{DD} - 0.4			V
V_{OL}	DC Voltage Output Low	I_{OL} = -4mA			0.4	V

Note:
1. Using K28.7 (0011111000) pattern)
2. The parameter is determined by device characterization, and is not production tested

Packaging Mechanical: 36-pad TQFN (ZF36)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM® Enabling Serial Connectivity — DATE: 03/10/09

DESCRIPTION: 36-contact, Very Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZF (ZF36)

DOCUMENT CONTROL #: PD-2023 REVISION: C

09-0143

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3201BLZFE	ZF	Pb-Free and Green 36-pad TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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