

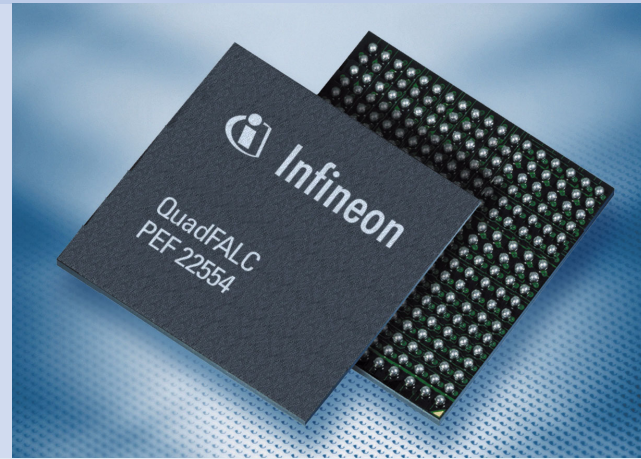


**THE DATASHEET OF  
PEF22554E V2.1-G**



# QuadFALC®

Four-channel E1/T1/J1 Framer and Line Interface Component  
PEF 22554



The QuadFALC® is an addition to Infineon's market leading FALC® family of advanced E1/T1/J1 Framer And Line Interface Unit (LIU) components. As a four port E1/T1/J1 framer and line interface unit (LIU), QuadFALC is optimized for a range of network equipment including Radio network Controllers, Node B line cards, PBX or SDH/SONET ADMs.

The QuadFALC features a unique clock generation unit that accepts any reference clock between 1.02 and 20 MHz as well as integrated analog switches for impedance matching or protection switching. Using industry leading QuadFALC Evaluation support tools, system developers can shorten design cycles while creating a wide range of highly flexible, low BOM E1/T1/J1 line cards.

## Applications

- Wireless base stations
- Router
- Multi-service access platforms,
- Digital loop carriers
- Remote access servers/concentrators
- SONET/SDH Add/Drop multiplexers

## Analog Line Interfaces

- Four independent E1/T1/J1 long haul/short haul line interface units
- Software programmable T1/E1/J1
- Integrated analog switch for impedance matching (E1-75/120, T1-100, J1-110) and protection switching (only PG-LBGA-160 package)
- Crystal-less wander and jitter attenuation/compensation according to TR 62411 and ETS-TBR 12/13
- Clock generation unit accepts any frequency reference clock from 1.02 MHz to 20 MHz
- Programmable transmit pulse shape for flexible pulse generation
- Receiver sensitivity exceeds -36 dB@772 kHz and -43 dB@1024 kHz
- Clock signal generation & extraction according to ITU-T G.703 Sec. 13

## Frame Aligners

- ITU-T G.704 frame alignment/synthesis for 2.048/1.544 Mbit/s

- Programmable frame formats
  - E1: Double- & CRC Multi-frame
  - T1: F4, F12 (D4), Ext. Super Frame (ESF), F72 (SLC96)
- Detects and generates LOS, AIS and RAI alarms
- CRC-4 performance monitoring
- PRBS generation and monitoring
- Detects & generates LOS, AIS & RAI alarms
- System bus data rate scalable from 1.544 Mbit/s up to 16 Mbit/s
- Synchronization Supply Message (SSM) generation and extraction

## HDLC Controllers

- 12 HDLC controllers (three per channel) including 128-byte deep FIFO buffers each
- CAS controller with micro-processor or system interface serial access
- Supports signaling system #7
- ANSI T1.403 Bit-Oriented Messages (BOM), generates periodical performance reports

## General Features

- Software and pin compatible to previous QuadFALC versions
- Intel® or Motorola® type 8/16-bit microprocessor interface
- Serial SPI bus and serial SCI bus slave interfaces
- Low power operation (150mW / channel typical)
- Dual voltage 1.8 V/3.3 V or single voltage 3.3 V power supply
- PG-LBGA-160, 15x15 mm with 1.0 mm ball pitch
- PG-TQFP-144, 20x20 mm, 0,5 mm pitch
- -40°C to +85°C operation
- Rohs compliant packages

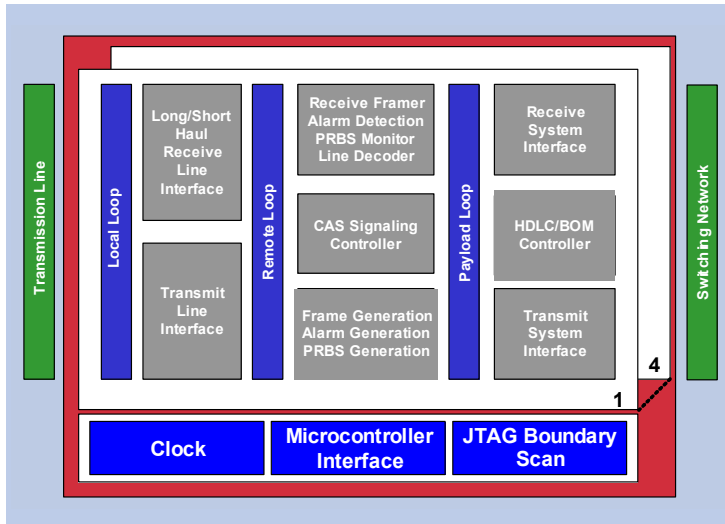
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COMMUNICATION

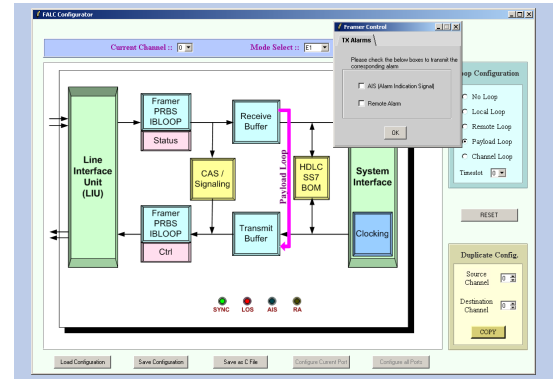


Never stop thinking.

## QuadFALC PEF 22554 Block Diagram

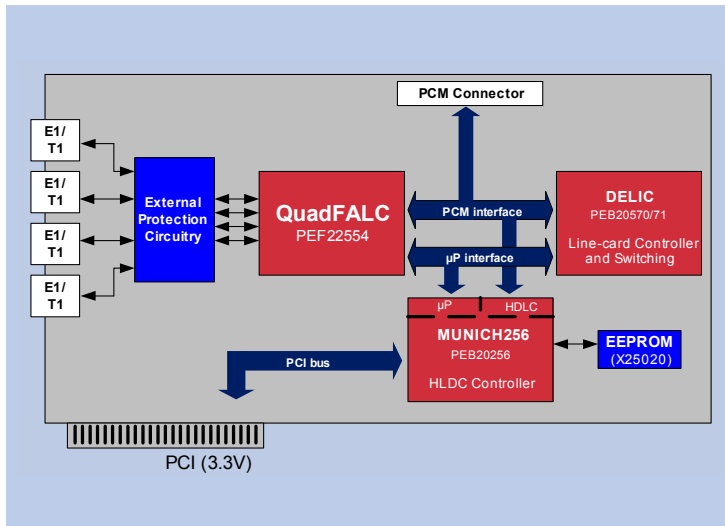


## Configuration Assistant Tool



The FALC Configuration Assistant supports the user during design phase. All QuadFALC functional blocks can be configured by a GUI supporting the low level API driver.

## System Application - VoIP Primary Access Board



## Documentation and Support Package

- Data Sheet
- Application Notes
- Hardware Evaluation System EASY 22554 with Schematics and Layout information
- WinEASY Software for MS Windows 98SE/NT/2000/XP CD-ROM Support Package
- Support Software (portable low level API driver)
- Configuration Assistant for rapid porting of device configuration to customer designs.
- Analog front end calculator
- Flexible master clocking calculator

## Product Summary

Type	Description	Package
PEF 22554 HT	QuadFALC	PG-TQFP-144
PEF 22554 E	QuadFALC	PG-LBGA-160

How to reach us:

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