



**THE DATASHEET OF
PCM1793DBR**





24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-Bit Resolution
- Analog Performance:
 - Dynamic Range: 113 dB
 - THD+N: 0.001%
 - Full-Scale Output: 2.1 V rms (at Postamplifier)
- Differential Voltage Output: 3.2 V p-p
- 8× Oversampling Digital Filter:
 - Stop-Band Attenuation: –82 dB
 - Pass-Band Ripple: ± 0.002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect
- Accepts 16-, 20-, and 24-Bit Audio Data
- Data Formats: Standard, I²S, and Left-Justified
- Digital De-Emphasis
- Soft Mute
- Zero Flags for Each Output
- Dual Supply Operation:
 - 5-V Analog, 3.3-V Digital

- 5-V Tolerant Digital Inputs
- Small 28-Lead SSOP Package, Lead-Free Product

APPLICATIONS

- A/V Receivers
- DVD Players
- Musical Instruments
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 24-Bit Audio

DESCRIPTION

The PCM1793 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1793 provides balanced voltage outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1793DB	28-lead SSOP	28DB	-25°C to 85°C	PCM1793	PCM1793DB	Tube
					PCM1793DBR	Tape and reel

ABSOLUTE MAXIMUM RATINGSover operating free-air temperature range unless otherwise noted⁽¹⁾

		PCM1793
Supply voltage	V _{CCF} , V _{CCL} , V _{CCC} , V _{CCR}	-0.3 V to 6.5 V
	V _{DD}	-0.3 V to 4 V
Supply voltage differences: V _{CCF} , V _{CCL} , V _{CCC} , V _{CCR}		±0.1 V
Ground voltage differences: AGNDF, AGNDL, AGNDC, AGNDR, DGND		±0.1 V
Digital input voltage	LRCK, DATA, BCK, SCK, DEMP0, DEMP1, FMT0, FMT1, FMT2, RST, MUTE	-0.3 V to 6.5 V
	ZEROL, ZEROR	-0.3 V to (V _{DD} + 0.3 V) < 4 V
Analog input voltage		-0.3 V to (V _{CC} + 0.3 V) < 6.5 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		-40°C to 125°C
Storage temperature		-55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICSall specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1793DB			UNIT
		MIN	TYP	MAX	
RESOLUTION			24		Bits
DATA FORMAT					
	Audio data interface format		Standard, I ² S, left justified		
	Audio data bit length		16-, 20-, 24-bit selectable		
	Audio data format		MSB first, 2s complement		
f _S	Sampling frequency		10	200	kHz
	System clock frequency		128, 192, 256, 384, 512, 768 f _S		
DIGITAL INPUT/OUTPUT					
	Logic family		TTL compatible		
V _{IH}	Input logic level		2		VDC
V _{IL}			0.8		
I _{IH}	Input logic current	V _{IN} = V _{DD}	10		μA
I _{IL}		V _{IN} = 0 V	-10		
V _{OH}	Output logic level	I _{OH} = -2 mA	2.4		VDC
V _{OL}		I _{OL} = 2 mA	0.4		

ELECTRICAL CHARACTERISTICS (Continued)

 all specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, and 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1793DB			UNIT
		MIN	TYP	MAX	
DYNAMIC PERFORMANCE (1)					
THD+N at $V_{OUT} = 0\text{ dB}$	$f_S = 44.1\text{ kHz}$		0.001%	0.002%	
	$f_S = 96\text{ kHz}$		0.0015%		
	$f_S = 192\text{ kHz}$		0.003%		
Dynamic range	EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$	110	113		dB
	EIAJ, A-weighted, $f_S = 96\text{ kHz}$		113		
	EIAJ, A-weighted, $f_S = 192\text{ kHz}$		113		
Signal-to-noise ratio	EIAJ, A-weighted, $f_S = 44.1\text{ kHz}$	110	113		dB
	EIAJ, A-weighted, $f_S = 96\text{ kHz}$		113		
	EIAJ, A-weighted, $f_S = 192\text{ kHz}$		113		
Channel separation	$f_S = 44.1\text{ kHz}$	106	110		dB
	$f_S = 96\text{ kHz}$		110		
	$f_S = 192\text{ kHz}$		109		
Level linearity error	$V_{OUT} = -120\text{ dB}$		± 1		dB
ANALOG OUTPUT					
Gain error		-8	± 3	8	% of FSR
Gain mismatch, channel-to-channel		-3	± 0.5	3	% of FSR
Bipolar zero error	At BPZ	-2	± 0.5	2	% of FSR
Differential output voltage (2)	Full scale (0 dB)		3.2		V p-p
Bipolar zero voltage (2)	At BPZ		1.4		V
Load impedance (2)	$R_1 = R_2$	1.7			k Ω
DIGITAL FILTER PERFORMANCE					
De-emphasis error				± 0.1	dB
Pass band	$\pm 0.002\text{ dB}$			$0.454 f_S$	
	-3 dB			$0.49 f_S$	
Stop band		$0.546 f_S$			
Pass-band ripple				± 0.002	dB
Stop-band attenuation	Stop band = $0.546 f_S$	-75			dB
	Stop band = $0.567 f_S$	-82			dB
Delay time			$29/f_S$		s

(1) Dynamic performance and DC accuracy are specified at the output of the postamplifier as shown in Figure 28. Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode. At all sampling frequency operations, measurement bandwidth is limited with a 20-kHz AES17 filter.

(2) These parameters are defined at the PCM1793 output pin. Load impedance, R1 and R2, are input resistors of the postamplifier. These are defined as dc loads.

ELECTRICAL CHARACTERISTICS (Continued)

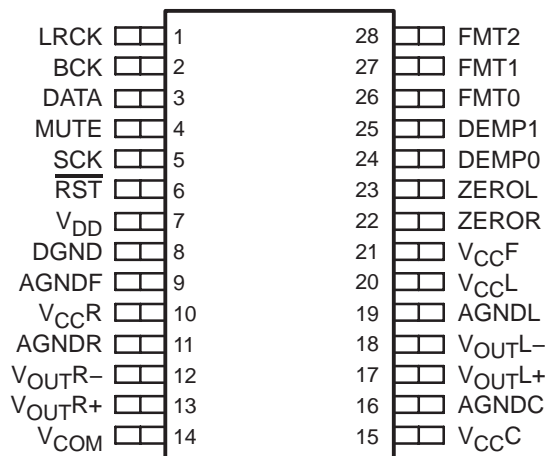
all specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, and 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1793DB			UNIT	
		MIN	TYP	MAX		
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
V_{CC}			4.5	5	5.5	
I_{DD}	Supply current (1)	$f_S = 44.1\text{ kHz}$		6.5	8	mA
		$f_S = 96\text{ kHz}$		13.5		
		$f_S = 192\text{ kHz}$		28		
I_{CC}	Supply current (1)	$f_S = 44.1\text{ kHz}$		14	16	mA
		$f_S = 96\text{ kHz}$		15		
		$f_S = 192\text{ kHz}$		16		
Power dissipation (1)		$f_S = 44.1\text{ kHz}$		90	110	mW
		$f_S = 96\text{ kHz}$		120		
		$f_S = 192\text{ kHz}$		170		
TEMPERATURE RANGE						
Operation temperature			-25		85	$^\circ\text{C}$
θ_{JA}	Thermal resistance	28-pin SSOP		100		$^\circ\text{C/W}$

(1) Input is BPZ data.

PIN ASSIGNMENTS

PCM1793
(TOP VIEW)

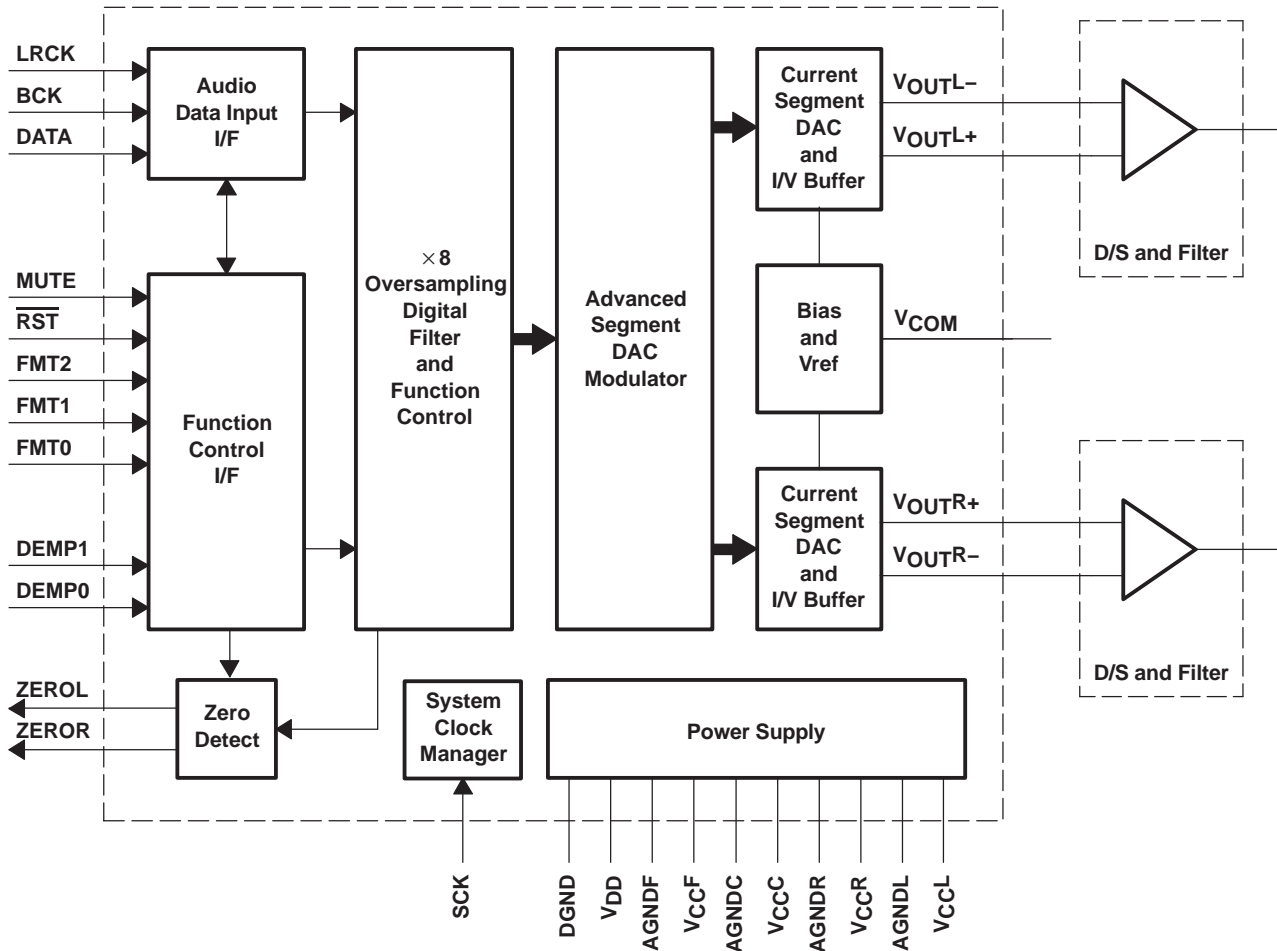


Terminal Functions

TERMINAL		I/O	DESCRIPTIONS
NAME	PIN		
AGNDC	16	–	Analog ground (internal bias and current DAC)
AGNDF	9	–	Analog ground (DACFF)
AGNDL	19	–	Analog ground (L-channel I/V)
AGNDR	11	–	Analog ground (R-channel I/V)
BCK	2	I	Bit clock input ⁽¹⁾
DATA	3	I	Serial audio data input ⁽¹⁾
DEMP0	24	I	De-emphasis control 0 ⁽¹⁾
DEMP1	25	I	De-emphasis control 1 ⁽¹⁾
DGND	8	–	Digital ground
FMT0	26	I	Audio data format select 0 ⁽¹⁾
FMT1	27	I	Audio data format select 1 ⁽¹⁾
FMT2	28	I	Audio data format select 2 ⁽¹⁾
LRCK	1	I	Left and right clock (f _S) input ⁽¹⁾
MUTE	4	I	Analog output mute control ⁽¹⁾
$\overline{\text{RST}}$	6	I	Reset ⁽¹⁾
SCK	5	I	System clock input ⁽¹⁾
V _{CC} C	15	–	Analog power supply (internal bias and current DAC), 5 V
V _{CC} F	21	–	Analog power supply (DACFF), 5 V
V _{CC} L	20	–	Analog power supply (L-channel I/V), 5 V
V _{CC} R	10	–	Analog power supply (R-channel I/V), 5 V
V _{COM}	14	–	Internal bias decoupling pin
V _{DD}	7	–	Digital power supply, 3.3 V
V _{OUT} L+	17	O	L-channel analog voltage output +
V _{OUT} L–	18	O	L-channel analog voltage output –
V _{OUT} R+	13	O	R-channel analog voltage output +
V _{OUT} R–	12	O	R-channel analog voltage output –
ZEROL	23	O	Zero flag for L-channel
ZEROR	22	O	Zero flag for R-channel

⁽¹⁾ Schmitt-trigger input, 5-V tolerant

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

Digital Filter Response

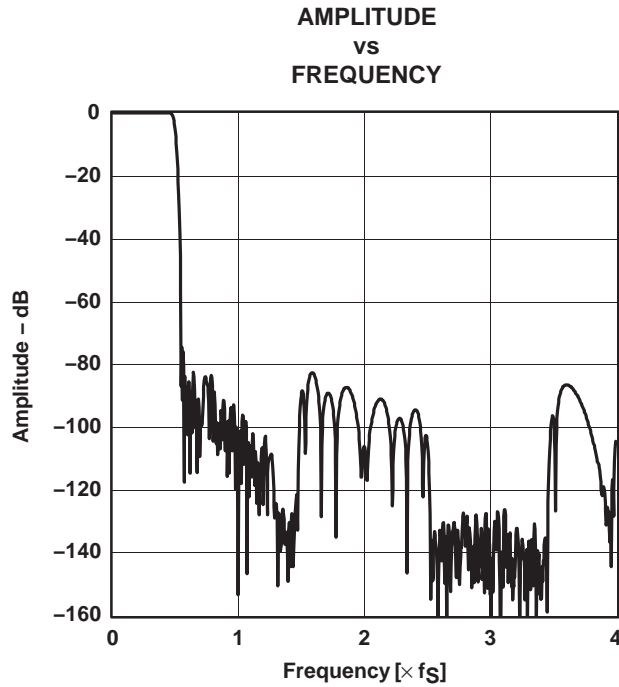


Figure 1. Frequency Response, Sharp Rolloff

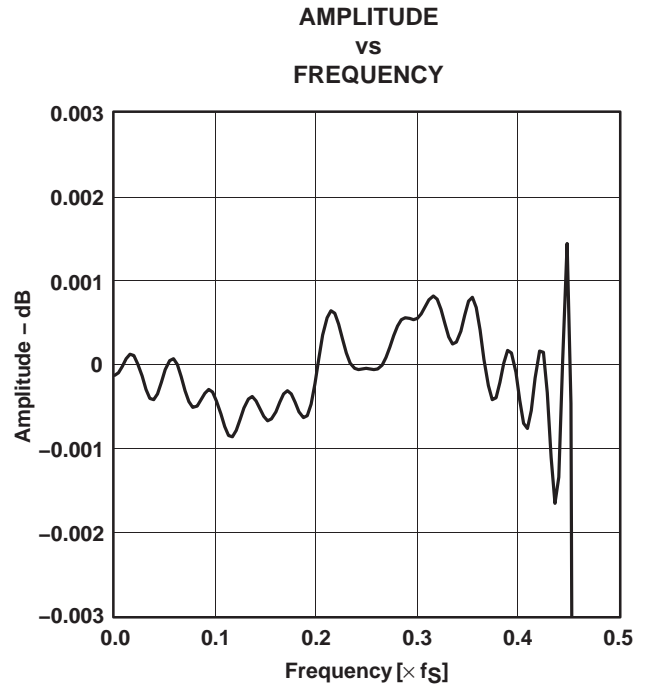


Figure 2. Pass-Band Ripple, Sharp Rolloff

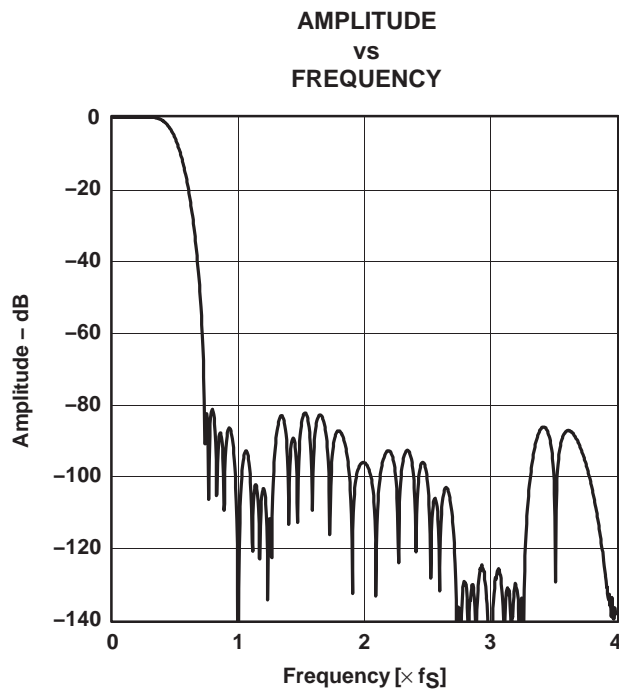


Figure 3. Frequency Response, Slow Rolloff

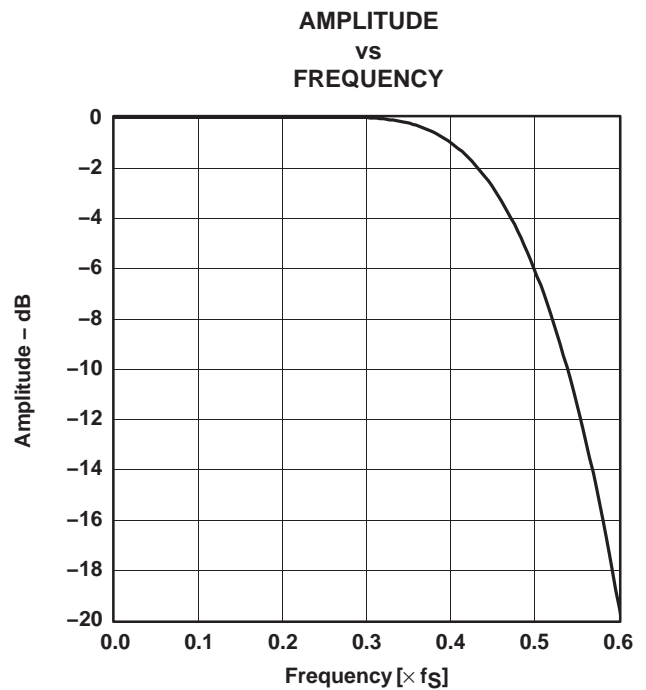


Figure 4. Transition Characteristics, Slow Rolloff

De-Emphasis Filter

DE-EMPHASIS LEVEL
VS
FREQUENCY

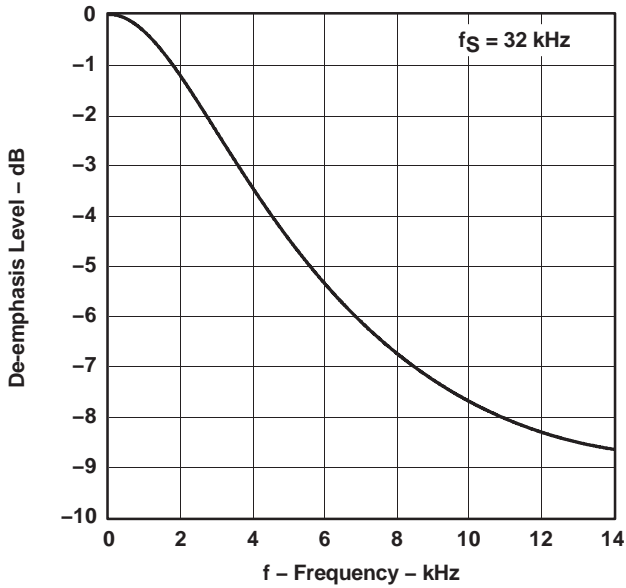


Figure 5

DE-EMPHASIS ERROR
VS
FREQUENCY

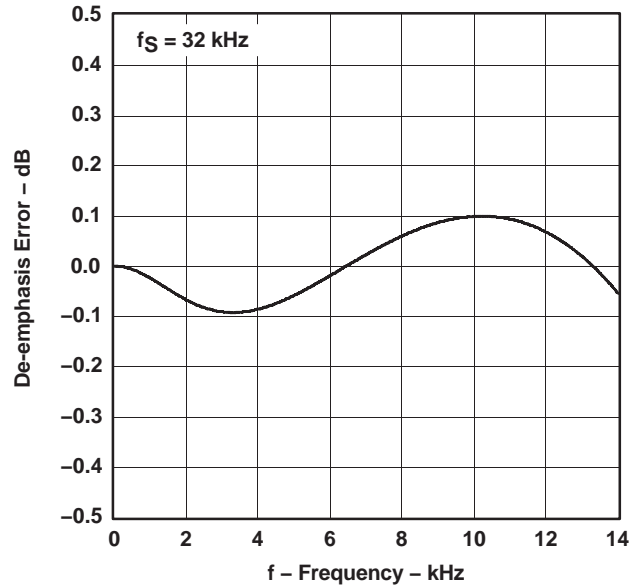


Figure 6

DE-EMPHASIS LEVEL
VS
FREQUENCY

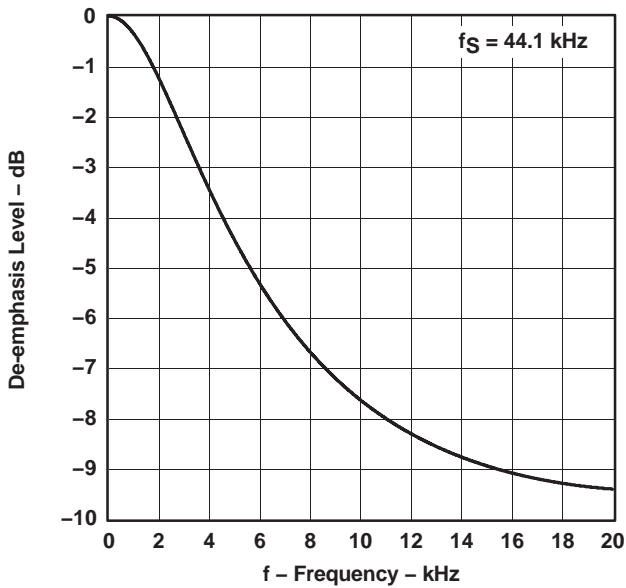


Figure 7

DE-EMPHASIS ERROR
VS
FREQUENCY

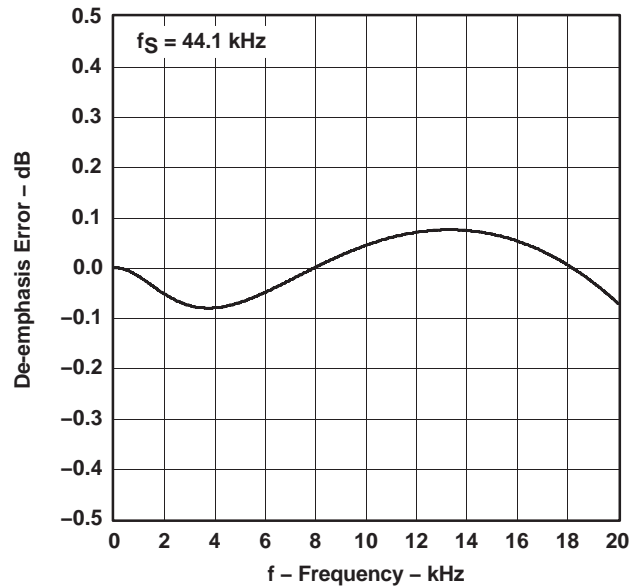


Figure 8

De-Emphasis Filter (Continued)

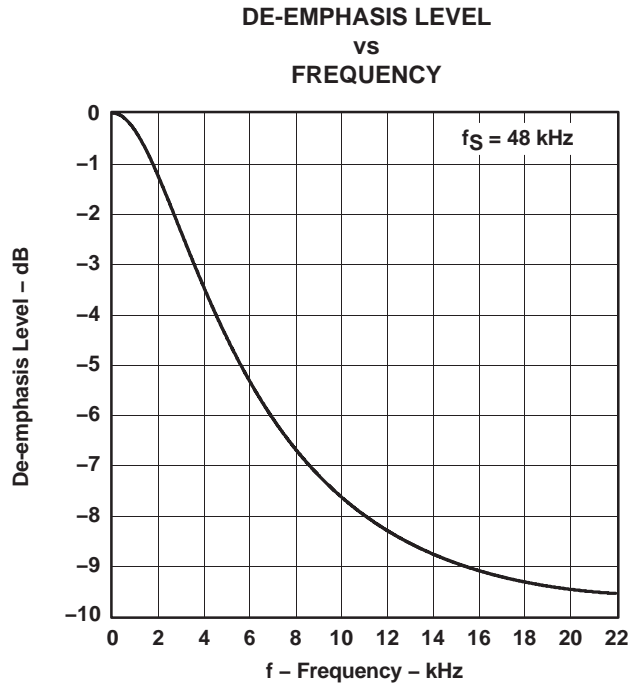


Figure 9

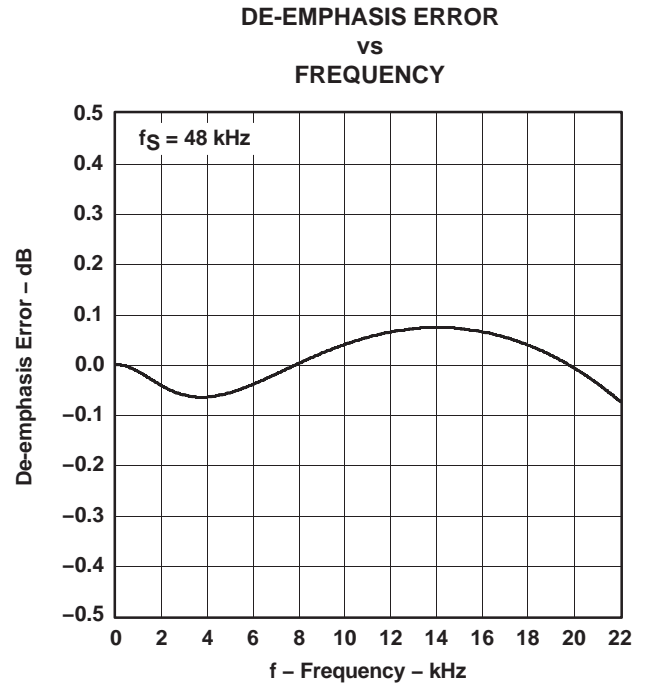


Figure 10

ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE

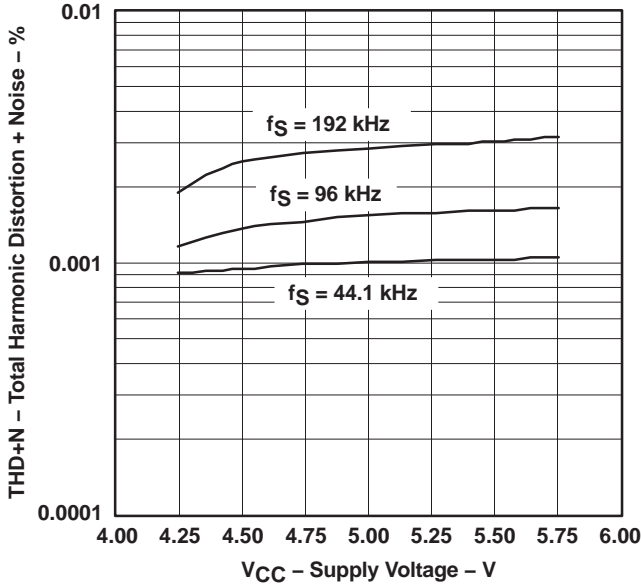


Figure 11

DYNAMIC RANGE
vs
SUPPLY VOLTAGE

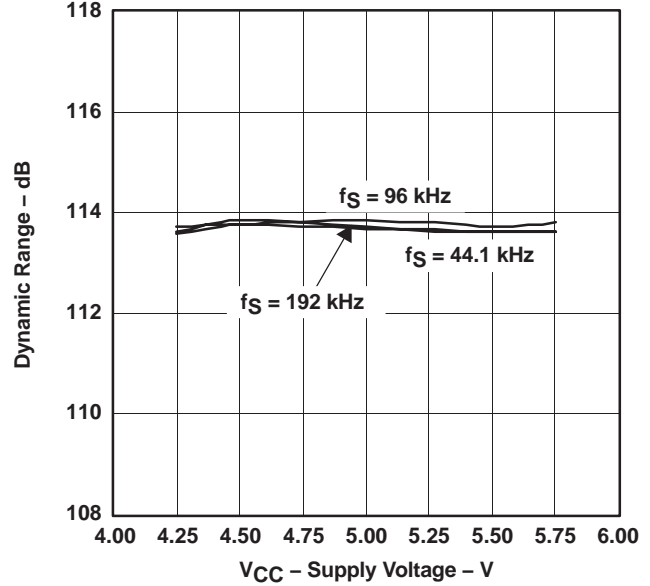


Figure 12

SIGNAL-to-NOISE RATIO
vs
SUPPLY VOLTAGE

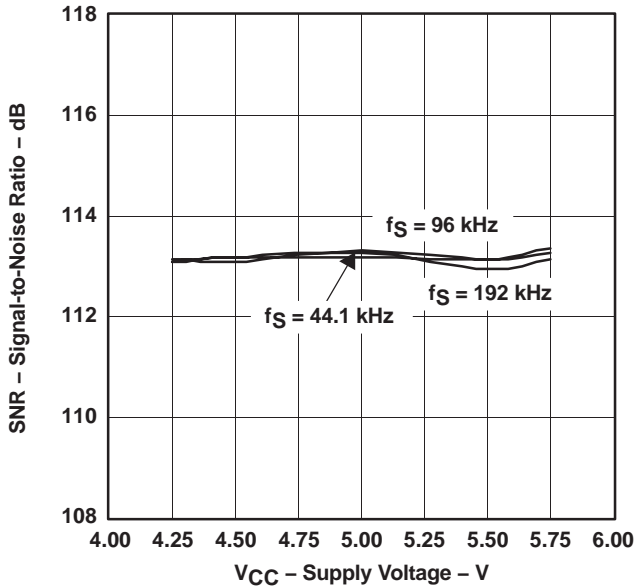


Figure 13

CHANNEL SEPARATION
vs
SUPPLY VOLTAGE

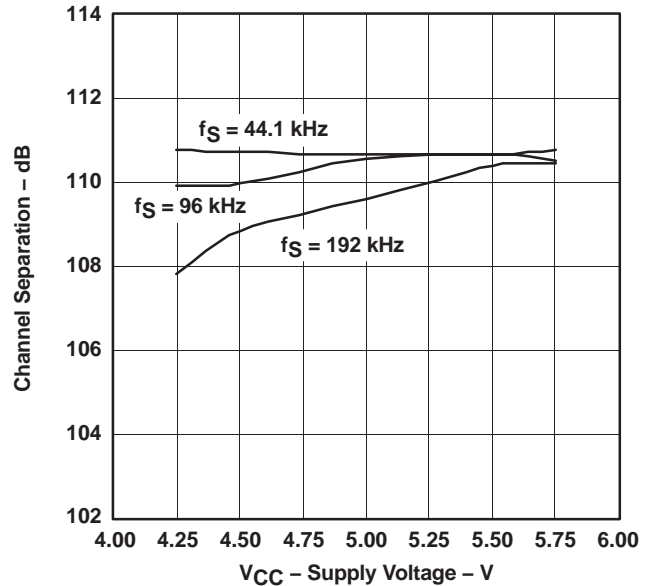


Figure 14

NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V.

Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE
vs
FREE-AIR TEMPERATURE

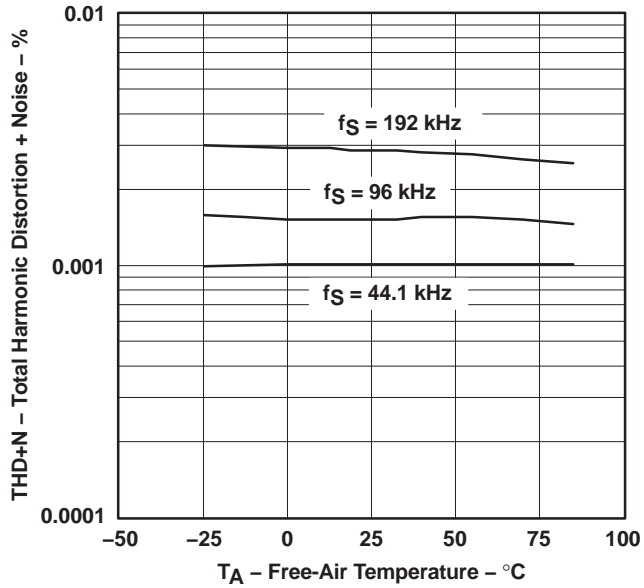


Figure 15

DYNAMIC RANGE
vs
FREE-AIR TEMPERATURE

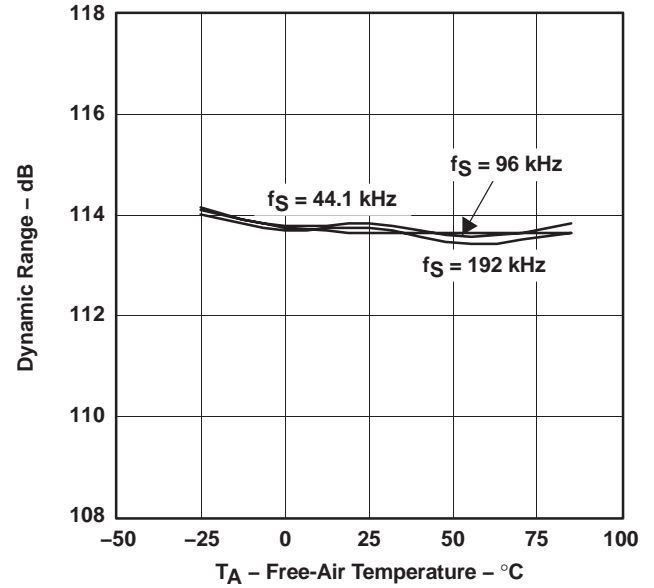


Figure 16

SIGNAL-to-NOISE RATIO
vs
FREE-AIR TEMPERATURE

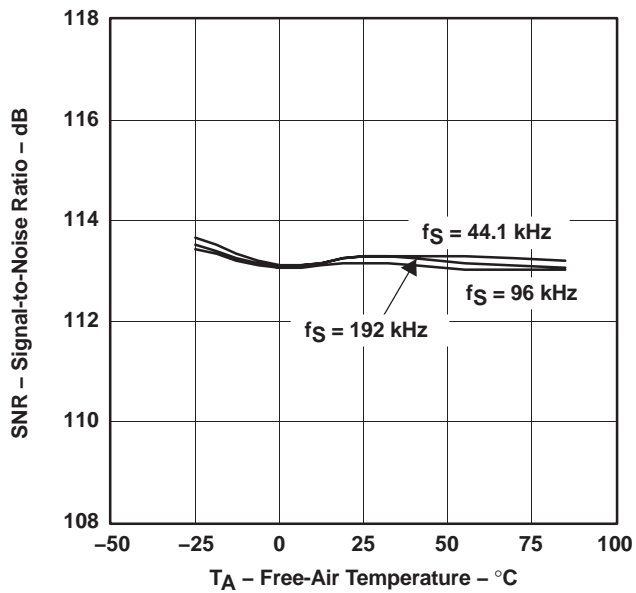


Figure 17

CHANNEL SEPARATION
vs
FREE-AIR TEMPERATURE

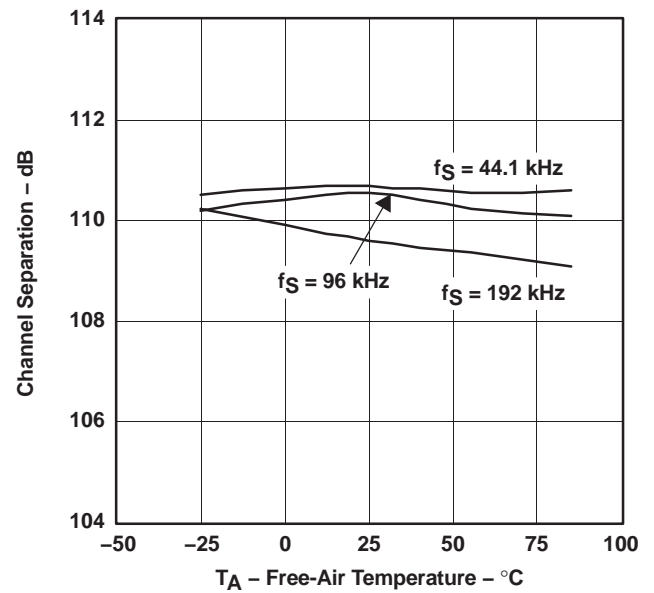


Figure 18

NOTE: PCM mode, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V.

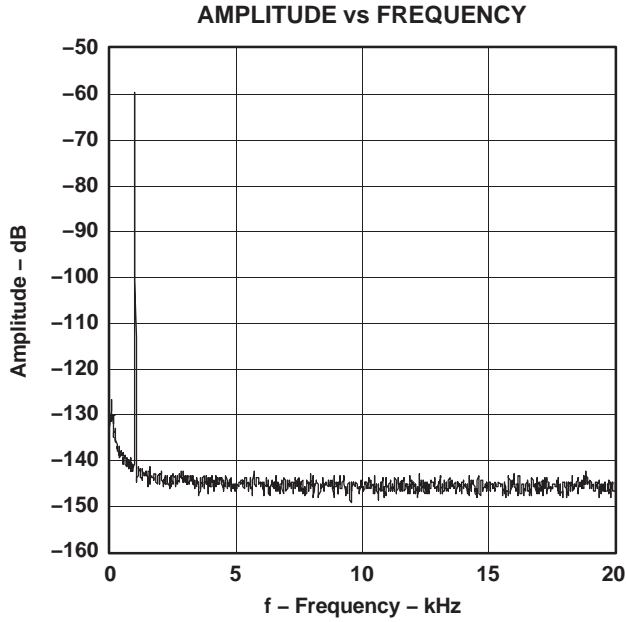


Figure 19. -60-dB Output Spectrum, BW = 20 kHz

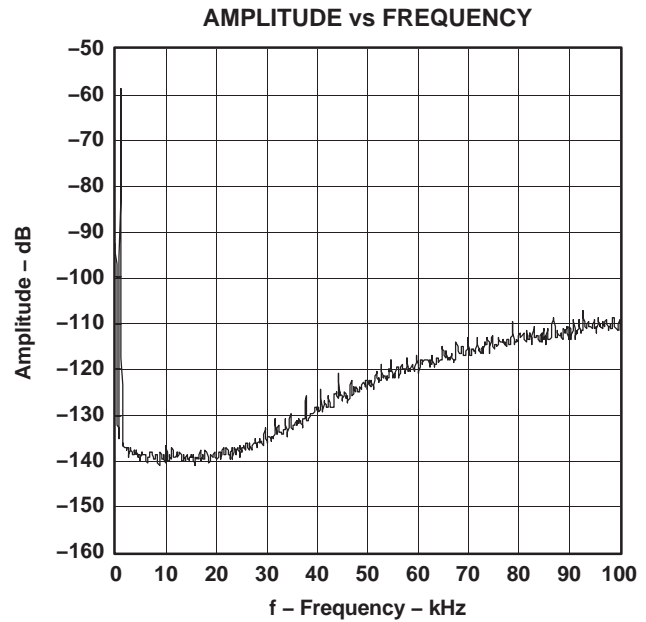


Figure 20. -60-dB Output Spectrum, BW = 100 kHz

NOTE: PCM mode, $f_S = 44.1$ kHz, 32768 points, 8 average, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V.

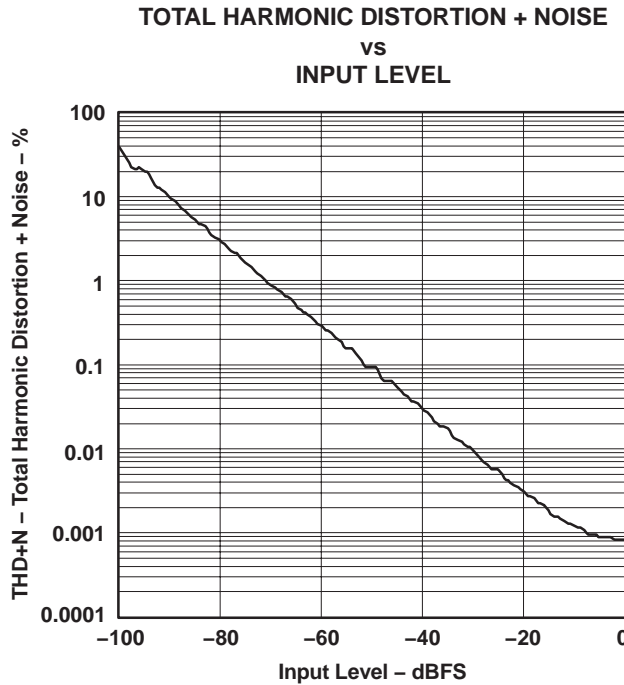


Figure 21. THD+N vs Input Level, PCM Mode

NOTE: PCM mode, $f_S = 44.1$ kHz, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V.

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

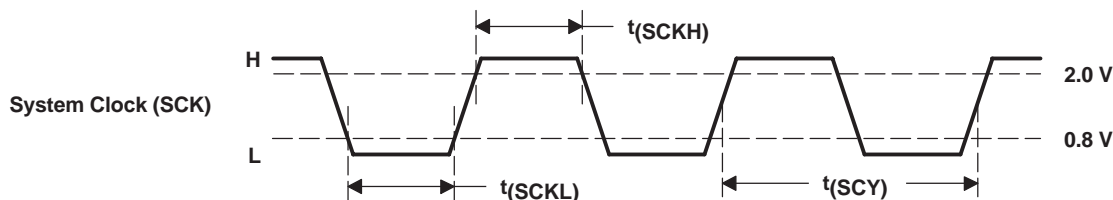
The PCM1793 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 5). The PCM1793 has a system clock detection circuit that automatically senses which frequency the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 22 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments' PLL1700 family of multiclock generators is an excellent choice for providing the PCM1793 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (F _{SCK}) (MHZ)					
	128 f _s	192 f _s	256 f _s	384 f _s	512 f _s	768 f _s
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.



PARAMETERS		MIN	MAX	UNITS
$t(SCY)$	System clock pulse cycle time	13		ns
$t(SCKH)$	System clock pulse duration, HIGH	5		ns
$t(SCKL)$	System clock pulse duration, LOW	5		ns

Figure 22. System Clock Input Timing

Power-On and External Reset Functions

The PCM1793 includes a power-on reset function. Figure 23 shows the operation of this function. With $V_{DD} > 2$ V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2$ V.

The PCM1793 also includes an external reset capability using the \overline{RST} input (pin 6). This allows an external controller or master reset circuit to force the PCM1793 to initialize to its default reset state.

Figure 24 shows the external reset operation and timing. The \overline{RST} pin is set to logic 0 for a minimum of 20 ns. The \overline{RST} pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1793 power up and system clock activation.

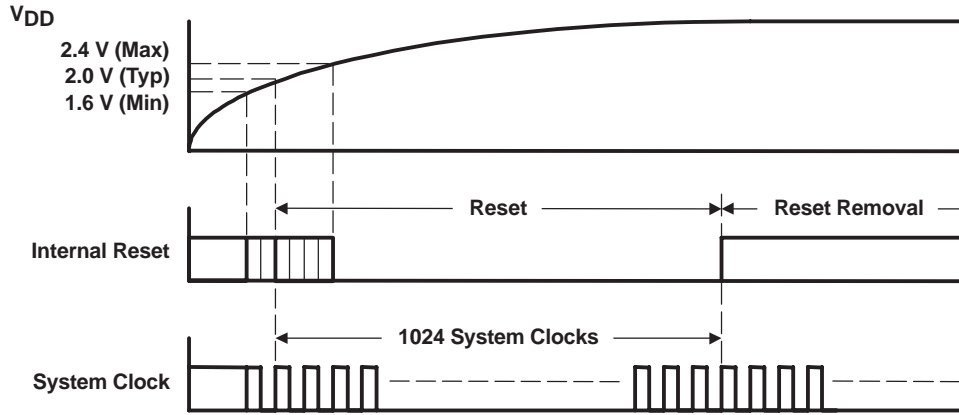
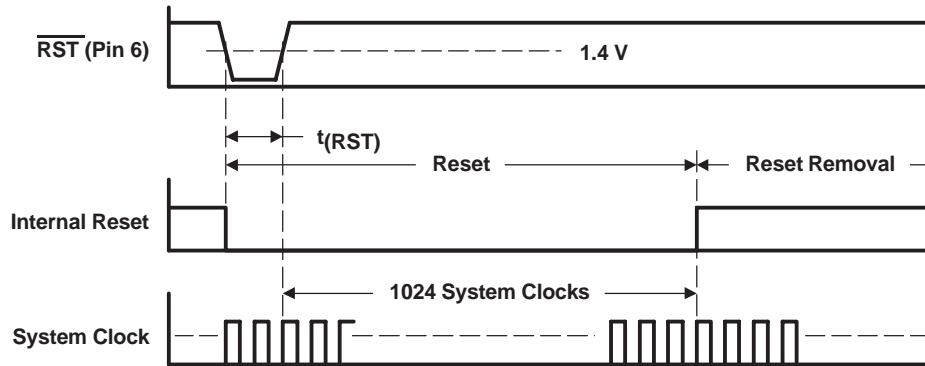


Figure 23. Power-On Reset Timing



PARAMETERS		MIN	MAX	UNITS
$t_{(RST)}$	Reset pulse duration, LOW	20		ns

Figure 24. External Reset Timing

AUDIO DATA INTERFACE

Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 1), BCK (pin 2), and DATA (pin 3). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1793 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1793 requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

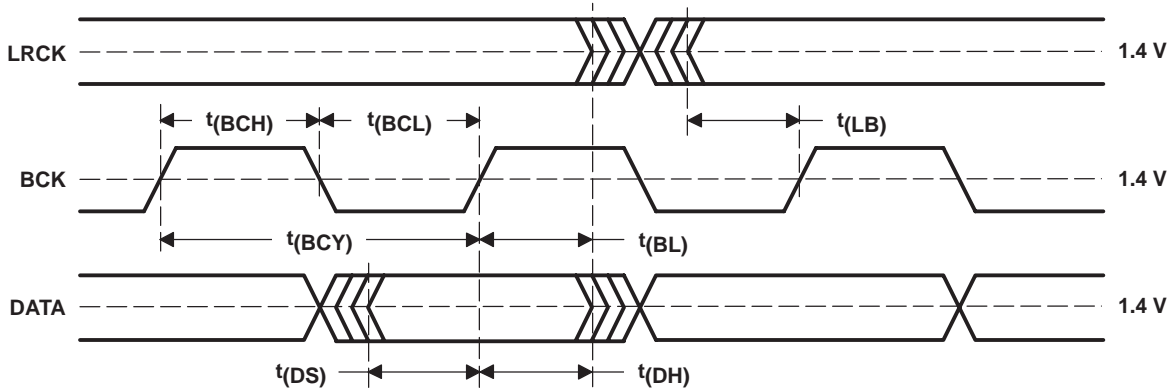
If the relationship between LRCK and the system clock changes more than ± 6 BCK, internal operation is initialized within $1/f_S$ and the analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

PCM Audio Data Formats and Timing

The PCM1793 supports industry-standard audio data formats, including standard right-justified, I²S, and left-justified. The data formats are shown in Figure 26. Data formats are selected using the format bits, FMT2 (pin 28), FMT1 (pin 27), and FMT0 (pin 26) as shown in Table 2. All formats require binary 2s complement, MSB-first audio data. Figure 25 shows a detailed timing diagram for the serial audio interface.

Table 2. Audio Data Format Selection

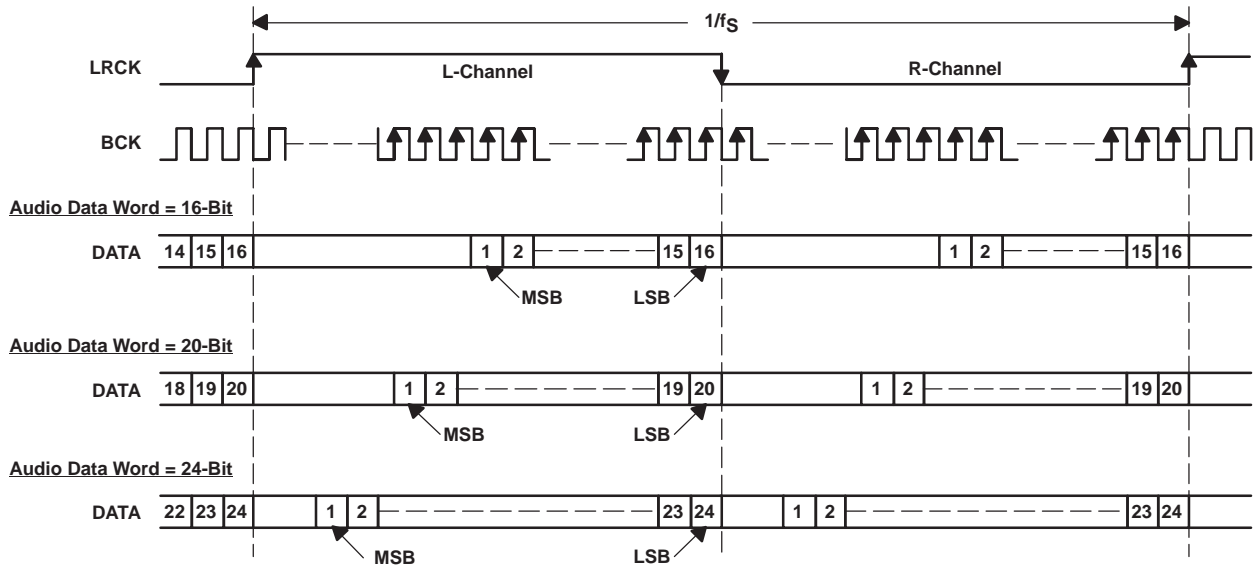
FMT2 PIN 28	FMT1 PIN 27	FMT0 PIN 26	FORMAT
LOW	LOW	LOW	16-bit standard format, right-justified
LOW	LOW	HIGH	20-bit standard format, right-justified
LOW	HIGH	LOW	24-bit standard format, right-justified
LOW	HIGH	HIGH	24-bit MSB-first, left-justified format
HIGH	LOW	LOW	16-bit I ² S format
HIGH	LOW	HIGH	24-bit I ² S format
HIGH	HIGH	LOW	Reserved
HIGH	HIGH	HIGH	Reserved



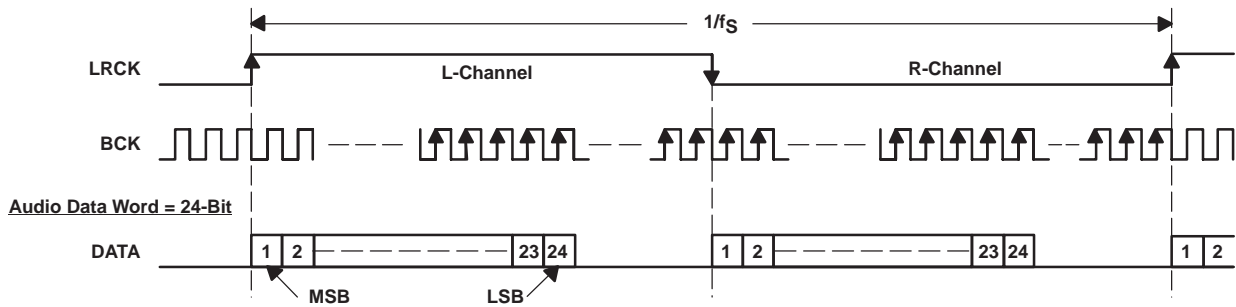
PARAMETERS		MIN	MAX	UNITS
t(BCY)	BCK pulse cycle time	70		ns
t(BCL)	BCK pulse duration, LOW	30		ns
t(BCH)	BCK pulse duration, HIGH	30		ns
t(BL)	BCK rising edge to LRCK edge	10		ns
t(LB)	LRCK edge to BCK rising edge	10		ns
t(DS)	DATA setup time	10		ns
t(DH)	DATA hold time	10		ns
—	LRCK clock duty	50% ± 2 bit clocks		

Figure 25. Timing of Audio Interface

(1) Standard Data Format (Right Justified); L-Channel = HIGH, R-Channel = LOW



(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(3) I²S Data Format; L-Channel = LOW, R-Channel = HIGH

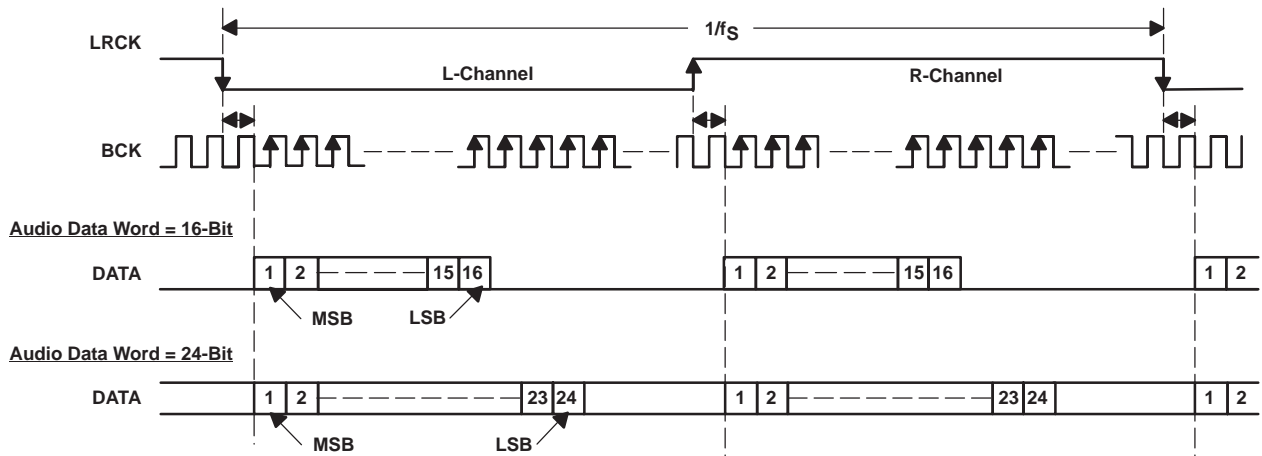


Figure 26. Audio Data Input Formats

FUNCTION DESCRIPTIONS

Zero Detect

When the PCM1793 detects that the audio input data in the L-channel or R-channel is continuously zero for $1024 f_S$, the PCM1793 sets ZEROL (pin 23) or ZEROR (pin 22) to HIGH.

Soft Mute

The PCM1793 supports mute operation. When MUTE (pin 4) is set to HIGH, both analog outputs are transitioned to the bipolar zero level in -0.5-dB steps with a transition speed of $1/f_S$ per step. This system provides pop-free muting of the DAC output.

De-Emphasis

The PCM1793 has de-emphasis filters for sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz. DEMP1 (pin 25) and DEMP0 (pin 24) select the sampling frequency for which de-emphasis filtering is performed, as shown in Table 3.

Table 3. De-Emphasis Control

DEMP1 PIN 25	DEMP0 PIN 24	DE-EMPHASIS FUNCTION
LOW	LOW	Disabled
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

TYPICAL CONNECTION DIAGRAM

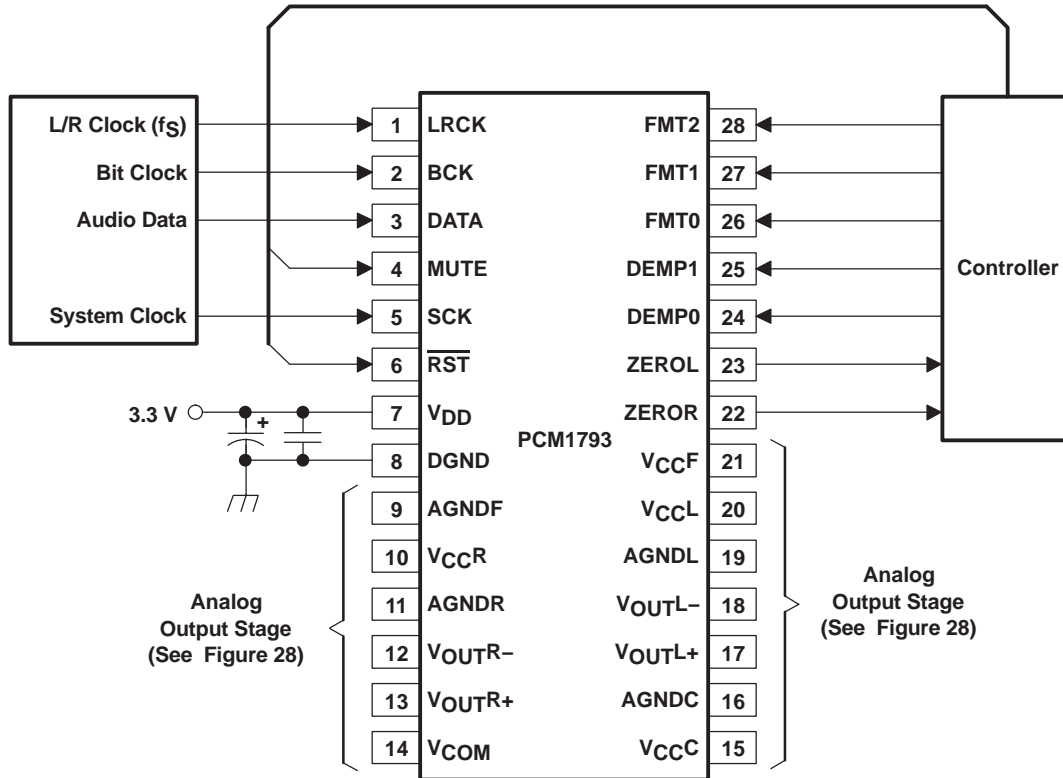
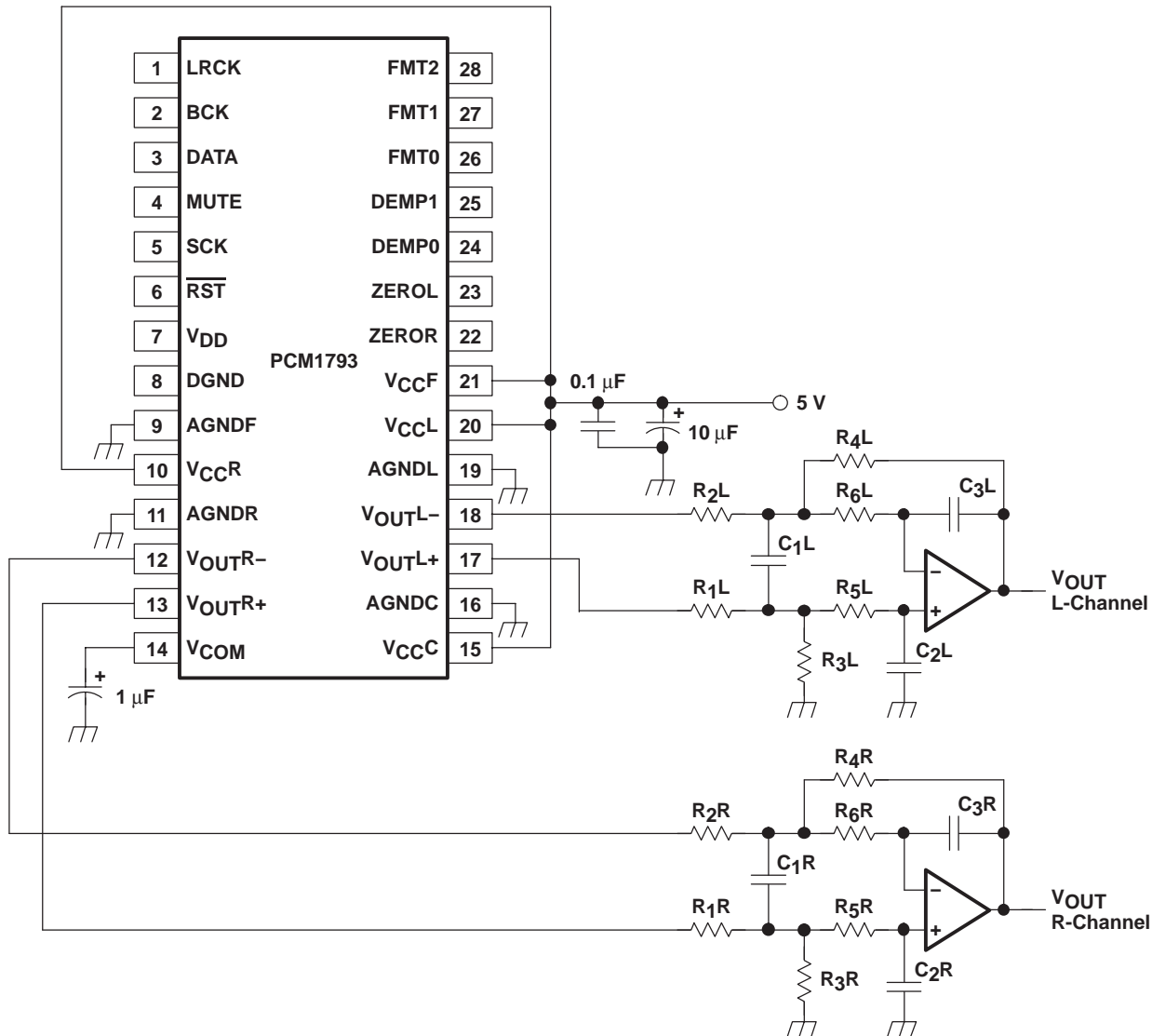


Figure 27. Typical Application Circuit

APPLICATION INFORMATION

ANALOG OUTPUTS



NOTE: Example R and C values for $f_C = 77$ kHz – R_1, R_2 : 1.8 k Ω , R_3, R_4 : 3.3 k Ω , R_5, R_6 : 680 Ω , C_1 : 1800 pF, C_2, C_3 : 560 pF.

Figure 28. Typical Application for Analog Output Stage

Analog Output Level and LPF

The signal level of the DAC differential-voltage output $\{(V_{OUTL+}) - (V_{OUTL-}), (V_{OUTR+}) - (V_{OUTR-})\}$ is 3.2 V_{p-p} at 0 dB (full scale). The voltage output of the LPF is given by following equation:

$$V_{OUT} = 3.2 \text{ V}_{p-p} \times (R_f / R_i)$$

Here, R_f is the feedback resistor in the LPF, and $R_3 = R_4$ in a typical application circuit. R_i is the input resistor in the LPF, and $R_1 = R_2$ in a typical application circuit.

Op Amp for LPF

An OPA2134 or 5532 type op amp is recommended for the LPF circuit to obtain the specified audio performance. Dynamic performance such as gain bandwidth, settling time, and slew rate of the op amp largely determines the audio dynamic performance of the LPF section. The input noise specification of the op amp should be considered to obtain a 113-dB S/N ratio.

Analog Gain of Balanced Amplifier

The DAC voltage outputs are followed by balanced amplifier stages, which sum the differential signals for each channel, creating a single-ended voltage output. In addition, the balanced amplifiers provide a third-order low-pass filter function, which band limits the audio output signal. The cutoff frequency and gain are determined by external R and C component values. In this case, the cutoff frequency is 77 kHz with a gain of 1.83. The output voltage for each channel is 5.9 V_{p-p}, or 2.1 V rms.

THEORY OF OPERATION

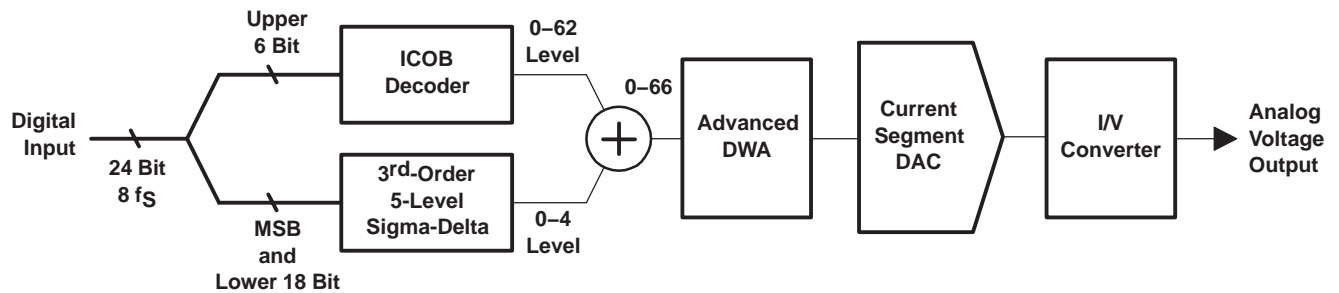


Figure 29. Advanced Segment DAC With I/V Converter

The PCM1793 uses TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1793 provides balanced voltage outputs.

Digital input data via the digital filter is separated into 6 upper bits and 18 lower bits. The 6 upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 f_s by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to an up-to-66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.

CONSIDERATIONS FOR APPLICATION CIRCUITS

PCB Layout Guidelines

A typical PCB floor plan for the PCM1793 is shown in Figure 30. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1793 must be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board. Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common 5-V supply would be used for the analog and digital sections, an inductance (RF choke, ferrite bead) must be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 31 shows the recommended approach for single-supply applications.

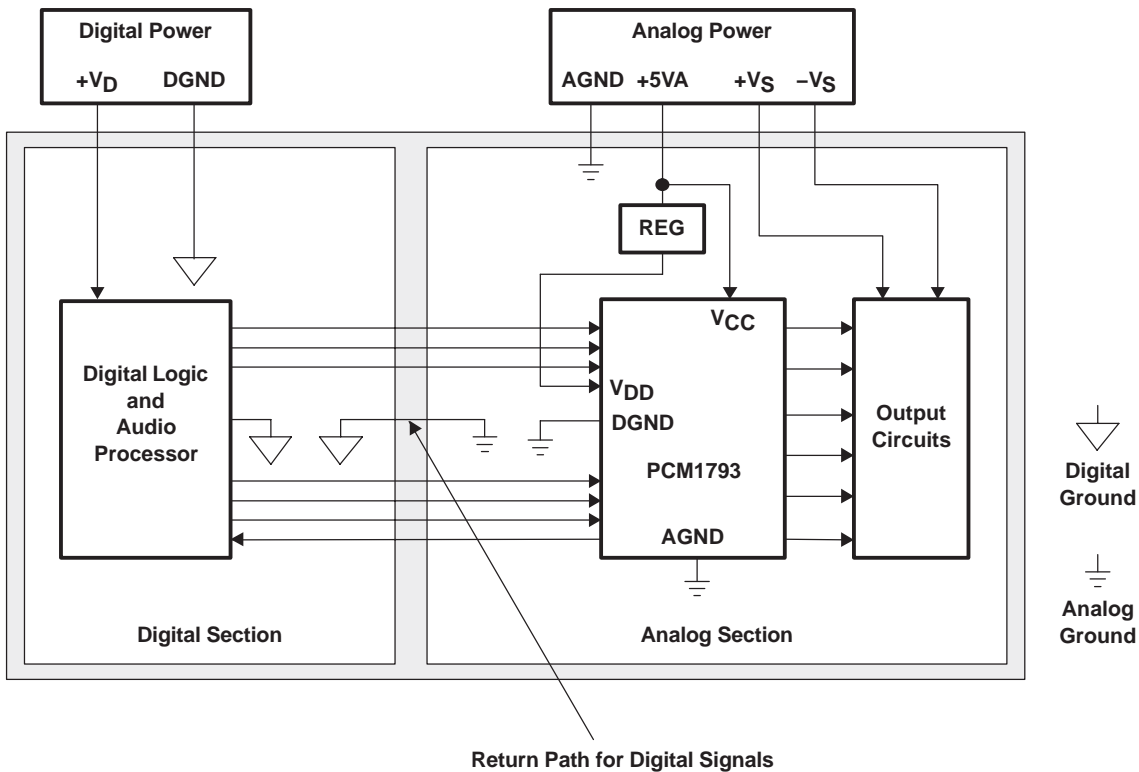


Figure 30. Recommended PCB Layout

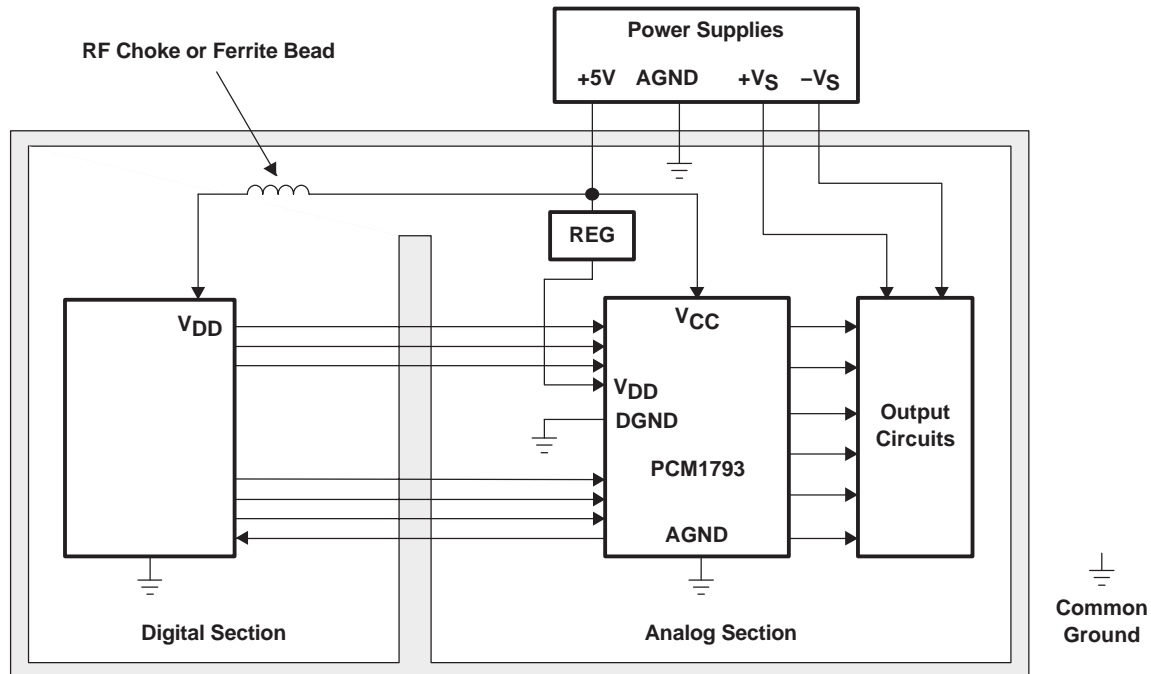


Figure 31. Single-Supply PCB Layout

Bypass and Decoupling Capacitor Requirements

Various-sized decoupling capacitors can be used, with no special tolerances being required. All capacitors must be located as close as possible to the appropriate pins of the PCM1793 to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors that are designed for hi-fi audio applications are recommended for larger values, while metal film or monolithic ceramic capacitors are used for smaller values.

Post-LPF Design

By proper choice of the op amp and resistors used in the post-LPF circuit, excellent performance of the PCM1793 should be achieved. To obtain 0.001% THD+N, 113 dB signal-to-noise-ratio audio performance, the THD+N and input noise performance of the op amp must be considered. This is because the input noise of the op amp contributes directly to the output noise level of the application. The V_{OUT} pins of the PCM1793 and the input resistor of the post-LPF circuit must be connected as closely as possible.

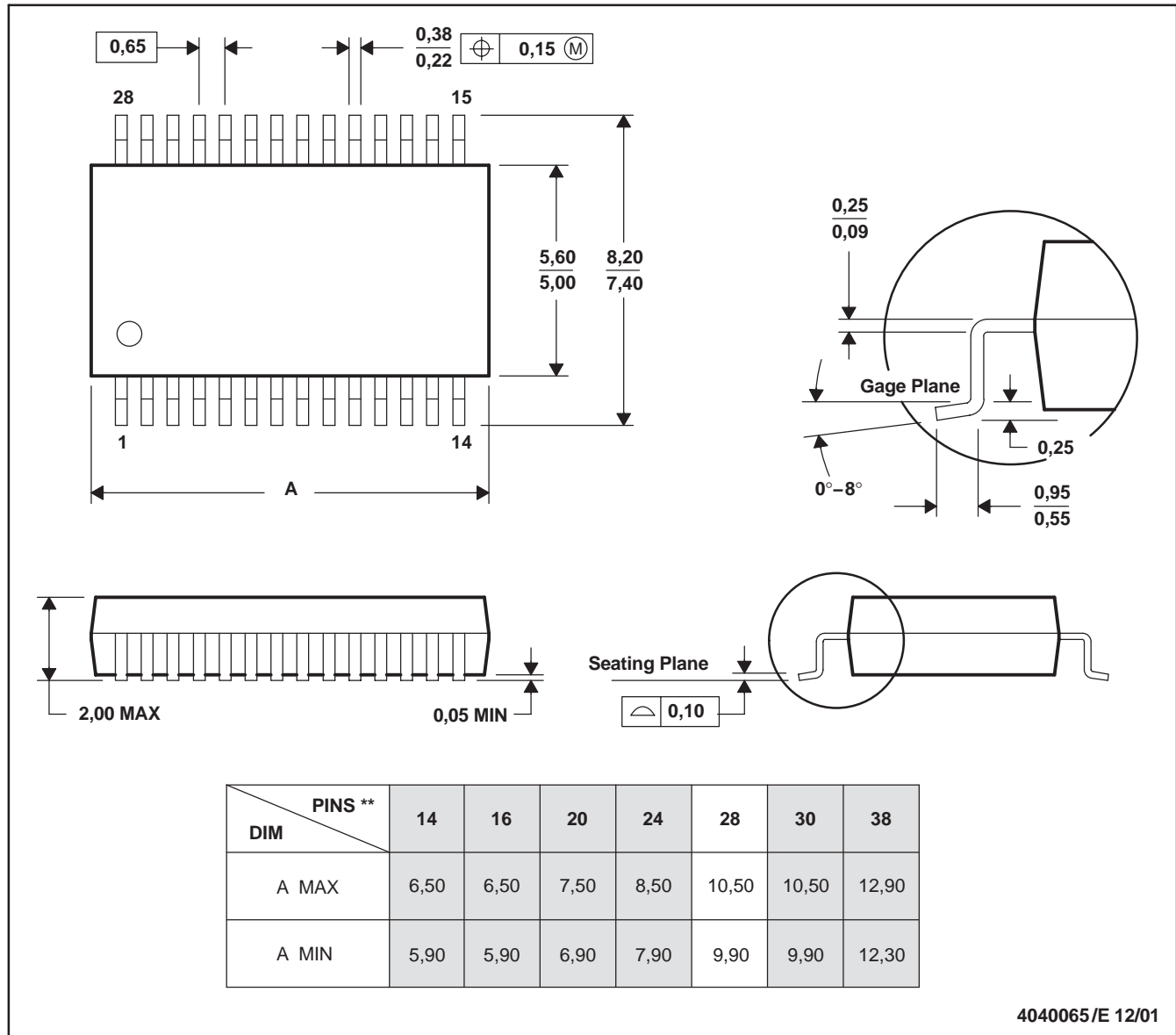
Out-of-band noise level and attenuated sampling spectrum level are much lower than for typical delta-sigma type DACs due to the combination of a high-performance digital filter and advanced segment DAC architecture. The use of a second-order or third-order post-LPF is recommended for the post-LPF of the PCM1793. The cutoff frequency of the post-LPF depends on the application. For example, there are many sampling-rate operations such as $f_S = 44.1$ kHz on CDDA, $f_S = 96$ kHz on DVD-M, $f_S = 192$ kHz on DVD-A, $f_S = 64 f_S$ on DSD (SACD).

MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1793DB	ACTIVE	SSOP	DB	28	47	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1793	Samples
PCM1793DBG4	ACTIVE	SSOP	DB	28	47	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1793	Samples
PCM1793DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1793	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

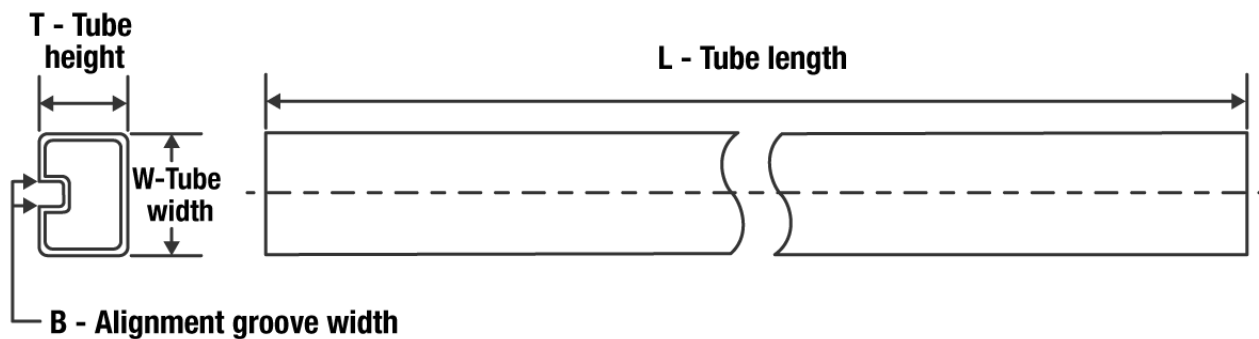

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1793DBR	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1793DBR	SSOP	DB	28	2000	336.6	336.6	28.6

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCM1793DB	DB	SSOP	28	47	500	10.6	500	9.6
PCM1793DBG4	DB	SSOP	28	47	500	10.6	500	9.6

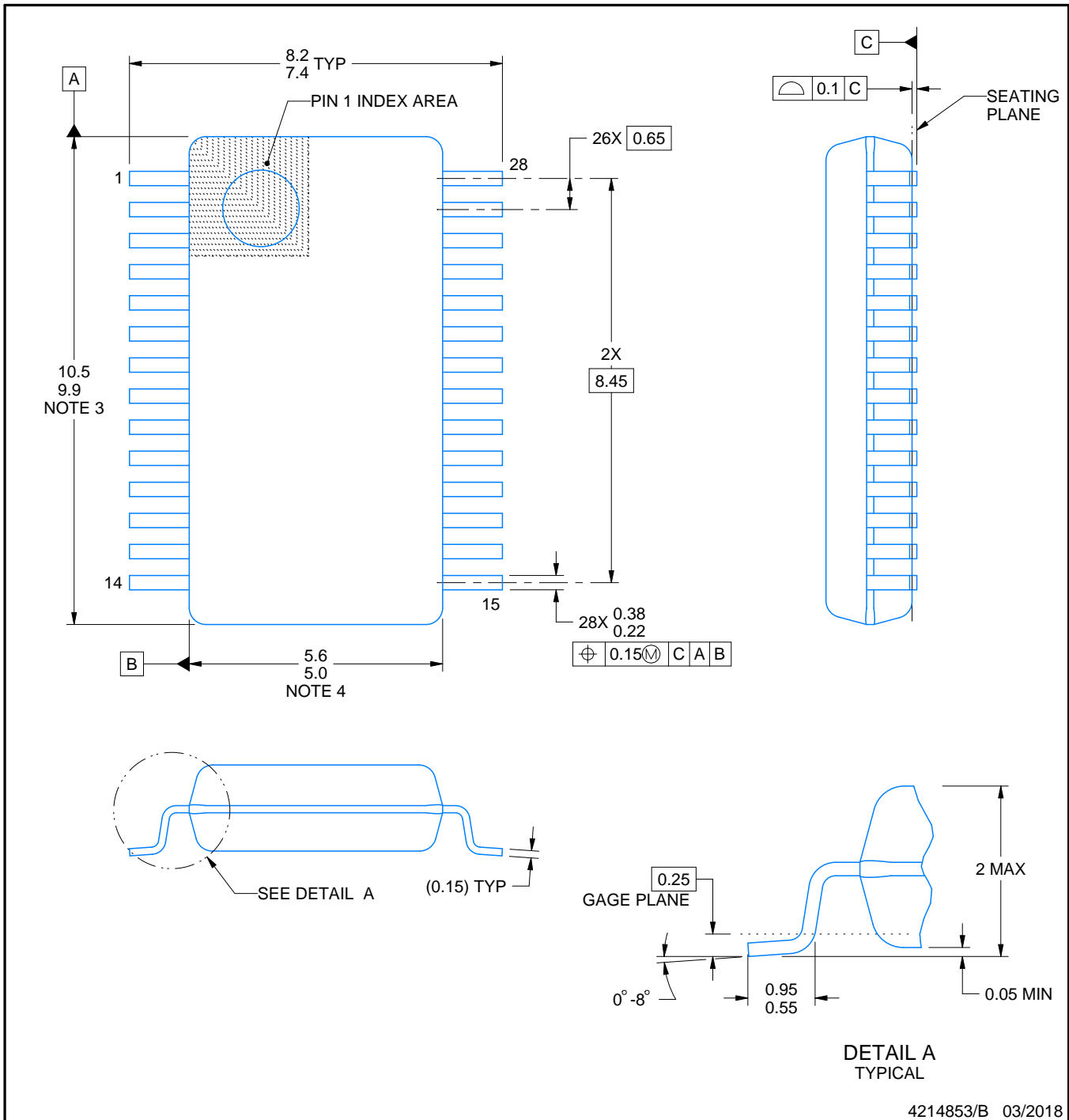
DB0028A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES:

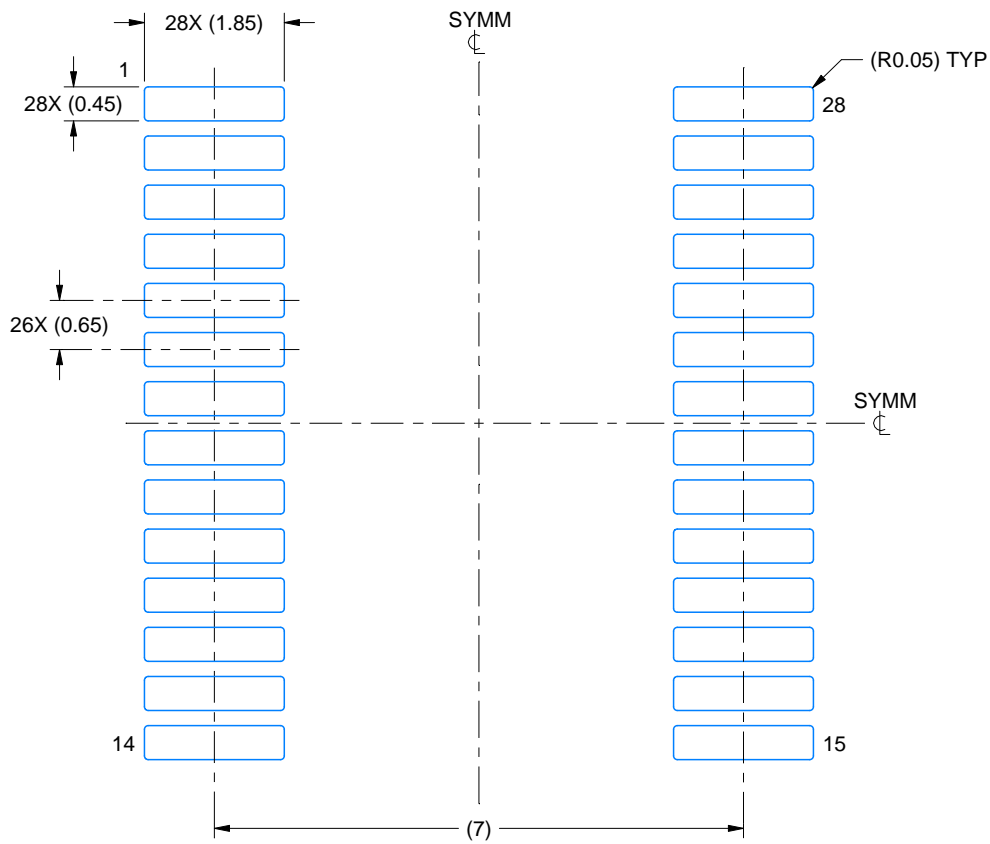
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

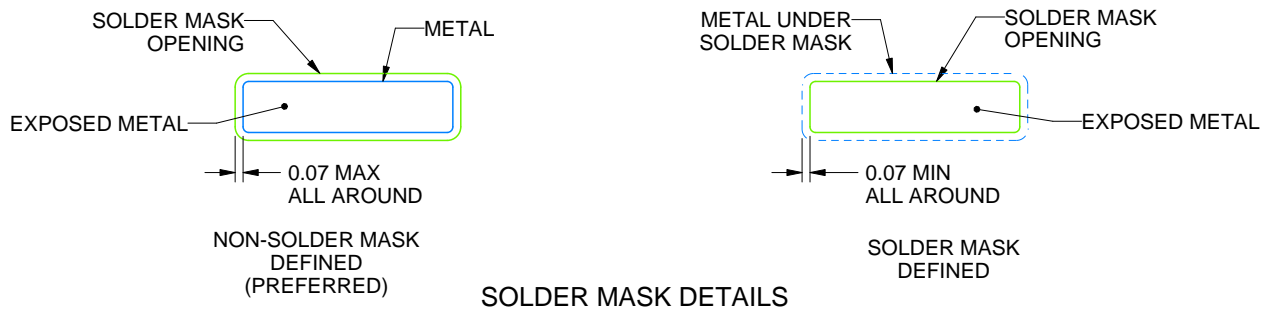
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214853/B 03/2018

NOTES: (continued)

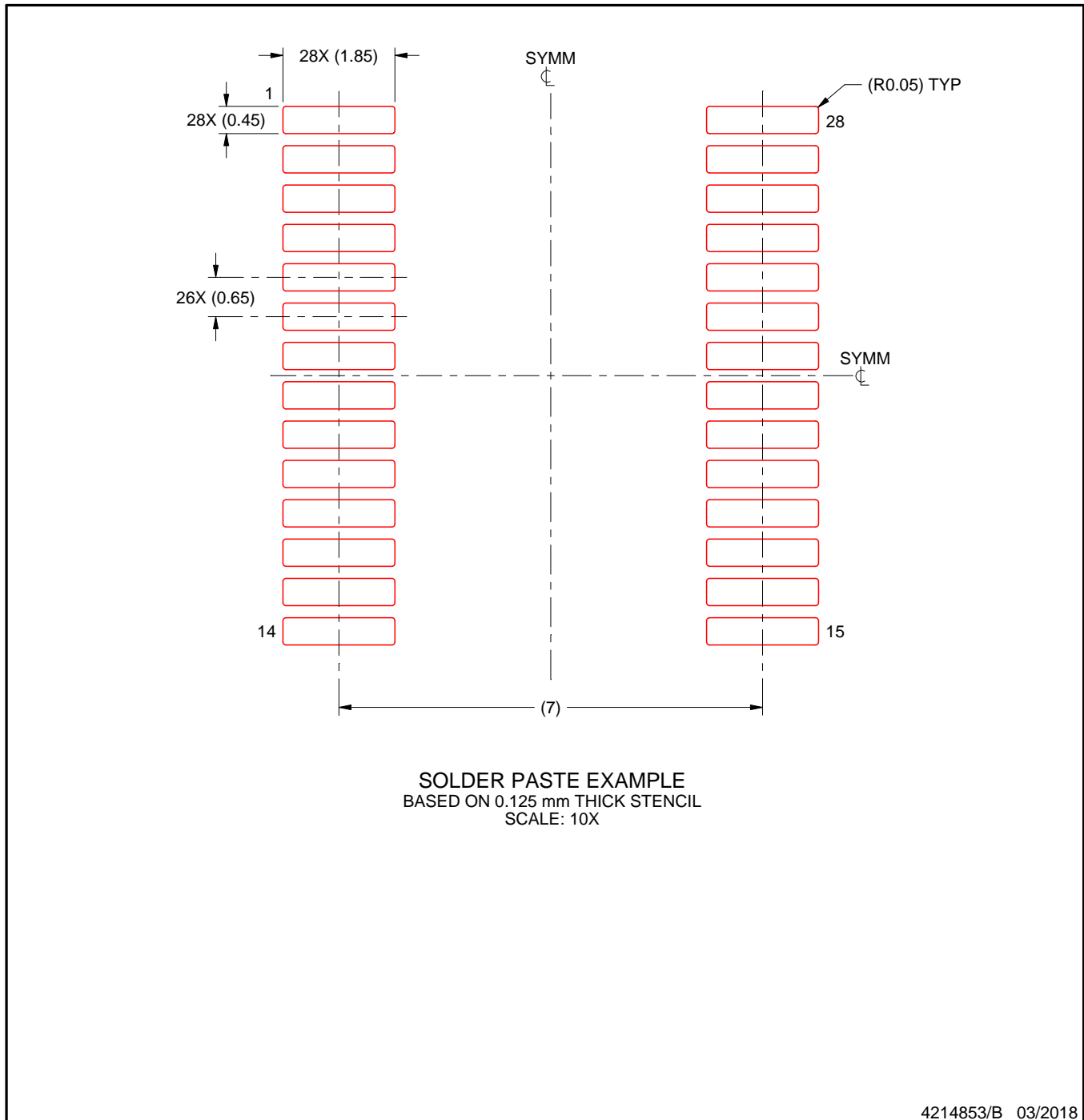
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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