

# DATA SHEET

## **PCKV857**

70–190 MHz differential 1:10 clock driver

Product data  
Supersedes data of 2001 Dec 03

2002 Sep 13

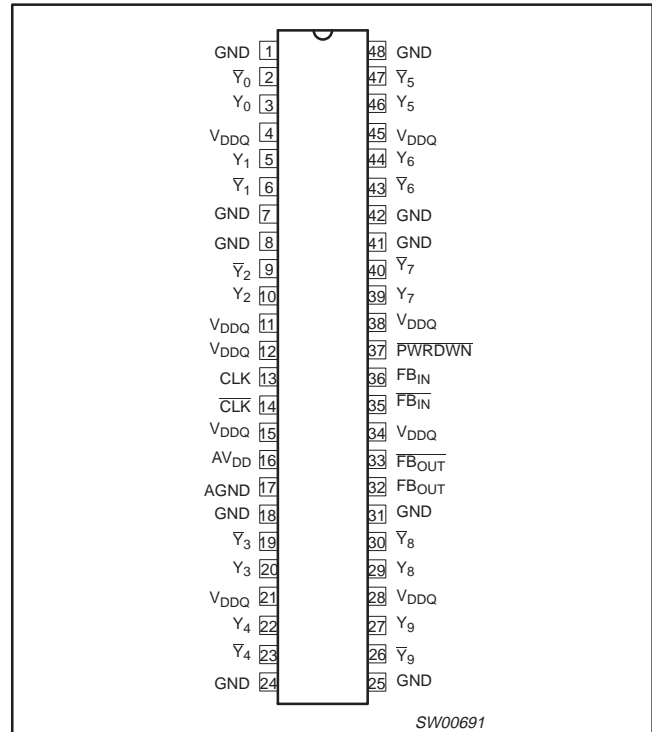
## 70–190 MHz differential 1:10 clock driver

## PCKV857

## FEATURES

- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications as per JEDEC specifications
- 1-to-10 differential clock distribution
- Very low skew (< 100 ps) and jitter (< 100 ps)
- Operation from 2.2 V to 2.7 V  $V_{DD}$  and 2.3 V to 2.7 V  $V_{DD}$
- SSTL\_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTL16877 or SSTV16857
- Designed for DDR 200 and 266 DIMM applications
- Available in TSSOP-48, TVSOP-48, and VFBGA56 (8 no connects) packages

## PIN CONFIGURATION



## DESCRIPTION

The PCKV857 is a high-performance, low-skew, low-jitter zero delay buffer designed for 2.5 V  $V_{DD}$  and 2.5 V  $AV_{DD}$  operation and differential data input and output levels.

The PCKV857 is a zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{CLK}$ ) to ten differential pairs of clock outputs ( $Y[0:9]$ ,  $\overline{Y}[0:9]$ ) and one differential pair feedback clock outputs ( $FB_{OUT}$ ,  $\overline{FB}_{OUT}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{CLK}$ ), the feedback clocks ( $FB_{IN}$ ,  $\overline{FB}_{IN}$ ), and the analog power input ( $AV_{DD}$ ). When  $PWRDWN$  is high, the outputs switch in phase and frequency with CLK. When  $PWRDWN$  is low, all outputs are disabled to high impedance state (3-State), and the PLL is shut down (low power mode). The device also enters the low power mode when the input frequency falls below 20 MHz. An input frequency detection circuit will detect the low frequency condition and after applying a > 20 MHz input signal, the detection circuit turns on the PLL again and enables the outputs.

When  $AV_{DD}$  is grounded, the PLL is turned off and bypassed for test purposes. The PCKV857 is also able to track spread spectrum clocking for reduced EMI.

The PCKV857 is characterized for operation from 0 to +70 °C.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	PCKV857DGG	SOT362-1
48-Pin Plastic TSSOP (TVSOP)	0 to +70 °C	PCKV857DGV	SOT480-1
56-ball Plastic VFBGA <sup>1</sup>	0 to +70 °C	PCKV857EV	SOT702-1

## NOTE:

1. 48 balls are connected, 8 balls are no-connects.

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## PIN DESCRIPTION

PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	SSTL_2 ground pins
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	$Y_n, \bar{Y}_n, FB_{OUT}, \overline{FB_{OUT}}$	SSTL_2 differential outputs
4, 11, 12, 15, 21, 28, 34, 38, 46	$V_{DDQ}$	SSTL_2 power pins
13, 14, 35, 36	$CLK_{IN}, \overline{CLK_{IN}}, FB_{IN}, \overline{FB_{IN}}$	SSTL_2 differential inputs
16	$AV_{DD}$	Analog power
17	AGND	Analog ground
37	$\overline{PWRDWN}$	Power-down control input

## BALL CONFIGURATION

	1	2	3	4	5	6
A	GND	NC	NC	NC	NC	GND
B	$Y_0$	$\bar{Y}_0$	$V_{DD}$	$V_{DD}$	$\bar{Y}_5$	$Y_5$
C	$\bar{Y}_1$	$Y_1$	GND	GND	$Y_6$	$\bar{Y}_6$
D	$\bar{Y}_2$	GND	$Y_2$	$Y_7$	GND	$\bar{Y}_7$
E	$V_{DD}$	$V_{DD}$			$V_{DD}$	$\overline{PWRDWN}$
F	CLK	$\overline{CLK}$			$\overline{FB_{IN}}$	$FB_{IN}$
G	$AV_{DD}$	AGND	$V_{DD}$	$V_{DD}$	$FB_{OUT}$	$\overline{FB_{OUT}}$
H	$\bar{Y}_3$	$Y_3$	GND	GND	$Y_8$	$\bar{Y}_8$
J	$Y_4$	$\bar{Y}_4$	$V_{DD}$	$V_{DD}$	$\bar{Y}_9$	$Y_9$
K	GND	NC	NC	NC	NC	GND

SW00951

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## FUNCTION TABLE

INPUTS			OUTPUTS				PLL ON/OFF
PWRDWN	CLK	CLK	$Y_n$	$\bar{Y}_n$	FB <sub>OUT</sub>	$\overline{\text{FB}}_{\text{OUT}}$	
L	L	H	Z	Z	Z <sup>1</sup>	Z <sup>1</sup>	OFF
L	H	L	Z	Z	Z <sup>1</sup>	Z <sup>1</sup>	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X <sup>2</sup>	< 20 MHz	< 20 MHz	Z	Z	Z <sup>1</sup>	Z <sup>1</sup>	OFF

### NOTES:

H = HIGH voltage level

L = LOW voltage level

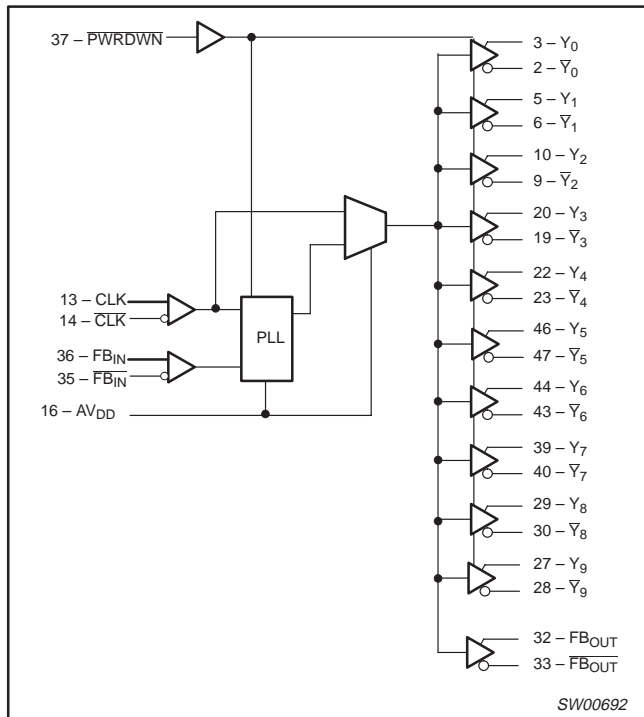
Z = high impedance OFF-state

X = don't care

1. Subject to change. May cause conflict with FB<sub>IN</sub> pins.

2. Additional feature that senses when the clock input is less than 20 MHz and places the part in sleep mode.

## BLOCK DIAGRAM



## 70–190 MHz differential 1:10 clock driver

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ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V <sub>DDQ</sub>	Supply voltage range		0.5	3.6	V
AV <sub>DD</sub>	Supply voltage range		0.5	3.6	V
V <sub>I</sub>	Input voltage range	see Notes 2 and 3	-0.5	V <sub>DDQ</sub> + 0.5	V
V <sub>O</sub>	Output voltage range	see Notes 2 and 3	-0.5	V <sub>DDQ</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub>	—	±50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub>	—	±50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>DDQ</sub>	—	±50	mA
	Continuous current to GND or V <sub>DDQ</sub>		—	±100	mA
T <sub>stg</sub>	Storage temperature range		-65	+150	°C

## NOTES:

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 3.6 V maximum.

RECOMMENDED OPERATING CONDITIONS<sup>1</sup>

SYMBOL	PARAMETER		CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
V <sub>DDQ</sub>	Supply voltage range			2.3	—	2.7	V
AV <sub>DD</sub>	Supply voltage range			2.2	—	2.7	V
V <sub>IL</sub>	Low level input voltage	CLK, $\overline{\text{CLK}}$ , FB <sub>IN</sub> , $\overline{\text{FB}}_{\text{IN}}$		—	—	V <sub>DDQ</sub> /2 - 0.18	V
		PWRDWN		-0.3	—	0.7	
V <sub>IH</sub>	High level input voltage	CLK, $\overline{\text{CLK}}$ , FB <sub>IN</sub> , $\overline{\text{FB}}_{\text{IN}}$		V <sub>DDQ</sub> /2 + 0.18	—	—	V
		PWRDWN		1.7	—	V <sub>DDQ</sub> + 0.3	
	DC input signal voltage		Note 2	-0.3	—	V <sub>DDQ</sub>	V
V <sub>ID</sub>	DC differential input signal voltage	CLK, FB <sub>IN</sub>	Note 3	0.36	—	V <sub>DDQ</sub> + 0.6	V
	AC differential input signal voltage	CLK, FB <sub>IN</sub>	Note 3	0.7	—	V <sub>DDQ</sub> + 0.6	V
V <sub>OX</sub>	Output differential cross-voltage		Note 4	V <sub>DDQ</sub> /2 - 0.2	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.2	V
V <sub>IX</sub>	Input differential cross-voltage		Note 4	V <sub>DDQ</sub> /2 - 0.2	—	V <sub>DDQ</sub> /2 + 0.2	V
I <sub>OH</sub>	High-level output current			—	—	-12	mA
I <sub>OL</sub>	Low-level output current			—	—	12	mA
SR	Input slew rate			1	—	4	V/ns
T <sub>amb</sub>	Operating free-air temperature			0	—	70	°C

## NOTES:

- Unused inputs must be held high or low to prevent them from floating.
- DC input signal voltage specifies the allowable DC execution of differential input.
- Differential input signal voltage specifies the differential voltage |V<sub>TR</sub> - V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input level and V<sub>CP</sub> is the complementary input level.
- Differential cross-point voltage is expected to track variations of V<sub>CC</sub> and is the voltage at which the differential signals must be crossing.

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$V_{IK}$	Input voltage, all inputs	$V_{DDQ} = 2.3 \text{ V}$ , $I_I = -18 \text{ mA}$	—	—	-1.2	V
$V_{OH}$	High-level output voltage	$V_{DDQ} = \text{min to max}$ , $I_{OH} = -1 \text{ mA}$	$V_{DDQ} - 0.1$	—	—	V
		$V_{DDQ} = 2.3 \text{ V}$ , $I_{OH} = -12 \text{ mA}$	1.7	—	—	V
$V_{OL}$	Low-level output voltage	$V_{DDQ} = \text{min to max}$ , $I_{OL} = 1 \text{ mA}$	—	—	0.1	V
		$V_{DDQ} = 2.3 \text{ V}$ , $I_{OL} = 12 \text{ mA}$	—	—	0.6	V
$I_I$	Input current	$V_{DDQ} = 2.7 \text{ V}$ , $V_I = 0 \text{ V to } 2.7 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OZ}$	High-impedance-state output current	$V_{DDQ} = 2.7 \text{ V}$ , $V_O = V_{DDQ} \text{ or GND}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{DDPD}$	Power-down current on $V_{DDQ} + AV_{DD}$	CLK and $\overline{\text{CLK}} = 0 \text{ MHz}$ , PWRDWN = low; $\Sigma$ of $I_{DD}$ and $AI_{DD}$	—	30	100	$\mu\text{A}$
$I_{DD}$	Dynamic current on $V_{DDQ}$	$f_O = 67 \text{ MHz to } 190 \text{ MHz}$	—	200	300	mA
$AI_{DD}$	Supply current on $AV_{DD}$	$f_O = 67 \text{ MHz to } 190 \text{ MHz}$	—	8	10	mA
$C_I$	Input capacitance	$V_{CC} = 2.5 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$	2	2.8	3	pF

**NOTE:**

1. This is intended to operate in the SSTL\_2 type IV unterminated mode without series resistors on the outputs.
2. All typical values are at respective nominal  $V_{DDQ}$ .
3. Differential cross-point voltage is expected to track variations of  $V_{DDQ}$  and is the voltage at which the differential signals must be crossing.

**TIMING REQUIREMENTS**

Over recommended ranges of supply voltage and operating free-air temperature.

SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{CK}$	Operating clock frequency	60	190	MHz
	Input clock duty cycle	40	60	%
	Stabilization time <sup>1</sup>	100	—	$\mu\text{s}$

**NOTE:**

1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power-up.

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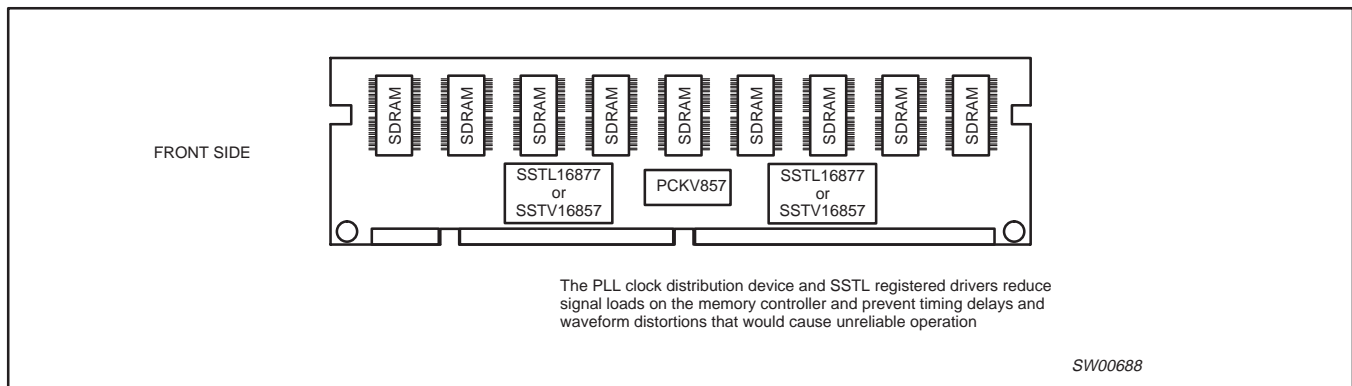
## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 1$  k $\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
$t_{(O)}$	Static phase offset	Figure 1		-150	0	150	ps
$t_{SK(O)}$	Output clock skew	Figure 2		—	—	75	ps
$t_{SLR(O)}$	Output clock skew rate	Figure 3		1	—	2	V/ns
$t_{JIT(PER)}$	Jitter (period)	Figure 4	$f_O = 67$ MHz to 200 MHz	-75	—	75	ps
$t_{JIT(CC)}$	Jitter (cycle-to-cycle)	Figure 5	$f_O = 67$ MHz to 200 MHz	-75	—	75	ps
$t_{JIT(HPER)}$	Half-period jitter	Figure 6		-100	—	100	ps
$t_{PLH}^1$	Low to high level propagation delay		Test mode/CLK to any output	—	3.7	—	ns
$t_{PHL}^1$	High to low level propagation delay		Test mode/CLK to any output	—	3.7	—	ns

**NOTE:**

1. Refers to transition of noninverting output.



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AC WAVEFORMS

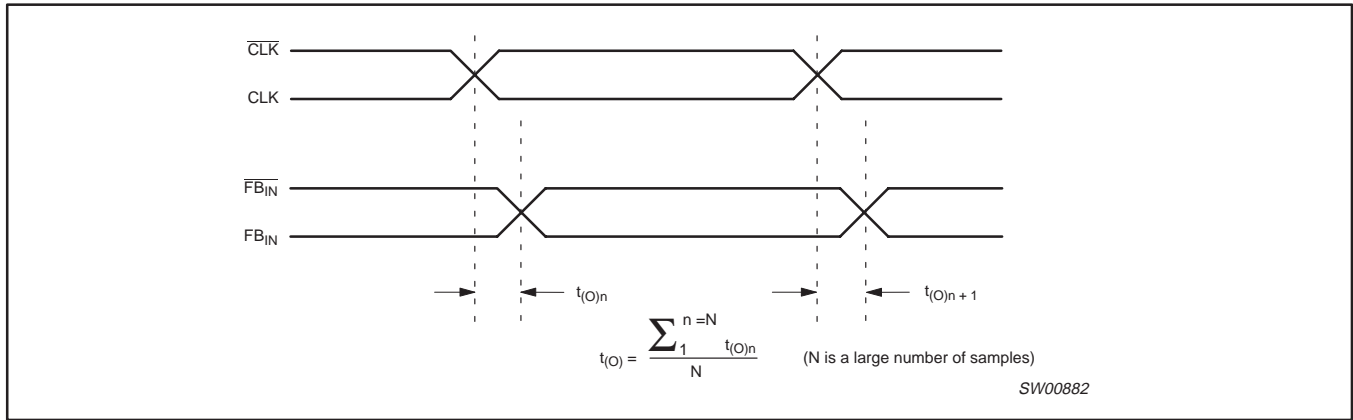


Figure 1. Static phase offset

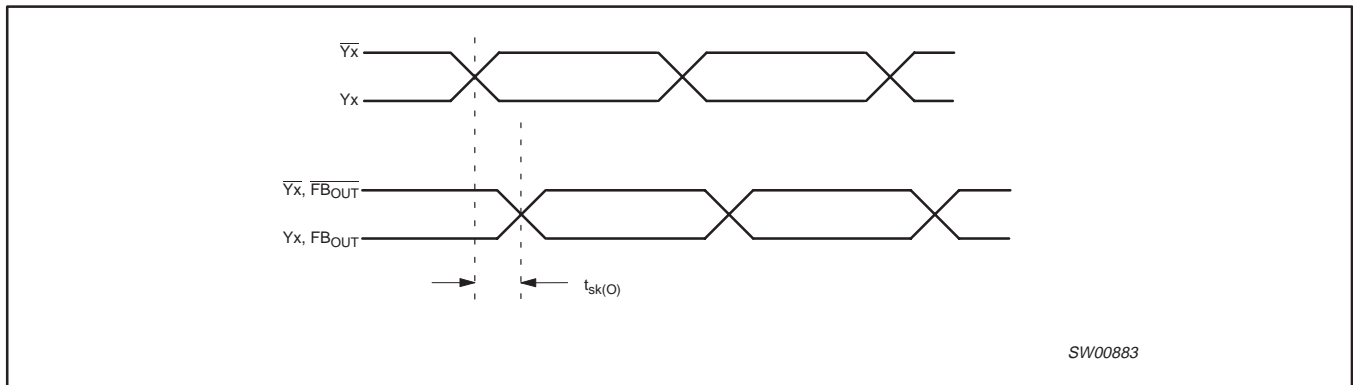


Figure 2. Output skew

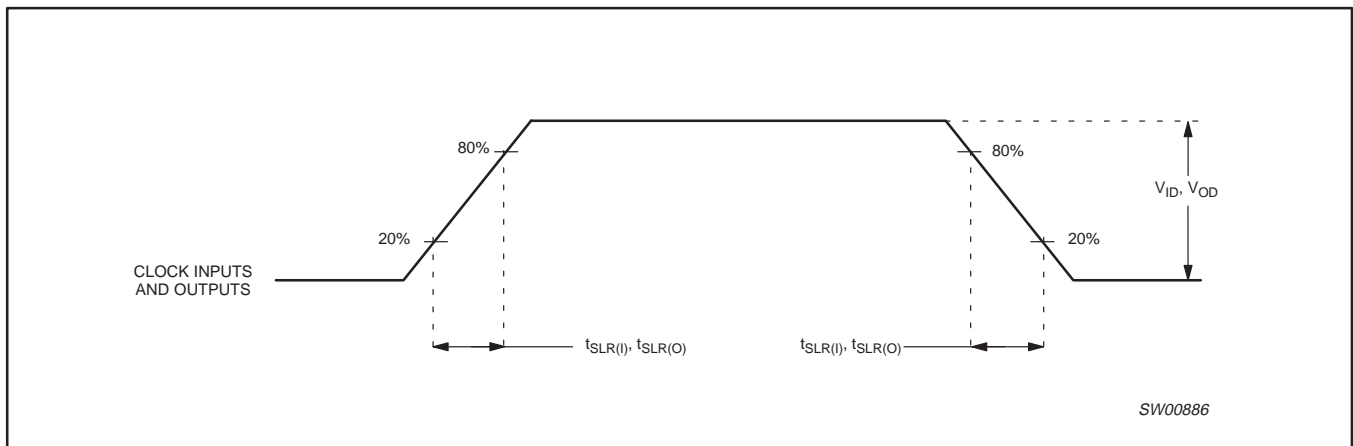


Figure 3. Input and output slew rates

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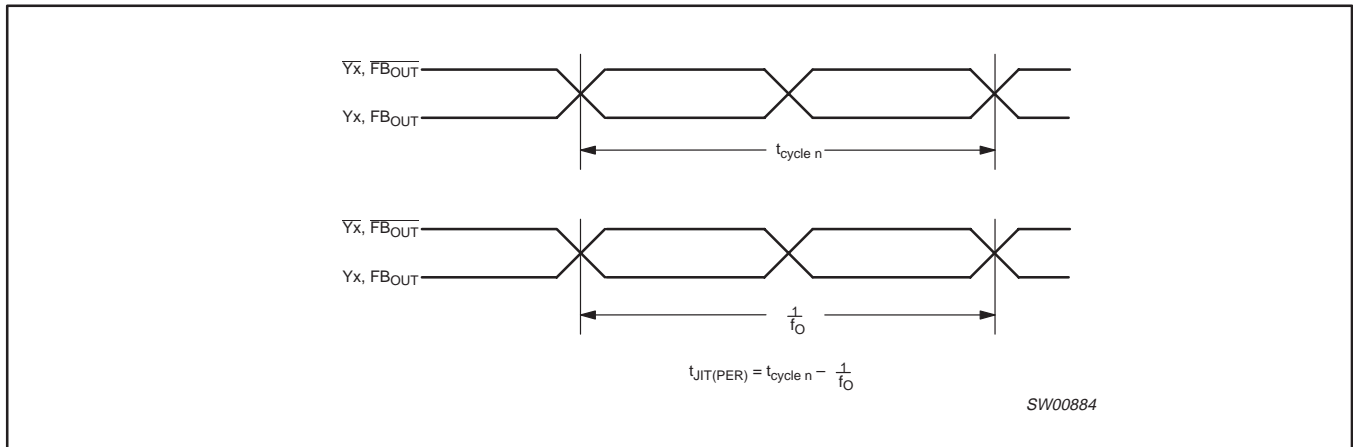


Figure 4. Period jitter

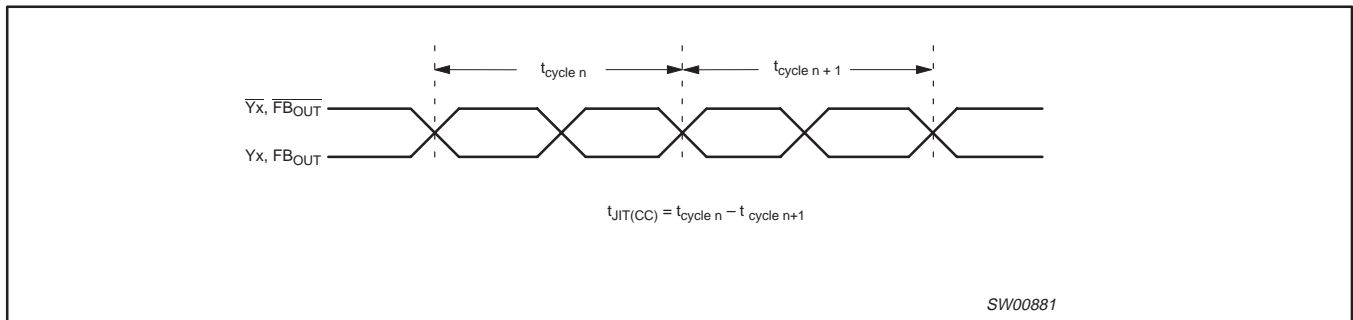


Figure 5. Cycle-to-cycle jitter

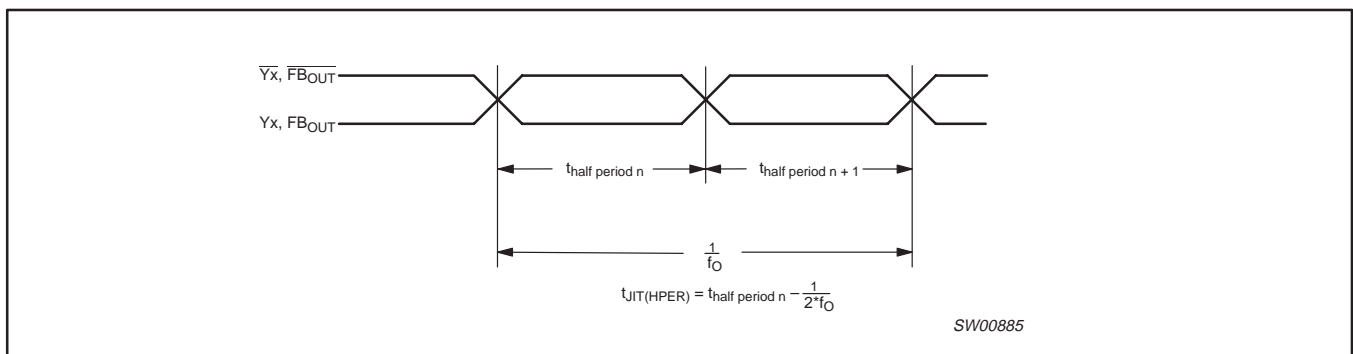


Figure 6. Half-period jitter

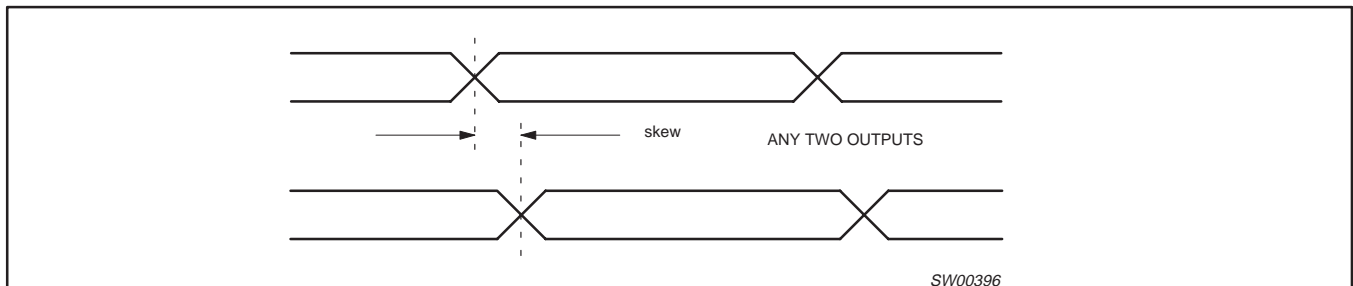


Figure 7. Skew between any two outputs.

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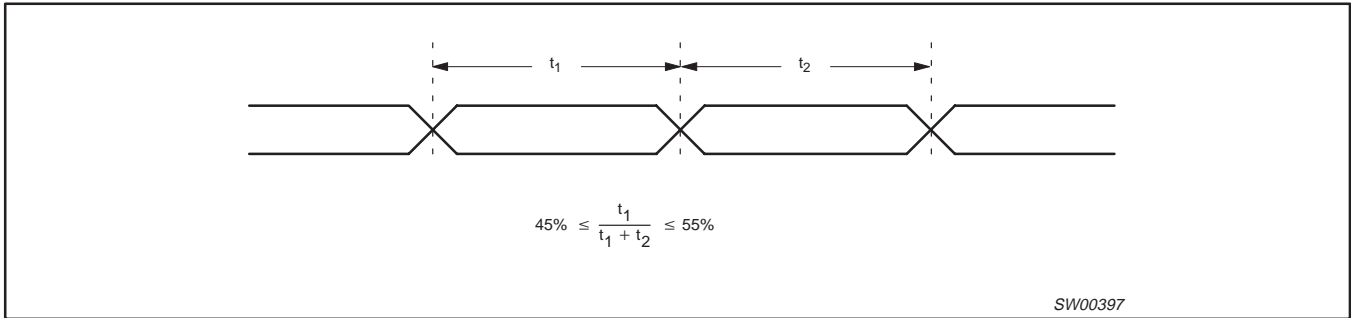


Figure 8. Duty cycle limits and measurement

## TEST CIRCUIT

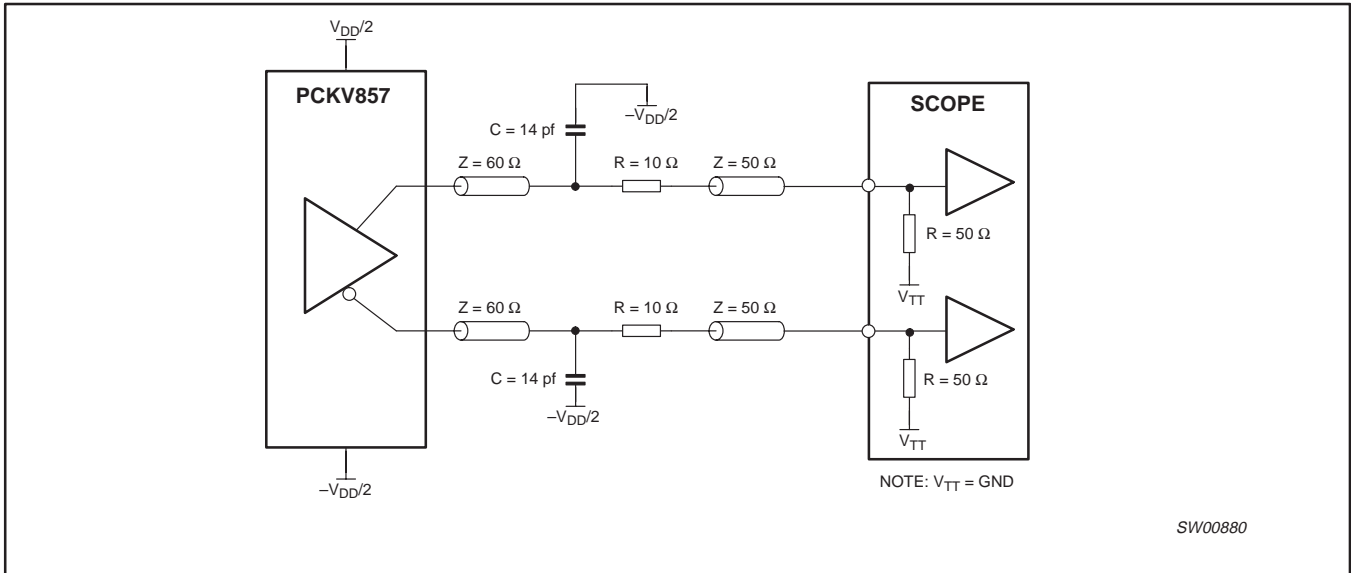


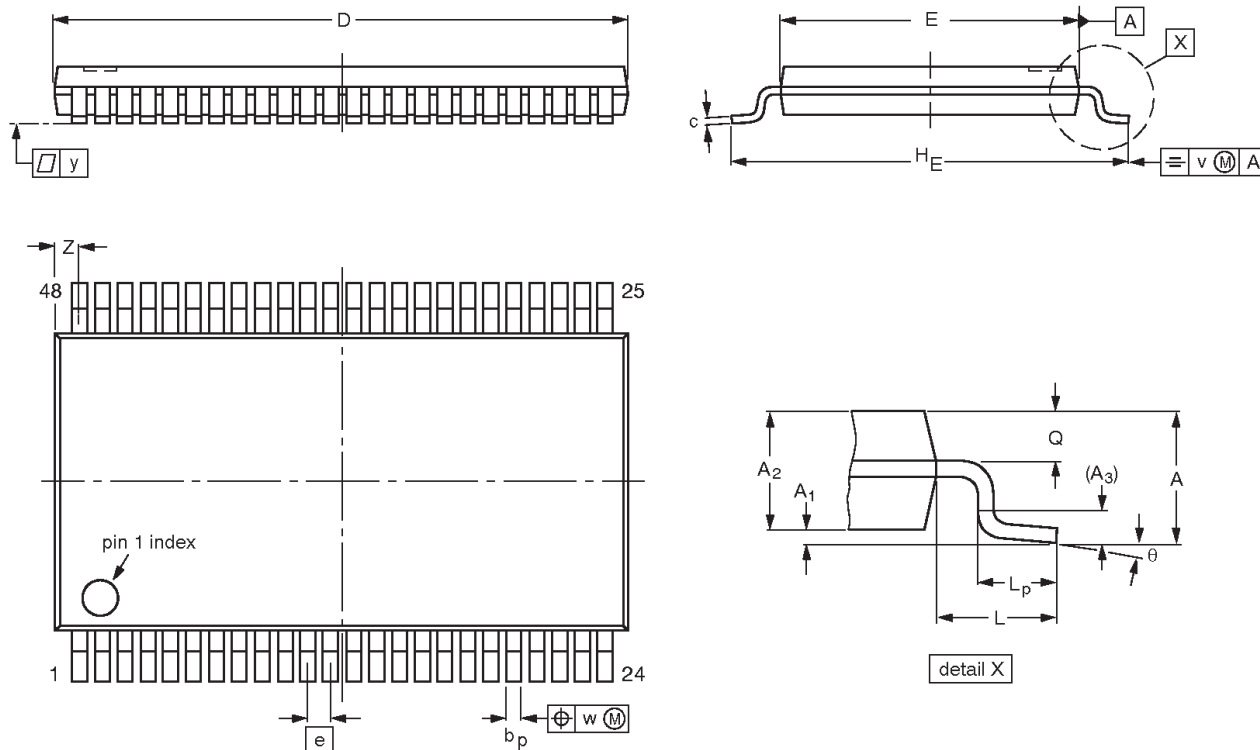
Figure 9. Output load test circuit

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

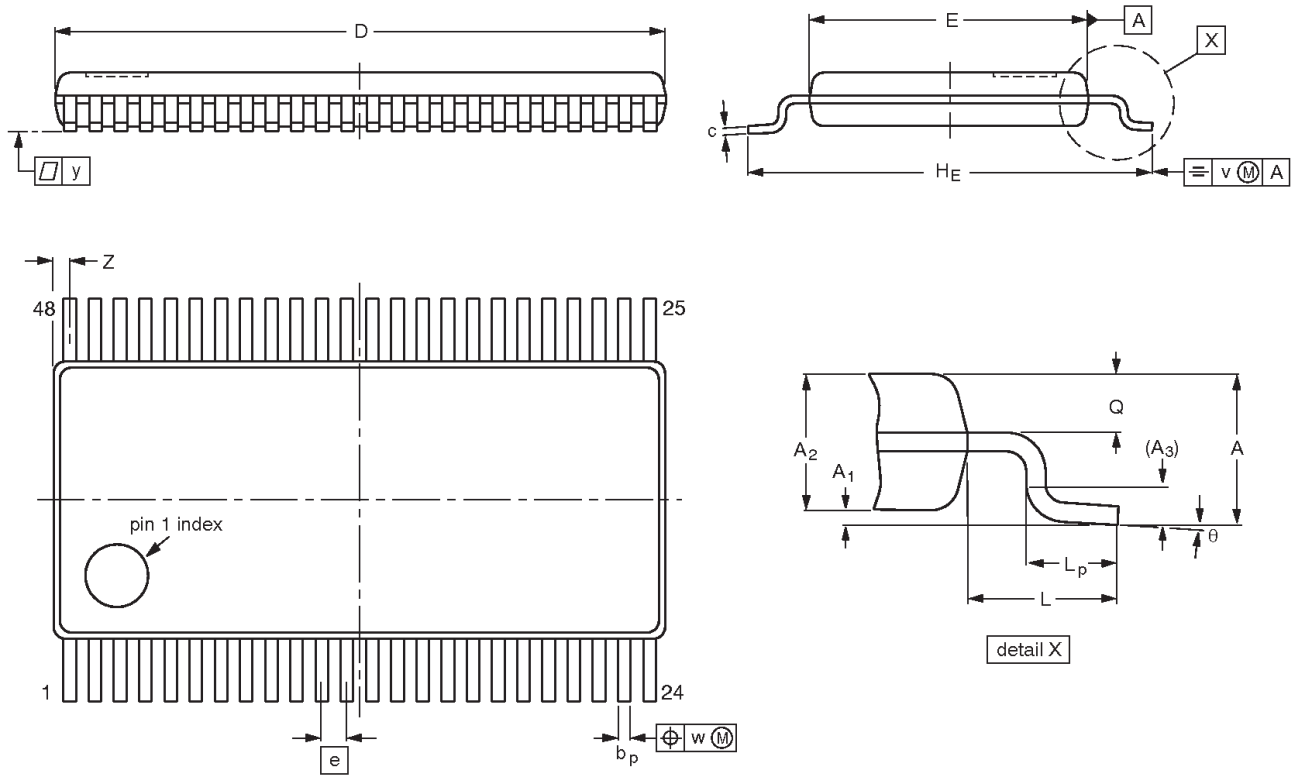
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

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TSSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D (1)	E (2)	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.80 9.60	4.50 4.30	0.40	6.60 6.20	1.00	0.70 0.50	0.40 0.30	0.20	0.07	0.08	0.40 0.10	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

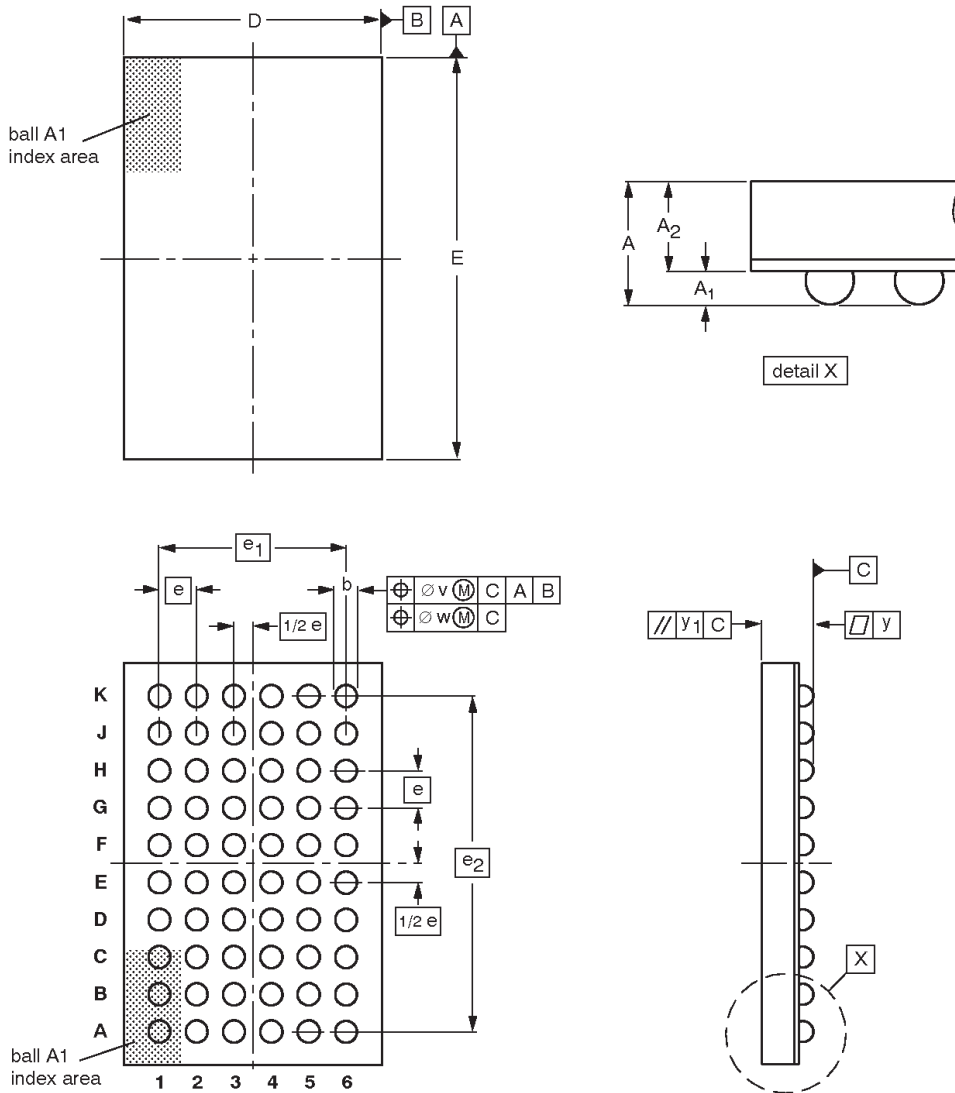
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT480-1		MO-153				97-03-20 99-12-27

70–190 MHz differential 1:10 clock driver

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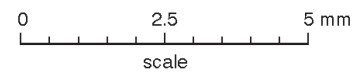
**VF8GA56:** plastic very thin fine-pitch ball grid array package; 56 balls;  
body 4.5 x 7 x 0.65 mm

**SOT702-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				-01-06-25- 02-08-08

## 70–190 MHz differential 1:10 clock driver

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**REVISION HISTORY**

Rev	Date	Description
_4	2002 Sep 06	Product data (9397 750 10343); fourth version supersedes Product data 2001 Dec 03. Engineering Change Notice 853-2242 28874 (2002 Sep 09). Modifications: Add new package option (VFBGA) to existing product data sheet.
_3	2001 Dec 03	Product data (9397 750 09244); third version

## 70–190 MHz differential 1:10 clock driver

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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<sup>[1]</sup> Please consult the most recently issued datasheet before initiating or completing a design.

<sup>[2]</sup> The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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