PCF2113x

LCD controllers/drivers

Rev. 04 — 4 March 2008 Product data sheet

1. General description

The PCF2113x is a low-power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 lines of 12 characters or 1 line of 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4-bit or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters.

The letter ‘x’ in PCF2113x characterizes the built-in character set. Various character sets can be manufactured on request.

2. Features

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user-defined symbols
- Icon mode for e.g. additional segment display section: reduced current consumption while displaying icons only
- Icon blink function
- Very low current consumption (20 µA to 200 µA):
  - Icon mode: < 25 µA
  - Power-down mode: < 2 µA
- On-chip:
  - Configurable 4, 3 or 2 voltage multiplier, generating LCD supply voltage V_{LCD}, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: –0.16 %/K to –0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters of 5 × 8 dots
- Character generator RAM: 16 characters of 5 × 8 dots; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4-bit or 8-bit parallel bus and 2-wire I^2C-bus interface
- 18 row and 60 column outputs

- Multiplex rates (MUX) 1:18 (for normal operation), 1:9 (for single-line operation) and 1:2 (for Icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range $V_{DD1} - V_{SS1}$ = 1.8 V to 5.5 V (chip may be driven with two battery cells)
- V_{LCD} generator supply voltage range $V_{DD2} - V_{SS2}$ = 2.2 V to 4.0 V
- Display supply voltage range $V_{LCD} - V_{SS2}$ = 2.2 V to 6.5 V
- Direct mode to save current consumption for Icon mode and MUX 1:9 (depending on V_{DD2} and LCD liquid properties)
- CMOS compatible
- **Remark:** Icon mode is a way to save current. When only icons are displayed (i.e. only the lower two rows are active), a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

3. Applications

- Telecom equipment
- Point-of-sale terminals
- Portable instruments

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2113AU/10/F4	-	chip on flexible film carrier	-
PCF2113DU/F4	-	chip in tray	-
PCF2113DH/4	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCF2113DU/2/F4	-	chip with bumps in tray	-
PCF2113EU/2/F4	-	chip with bumps in tray	-
PCF2113WU/2/F4	-	chip with bumps in tray	-

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF2113DH/4	PCF2113DH

6. Block diagram

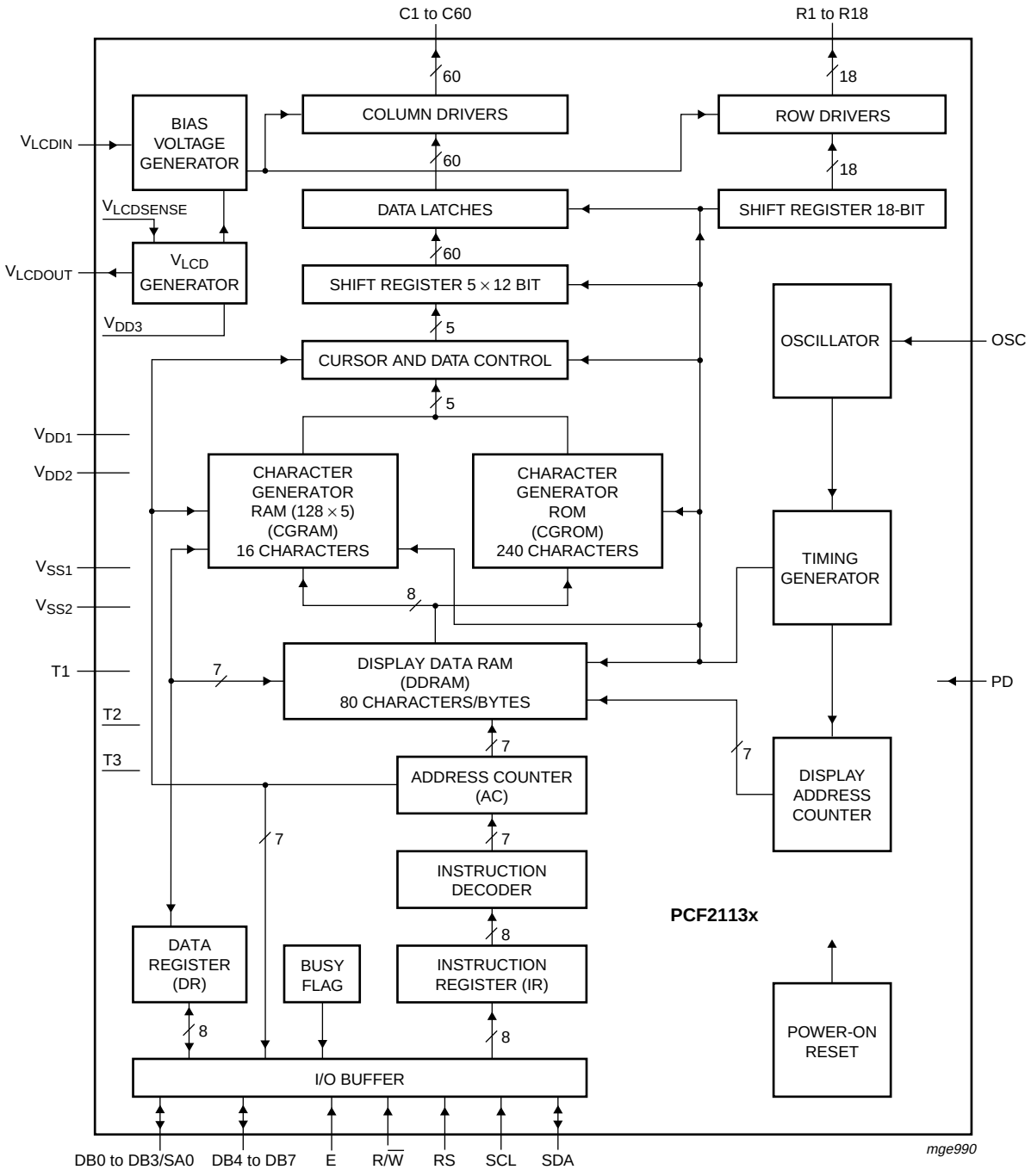


Fig 1. Block diagram of PCF2113x

7. Pinning information

7.1 Pinning

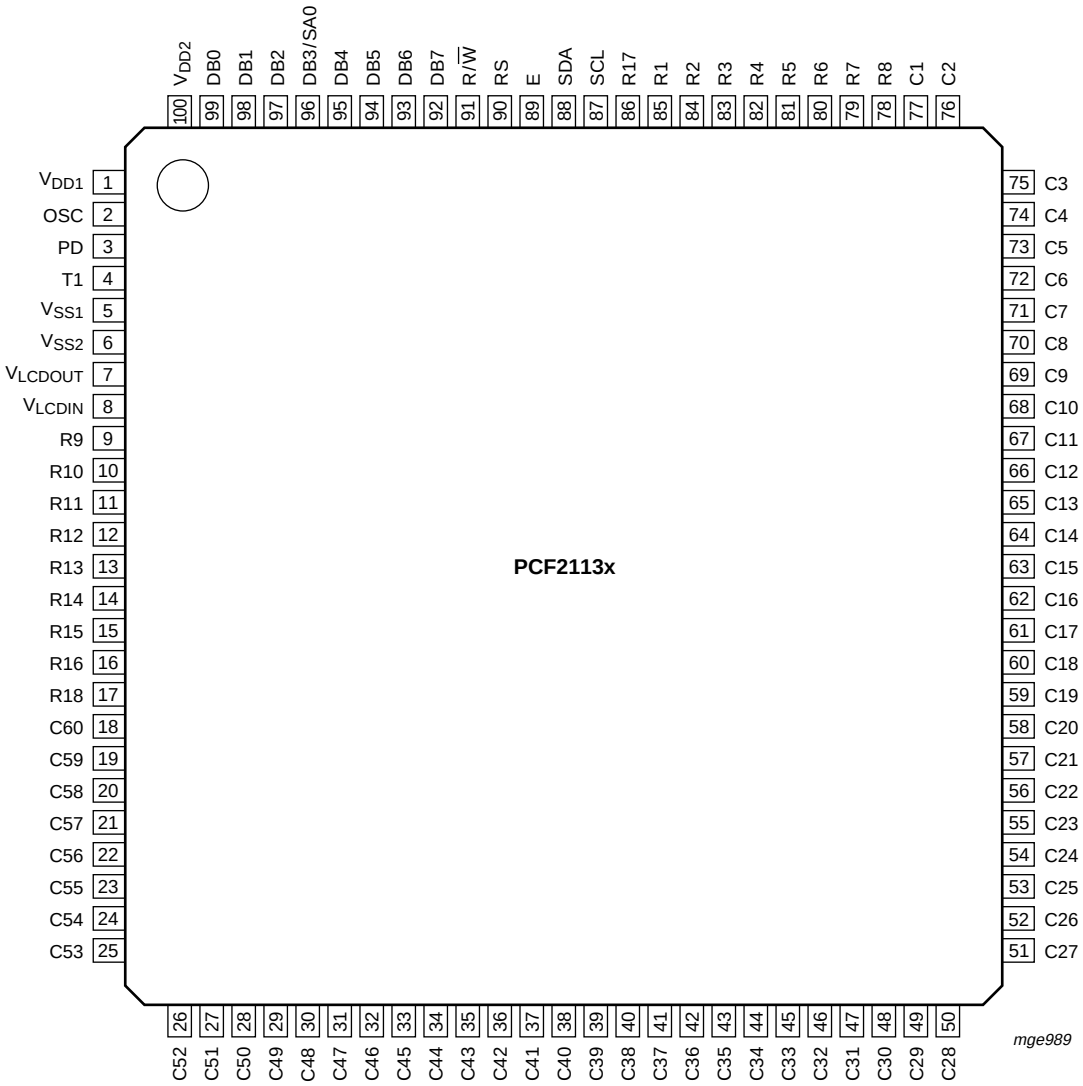


Fig 2. Pin configuration for PCF2113DH (LQFP100)

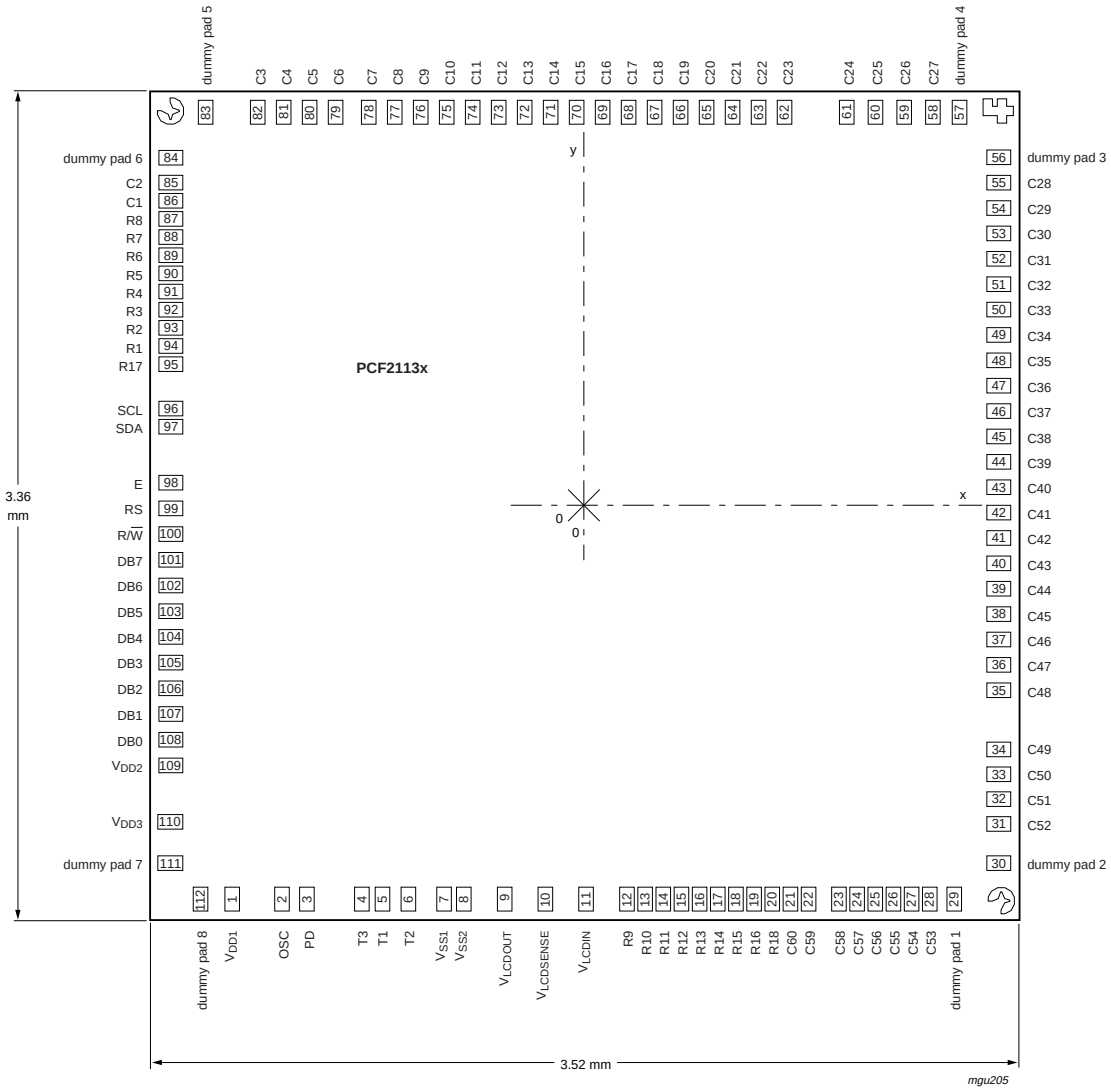


Fig 3. Bonding pad locations for PCF2113xU (bottom view)

Table 3. Pin (LQFP100 package) or pad allocation table

Pin	Pad	Symbol	Pin	Pad	Symbol
1	1	V_{DD1}	-	84	dummy pad
2	2	OSC	76	85	C2
3	3	PD	77	86	C1
-	4	T3	78 to 85	87 to 94	R8 to R1
4	5	T1	86	95	R17
-	6	T2	87	96	SCL
5	7	V_{SS1}	88	97	SDA
6	8	V_{SS2}	89	98	E
7	9	V_{LCDOUT}	90	99	RS
-	10	$V_{LCDSENSE}$	91	100	R/$\overline{W}$

Table 3. Pin (LQFP100 package) or pad allocation table *...continued*

Pin	Pad	Symbol	Pin	Pad	Symbol
8	11	V_{LCDIN}	92	101	DB7
9 to 16	12 to 19	R9 to R16	93	102	DB6
17	20	R18	94	103	DB5
18 to 25	21 to 28	C60 to C53	95	104	DB4
-	29	dummy pad	96	105	DB3/SA0
-	30	dummy pad	97	106	DB2
26 to 50	31 to 55	C52 to C28	98	107	DB1
-	56	dummy pad	99	108	DB0
-	57	dummy pad	100	109	V_{DD2}
51 to 75	58 to 82	C27 to C3	-	110	V_{DD3}
-	83	dummy pad	-	-	-

Table 4. Bonding pad dimensions

Pad	Size		Unit
Type	galvanic pure Au		
Bump dimensions	$(50 \pm 6) \times (90 \pm 6) \times (17.5 \pm 5)$		µm
Height difference in one die	< 2		µm
Convex deformation	< 5		µm
Pad size (aluminium)	62×100		µm
Passivation opening	36×76		µm
Pad pitch	–635.0		µm
Wafer thickness (excluding bumps)	380 ± 25		µm
	Fab 1 [1]	**Fab 2** [2]	
Die size X	3.52	3.47	mm
Die size Y	3.36	3.31	mm

[1] Fab 1 identification starts with nnnnnn, where n represents a number between 0 and 9 (8 inch wafer).

[2] Fab 2 identification starts with AXnnnn, where X represents a letter or a number and n represents a number between 0 and 9 (6 inch wafer).

Table 5. Pin and bonding pad description

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (µm)	Y (µm)	Description	
V_{DD1}	1	P	1	–1345	–1550	supply voltage 1 for all except V_{LCD} generator	
OSC	2	I	2	–1155	–1550	oscillator and external clock input	[1]
PD	3	I	3	–1055	–1550	power-down select input; for normal operation PD is LOW	
T3	-	I	4	–845	–1550	test pad; open circuit and not user accessible	
T1	4	I	5	–765	–1550	test pin; must be connected to V_{SS1}	
T2	-	I	6	–665	–1550	test pad; must be connected to V_{SS1}	
V_{SS1}	5	P	7	–525	–1550	ground 1 for all except V_{LCD} generator	

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description
V_{SS2}	6	P	8	–455	–1550	ground 2 for V_{LCD} generator
V_{LCDOUT}	7	O	9	–295	–1550	V_{LCD} output if V_{LCD} is generated internally [2]
$V_{LCDSENSE}$	-	I	10	–145	–1550	input (V_{LCD}) for voltage multiplier regulation [2][3]
V_{LCDIN}	8	I	11	15	–1550	input for generation of LCD bias levels [2]
R9	9	O	12	175	–1550	LCD row driver output
R10	10	O	13	245	–1550	LCD row driver output
R11	11	O	14	315	–1550	LCD row driver output
R12	12	O	15	385	–1550	LCD row driver output
R13	13	O	16	455	–1550	LCD row driver output
R14	14	O	17	525	–1550	LCD row driver output
R15	15	O	18	595	–1550	LCD row driver output
R16	16	O	19	665	–1550	LCD row driver output
R18	17	O	20	735	–1550	LCD row driver output
C60	18	O	21	805	–1550	LCD column driver output
C59	19	O	22	875	–1550	LCD column driver output
C58	20	O	23	995	–1550	LCD column driver output
C57	21	O	24	1065	–1550	LCD column driver output
C56	22	O	25	1135	–1550	LCD column driver output
C55	23	O	26	1205	–1550	LCD column driver output
C54	24	O	27	1275	–1550	LCD column driver output
C53	25	O	28	1345	–1550	LCD column driver output
dummy pad 1	-	-	29	1435	–1550	-
dummy pad 2	-	-	30	1630	–1395	-
C52	26	O	31	1630	–1255	LCD column driver output
C51	27	O	32	1630	–1155	LCD column driver output
C50	28	O	33	1630	–1055	LCD column driver output
C49	29	O	34	1630	–955	LCD column driver output
C48	30	O	35	1630	–735	LCD column driver output
C47	31	O	36	1630	–635	LCD column driver output
C46	32	O	37	1630	–535	LCD column driver output
C45	33	O	38	1630	–435	LCD column driver output
C44	34	O	39	1630	–335	LCD column driver output
C43	35	O	40	1630	–235	LCD column driver output
C42	36	O	41	1630	–135	LCD column driver output
C41	37	O	42	1630	–35	LCD column driver output
C40	38	O	43	1630	65	LCD column driver output
C39	39	O	44	1630	165	LCD column driver output
C38	40	O	45	1630	265	LCD column driver output
C37	41	O	46	1630	365	LCD column driver output

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description
C36	42	O	47	1630	465	LCD column driver output
C35	43	O	48	1630	565	LCD column driver output
C34	44	O	49	1630	665	LCD column driver output
C33	45	O	50	1630	765	LCD column driver output
C32	46	O	51	1630	865	LCD column driver output
C31	47	O	52	1630	965	LCD column driver output
C30	48	O	53	1630	1065	LCD column driver output
C29	49	O	54	1630	1165	LCD column driver output
C28	50	O	55	1630	1265	LCD column driver output
dummy pad 3	-	-	56	1630	1335	-
dummy pad 4	-	-	57	1435	1550	-
C27	51	O	58	1335	1550	LCD column driver output
C26	52	O	59	1225	1550	LCD column driver output
C25	53	O	60	1115	1550	LCD column driver output
C24	54	O	61	1005	1550	LCD column driver output
C23	55	O	62	765	1550	LCD column driver output
C22	56	O	63	665	1550	LCD column driver output
C21	57	O	64	565	1550	LCD column driver output
C20	58	O	65	465	1550	LCD column driver output
C19	59	O	66	365	1550	LCD column driver output
C18	60	O	67	265	1550	LCD column driver output
C17	61	O	68	165	1550	LCD column driver output
C16	62	O	69	65	1550	LCD column driver output
C15	63	O	70	–35	1550	LCD column driver output
C14	64	O	71	–135	1550	LCD column driver output
C13	65	O	72	–235	1550	LCD column driver output
C12	66	O	73	–335	1550	LCD column driver output
C11	67	O	74	–435	1550	LCD column driver output
C10	68	O	75	–535	1550	LCD column driver output
C9	69	O	76	–635	1550	LCD column driver output
C8	70	O	77	–735	1550	LCD column driver output
C7	71	O	78	–835	1550	LCD column driver output
C6	72	O	79	–965	1550	LCD column driver output
C5	73	O	80	–1065	1550	LCD column driver output
C4	74	O	81	–1165	1550	LCD column driver output
C3	75	O	82	–1265	1550	LCD column driver output
dummy pad 5	-	-	83	–1465	1550	-
dummy pad 6	-	-	84	–1630	1355	-
C2	76	O	85	–1630	1255	LCD column driver output

Table 5. Pin and bonding pad description *...continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 3).

Symbol	Pin	Type	Pad	X (μm)	Y (μm)	Description	
C1	77	O	86	−1630	1185	LCD column driver output	
R8	78	O	87	−1630	1115	LCD row driver output	
R7	79	O	88	−1630	1045	LCD row driver output	
R6	80	O	89	−1630	975	LCD row driver output	
R5	81	O	90	−1630	905	LCD row driver output	
R4	82	O	91	−1630	835	LCD row driver output	
R3	83	O	92	−1630	765	LCD row driver output	
R2	84	O	93	−1630	695	LCD row driver output	
R1	85	O	94	−1630	625	LCD row driver output	
R17	86	O	95	−1630	555	LCD row driver output	
SCL	87	I	96	−1630	375	I^2C-bus serial clock input	[4]
SDA	88	I/O	97	−1630	305	I^2C-bus serial data input/output	[4]
E	89	I	98	−1630	85	data bus clock input	[4]
RS	90	I	99	−1630	−15	register select input	
R/$\overline{W}$	91	I	100	−1630	−115	read or write input	
DB7	92	I/O	101	−1630	−215	8-bit bidirectional bus bit 7	[5]
DB6	93	I/O	102	−1630	−315	8-bit bidirectional bus bit 6	
DB5	94	I/O	103	−1630	−415	8-bit bidirectional bus bit 5	
DB4	95	I/O	104	−1630	−515	8-bit bidirectional bus bit 4	
DB3/SA0	96	I/O	105	−1630	−615	8-bit bidirectional bus bit 3 or I^2C-bus address input	[4][5]
DB2	97	I/O	106	−1630	−715	8-bit bidirectional bus bit 2	
DB1	98	I/O	107	−1630	−815	8-bit bidirectional bus bit 1	
DB0	99	I/O	108	−1630	−915	8-bit bidirectional bus bit 0	
V_{DD2}	100	P	109	−1630	−1015	supply voltage 2 for V_{LCD} generator	[6]
V_{DD3}	-	P	110	−1630	−1235	supply voltage 3 for V_{LCD} generator	[3][6]
dummy pad 7	-	-	111	−1630	−1395	-	
dummy pad 8	-	-	112	−1465	−1550	-	

[1] When the on-chip oscillator is used this pad must be connected to V_{DD1}.

[2] When V_{LCD} is generated internally, pins V_{LCDIN}, V_{LCDOUT} and $V_{LCDSENSE}$ must be connected together. When an external V_{LCD} is supplied, this should be done via V_{LCDIN}. In this case only pins V_{LCDOUT} and $V_{LCDSENSE}$ must be connected together.

[3] In the LQFP100 version this signal is connected internally and is not accessible.

[4] When the I^2C-bus is used, the parallel interface pin E must be LOW. In the I^2C-bus read mode pins DB7 to DB0 must be connected to V_{DD1} or left open-circuit.

When the parallel bus is used, the pins SCL and SDA must be connected to pin V_{SS1} or pin V_{DD1}; they must not be left open-circuit.

When the 4-bit interface is used without reading out from the PCF2113x (bit R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be connected to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

[5] DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the four higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit except for I^2C-bus operations (see Table note 4).

[6] V_{DD2} and V_{DD3} must always be equal.

8. Functional description

8.1 LCD supply voltage generator

The LCD supply voltage (V_{LCD}) may be generated on-chip. The V_{LCD} generator is controlled by two internal 6-bit registers: VA and VB. Section 10.10.1 shows how to program these registers. The nominal LCD operating voltage at room temperature is given by the relationship:

$V_{oper(nom)}$ = (integer value of register $\times$ 0.08 V) + 1.82 V

With a programmed value from 1 to 63, $V_{oper(nom)}$ = 1.90 V to 6.86 V at T_{amb} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} tolerance and temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and therefore are not allowed.

Value 0 for VA and VB switches off the generator (i.e. VA = 0 in Character mode, VB = 0 in Icon mode).

Usually register VA is programmed with the voltage for Character mode and register VB with the voltage for Icon mode.

When V_{LCD} is generated on-chip, the V_{LCD} pins must be decoupled to V_{SS} with a suitable capacitor.

The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the V_{LCD} generator and the Direct mode are switched off, an external voltage may be supplied at pins V_{LCDIN} and V_{LCDOUT} (which are connected together). V_{LCDIN} and V_{LCDOUT} may be higher or lower than V_{DD2}.

During Direct mode (program DM bit) the internal V_{LCD} generator is turned off and the V_{LCDOUT} output voltage is directly connected to V_{DD2}. This reduces the current consumption during Icon mode and MUX 1:9 (depending on V_{DD2} and LCD liquid properties).

The V_{LCD} generator ensures that, as long as V_{DD} is in the valid range (2.2 V to 4 V), the required peak operating voltage of 6.5 V can be generated at any time.

8.2 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for 1:18 maximum rate allows V_{LCD} < 5 V for most LCD liquids. The intermediate bias levels for the different multiplex rates are shown in Table 6. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 6. Bias levels as a function of multiplex rate

Multiplex rate	Number of levels	Bias voltages[1]					
		V_1	V_2	V_3	V_4	V_5	V_6
1:18	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1:9	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1:2	4	V_{LCD}	$^2/_3$	$^2/_3$	$^1/_3$	$^1/_3$	V_{SS}

[1] The values in the table are given relative to $V_{LCD} - V_{SS}$, e.g. $^3/_4$ means $\{^3/_4 \times (V_{LCD} - V_{SS})\} + V_{SS}$.

8.3 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD1}.

8.4 External clock

If an external clock is to be used, this input is at the OSC pin. The resulting display frame frequency is given by: $f_{fr(LCD)} = \frac{f_{osc}}{3072}$

Only in the Power-down mode is the clock allowed to be stopped (pin OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

8.5 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed.

8.6 Registers

The PCF2113x has two 8-bit registers: an Instruction Register (IR) and a Data Register (DR). The Register Select (RS) signal determines which register will be accessed. The instruction register stores instruction codes such as ‘display clear’, ‘cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to but not read from by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the ‘read data’ instruction.

8.7 Busy flag

The busy flag indicates the internal status of the PCF2113x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when bit RS = 0 and bit R/$\overline{W}$ = 1. Instructions must only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

8.8 Address counter

The Address Counter (AC) assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands ‘set DDRAM address’ and ‘set CGRAM address’. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when bit RS = 0 and bit R/$\overline{W}$ = 1.

8.9 Display data RAM

The Display Data RAM (DDRAM) stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Figure 4. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00h in line 1 are displayed. Figure 5 and Figure 6 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 7.

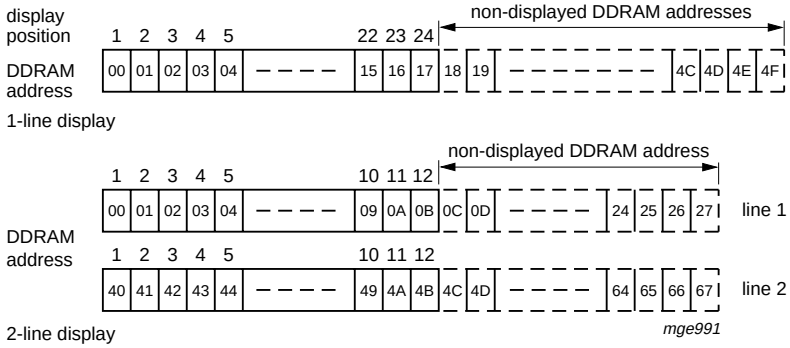


Fig 4. DDRAM to display mapping: no shift

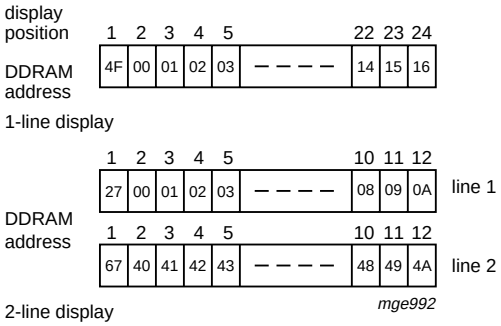


Fig 5. DDRAM to display mapping: right shift

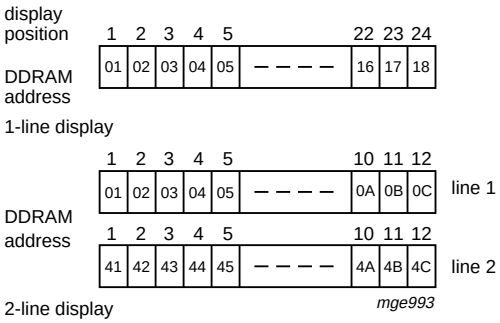


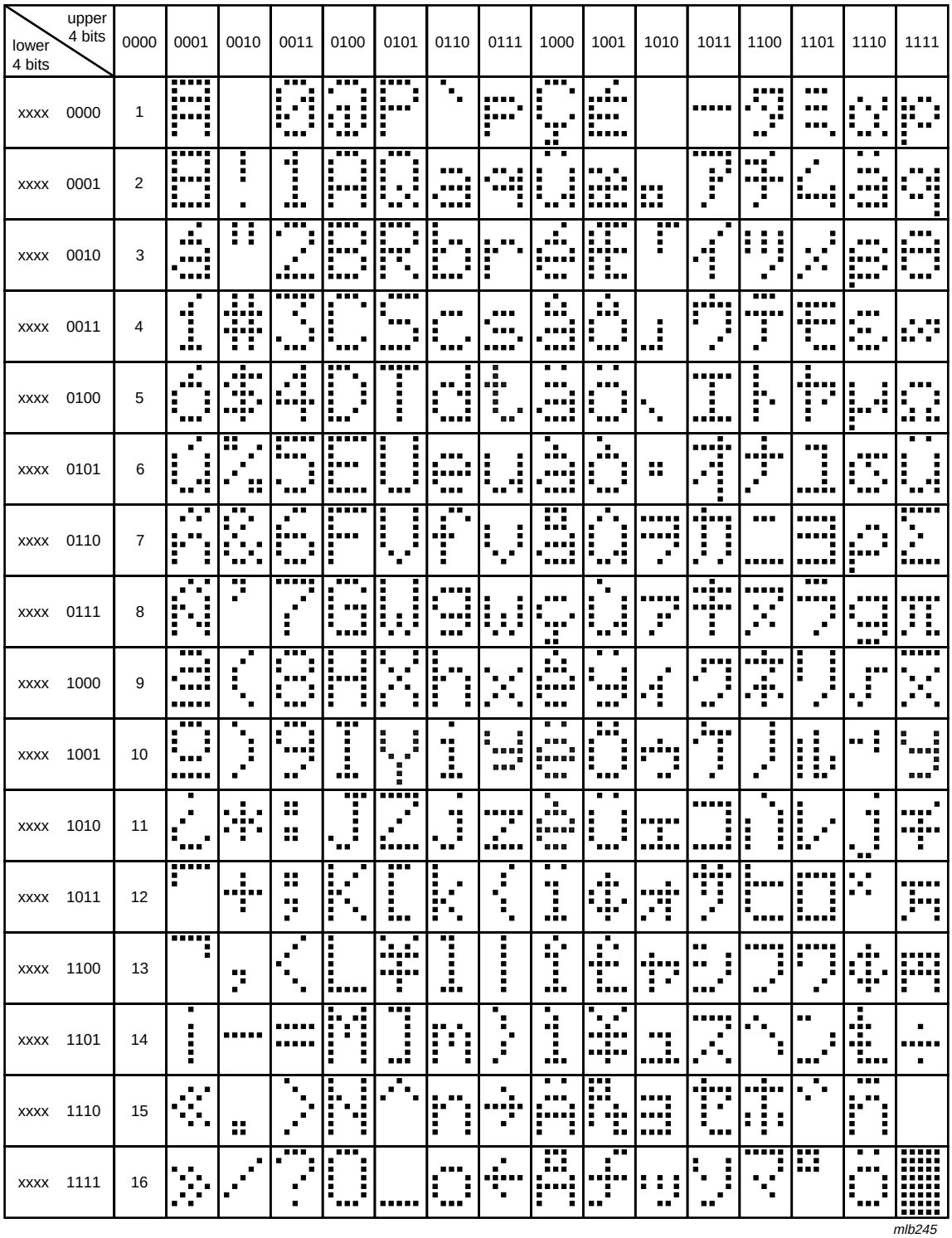
Fig 6. DDRAM to display mapping: left shift

Table 7. Address space and wrap-around operation

Mode	1 × 24	2 × 12	1 × 12
Address space	00h to 4Fh	00h to 27h; 40h to 67h	00h to 27h
Read/write wrap-around (moves to next line)	4Fh to 00h	27h to 40h; 67h to 00h	27h to 00h
Display shift wrap-around (stays within line)	4Fh to 00h	27h to 00h; 67h to 40h	27h to 00h

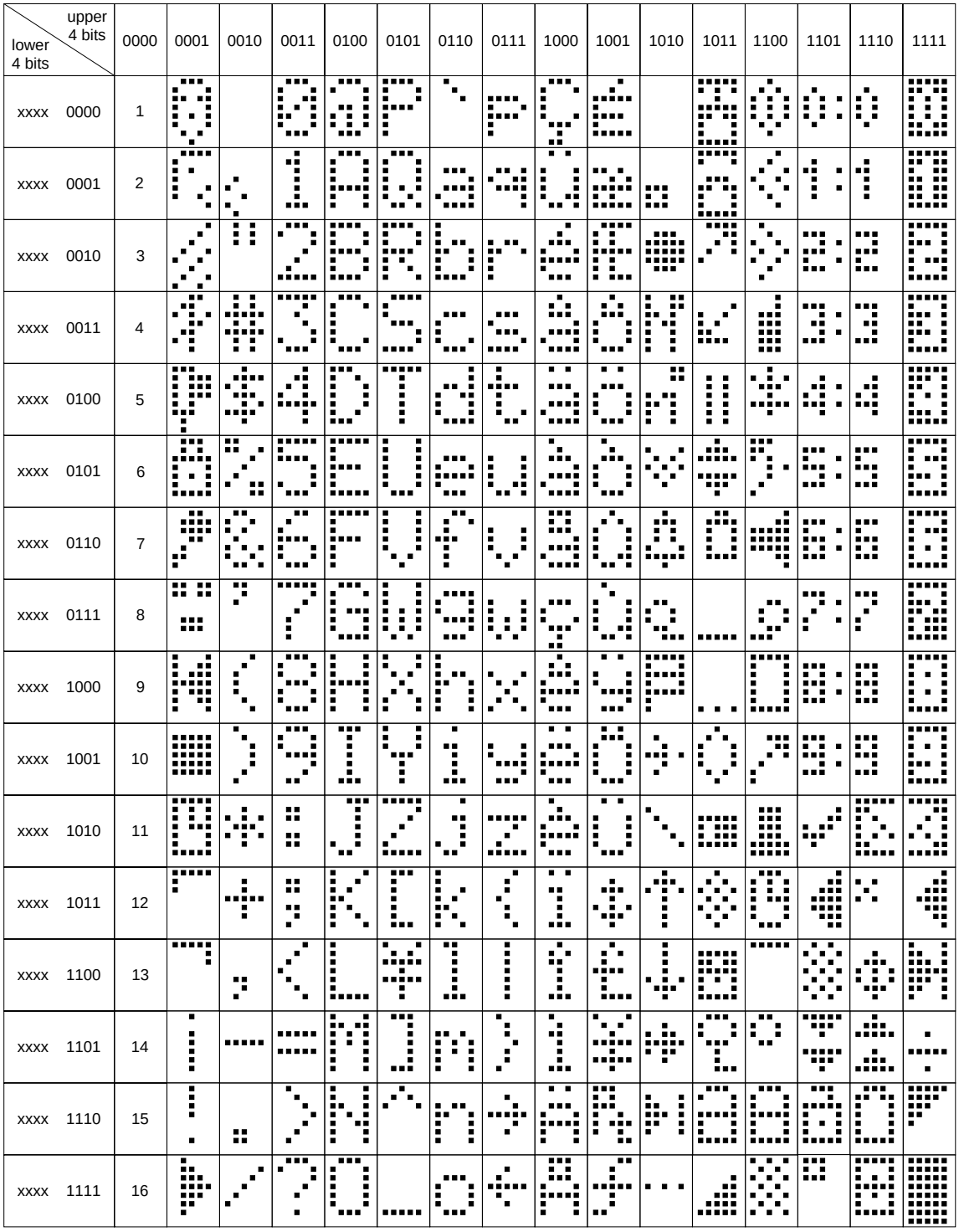
8.10 Character generator ROM

The Character Generator ROM (CGROM) generates 240 character patterns in a 5 × 8 dot format from 8-bit character codes. Figure 7, Figure 8, Figure 9 and Figure 10 show the character sets that are currently implemented.



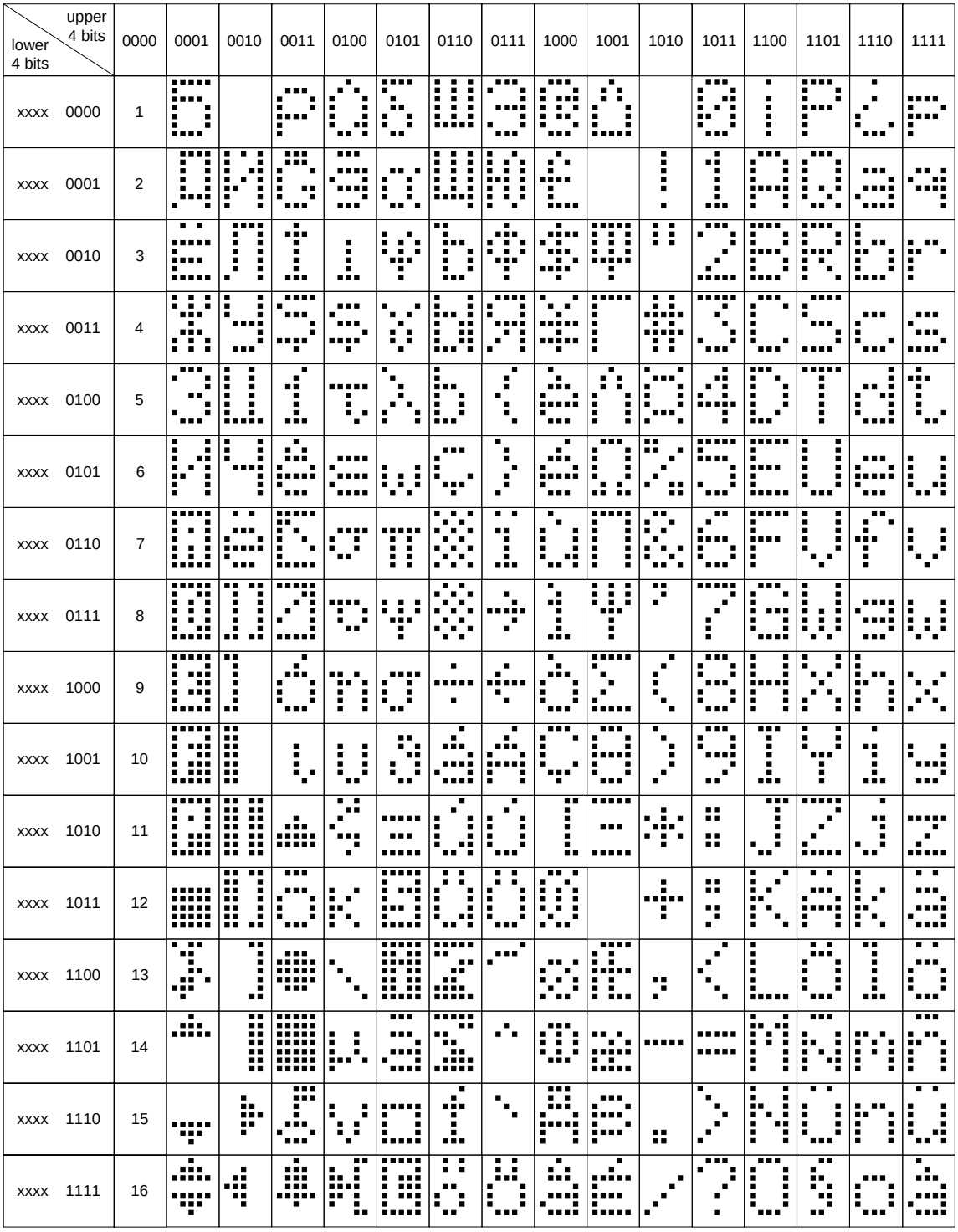
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 7. Character set ‘A’ in CGROM



The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 8. Character set ‘D’ in CGROM



mgd689

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 9. Character set ‘E’ in CGROM

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

mgu204

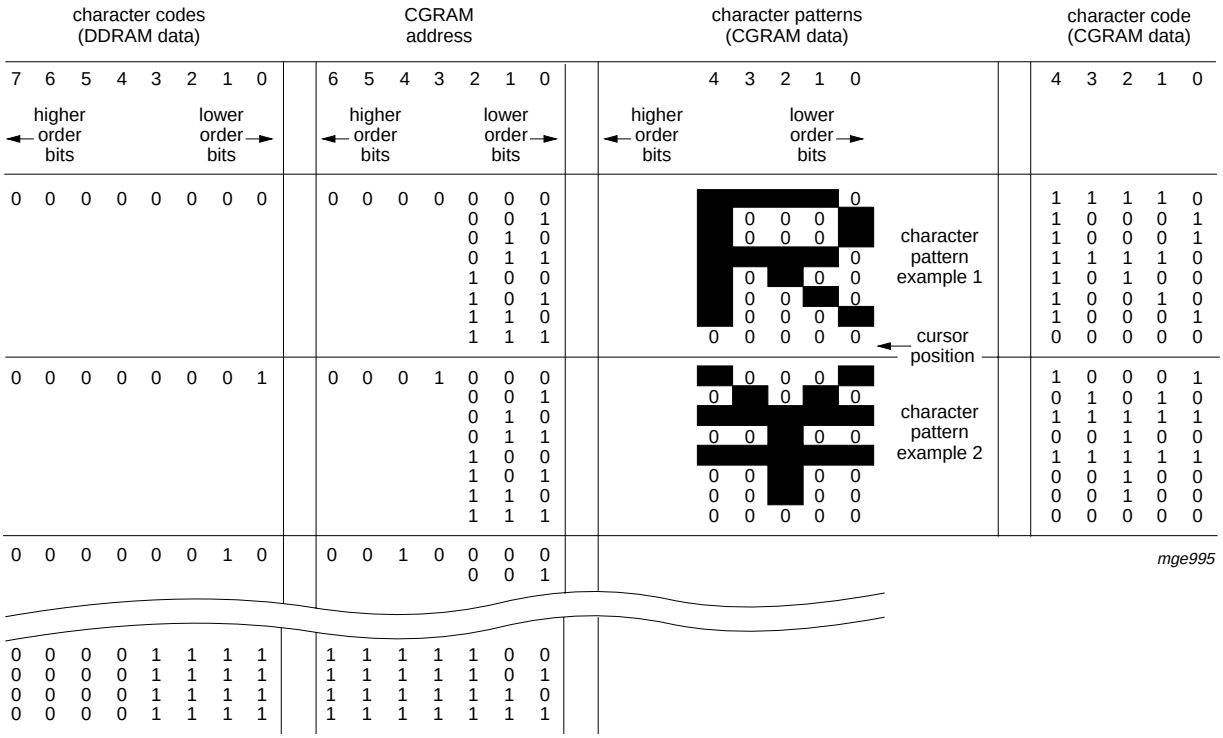
The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 10. Character set ‘W’ in CGROM

8.11 Character generator RAM

Up to 16 user-defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Figure 18 and Figure 19) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Figure 7, Figure 8, Figure 9 and Figure 10).

Figure 11 shows the addressing principle for the CGRAM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logic OR with the cursor. Data in the 8th position appears in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in this figure.

CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘set CGRAM address’ command. Bit 6 can be set using the ‘set DDRAM address’ command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘read busy flag’ and ‘address counter’ command.

Fig 11. Relationship between CGRAM addresses, data and display patterns

8.12 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Figure 12 at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

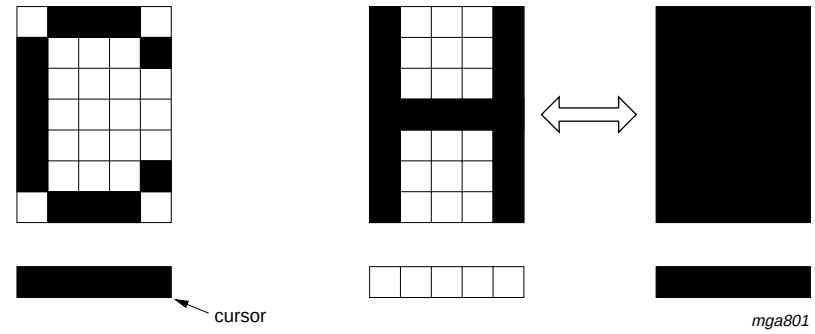
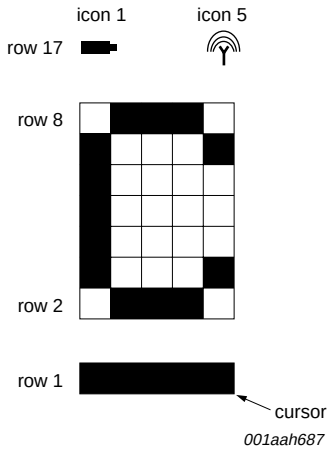


Fig 12. Cursor and blink display examples



Bit Q = 1

Fig 13. Example of a display with icons

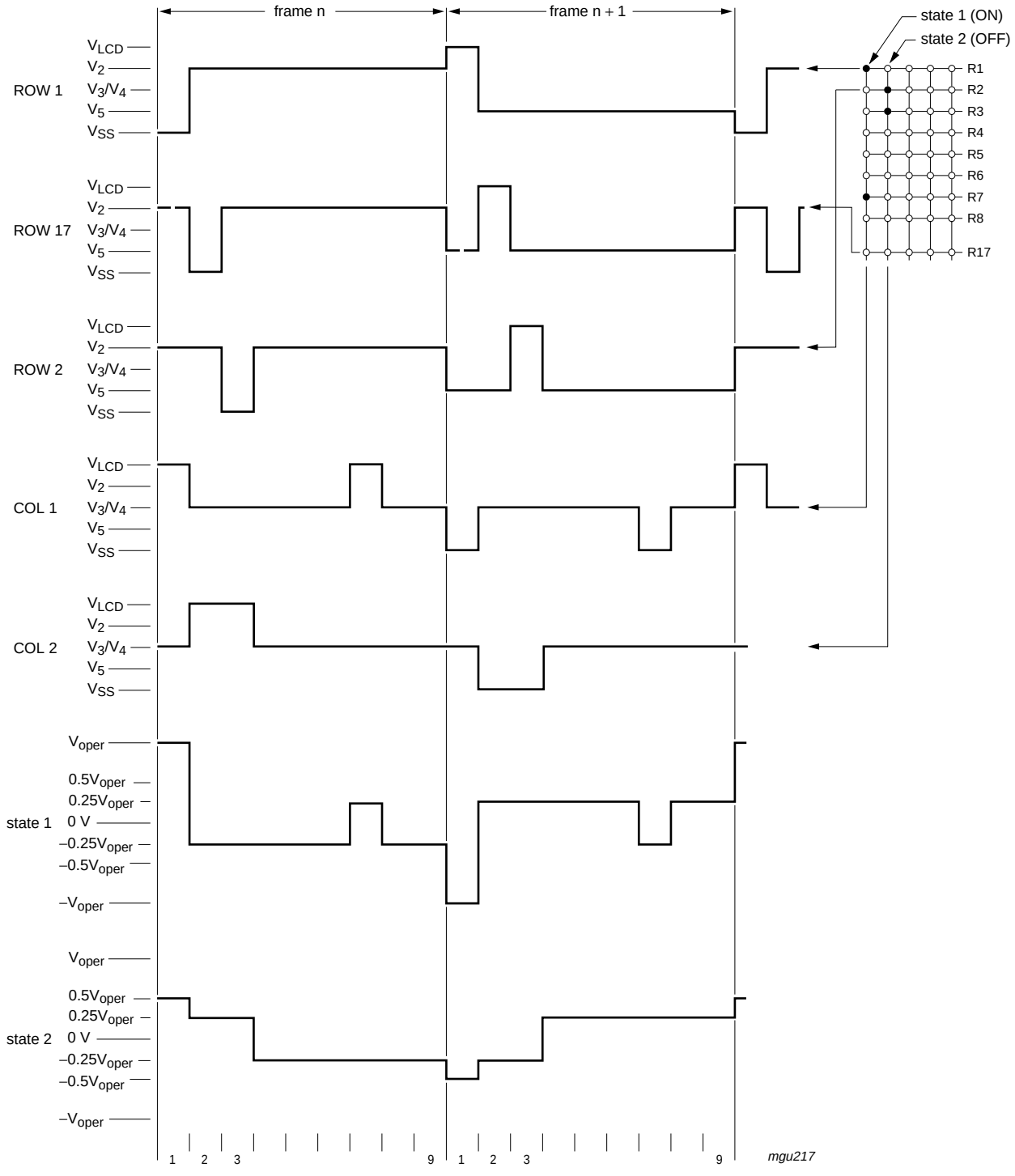
8.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.14 LCD row and column drivers

The PCF2113x contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figure 14, Figure 15, Figure 16 and Figure 17 show typical waveforms. Unused outputs should be left unconnected.



R9 to R16 and R18 to be left open

Fig 14. MUX 1:9 LCD waveforms; Character mode

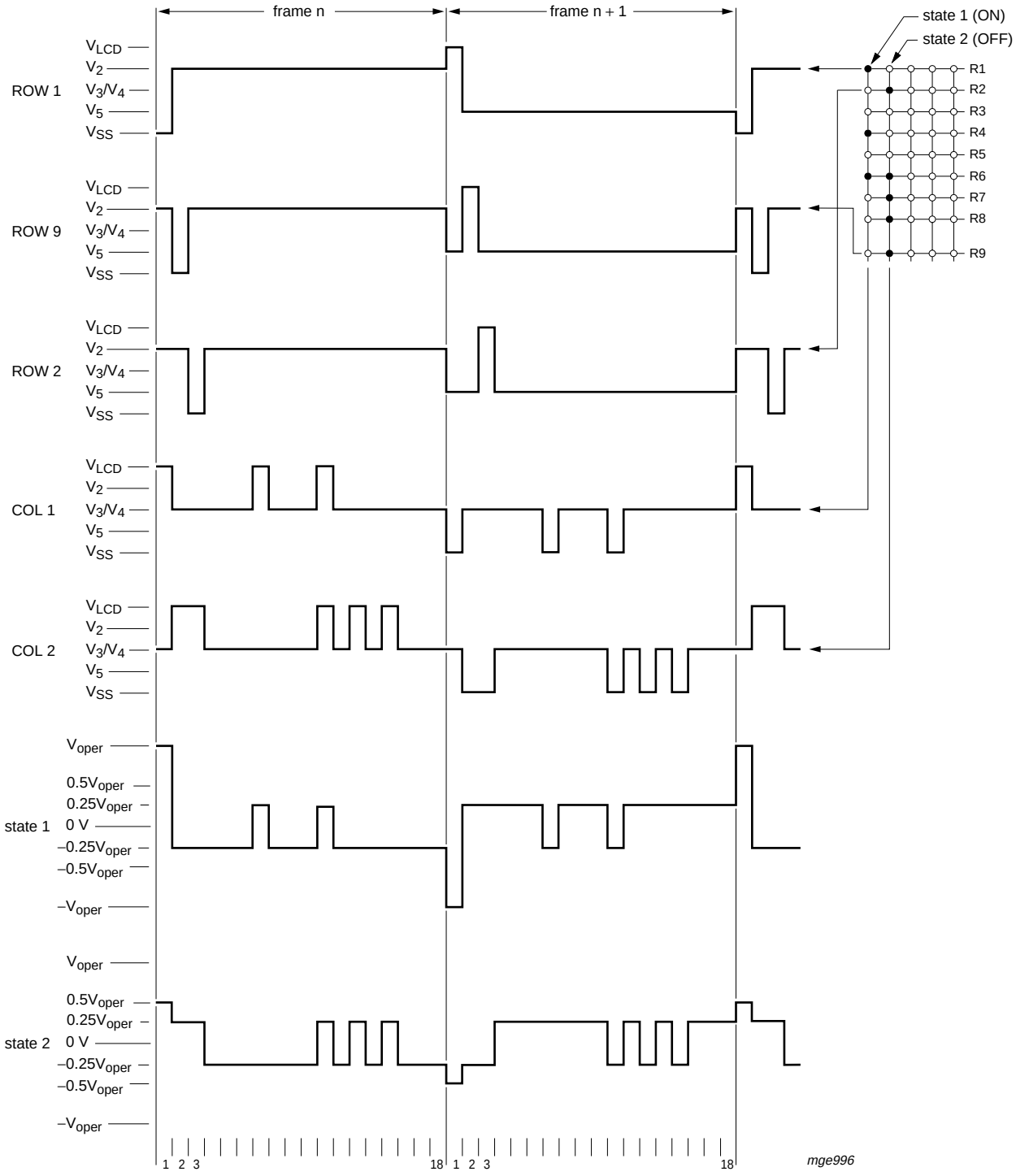


Fig 15. MUX 1:18 LCD waveforms; Character mode

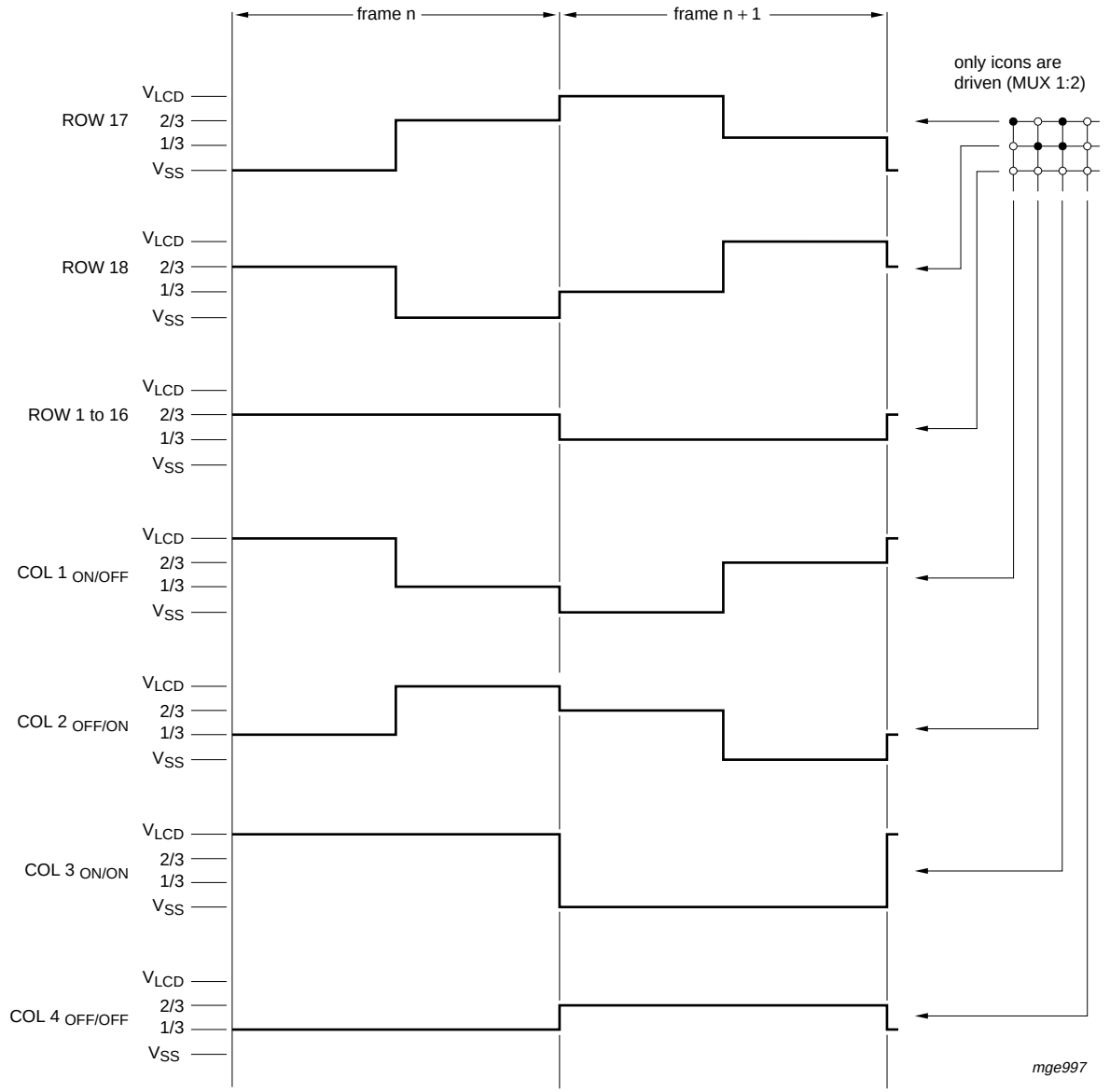
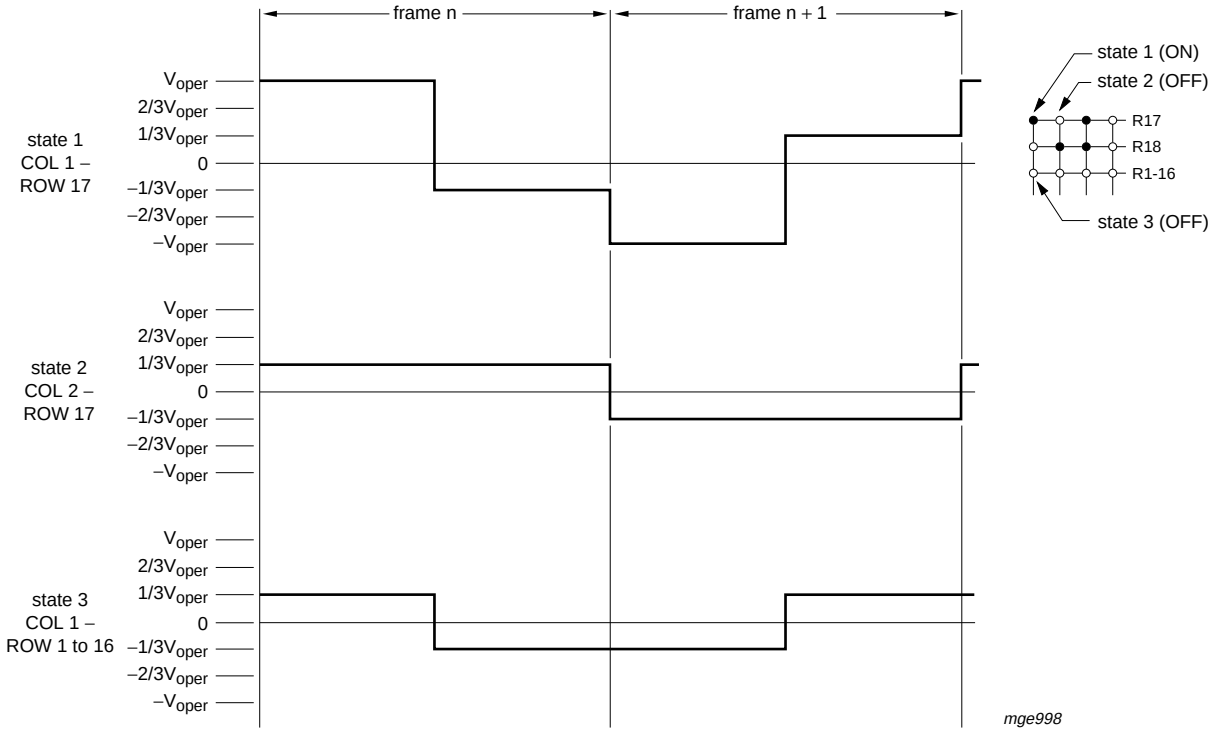


Fig 16. MUX 1:2 LCD waveforms; Icon mode (a)



$V_{on(RMS)} = 0.745V_{oper}$

$V_{off(RMS)} = 0.333V_{oper}$

$$D = \frac{V_{on}}{V_{off}} = 2.23$$

Fig 17. MUX 1:2 LCD waveforms; Icon mode (b)

8.15 Power-down mode

The chip can be put into Power-down mode by applying an external HIGH level to the PD pin. In Power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when pin OSC is externally clocked.

8.16 Reset function

The PCF2113x automatically initializes (resets) when power is turned on. The chip executes a reset sequence, including a ‘clear display’, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 8.

Table 8. State after reset

Step	Function	Control bit state	Conditions
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1:18 mode
5	default address pointer to DDRAM	the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends	the busy state lasts 2 ms; the chip may also be initialized by software; see Table 26 (8-bit interface) and Table 27 (4-bit interface).
6	icon control	IM = 0; IB = 0; DM = 0	icons, icon blink and Direct mode disabled
7	display or screen configuration	L = 0; P = 0; Q = 0	default configurations
8	V_{LCD} temperature coefficient	TC1 = 0; TC2 = 0	default temperature coefficient
9	set V_{LCD}	VA = 0; VB = 0	V_{LCD} generator off
10	I^2C-bus interface reset		
11	set HVgen stages	S1 = 1; S0 = 0	V_{LCD} generator voltage multiplier set at factor 4

9. Instructions

Only two PCF2113x registers, the Instruction Register (IR) and the Data Register (DR), can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interfacing to various types of microcontrollers which operate at different speeds or to allow interfacing to peripheral control ICs.

The instruction set for I^2C-bus commands is given in Table 9. Section 11.2.1 discusses how these control and command bytes are embedded in the I^2C-bus protocol.

Table 9. Instruction set for I^2C-bus commands

I^2C-bus commands	Control byte								Command byte								I^2C-bus commands
[1]	Co[2]	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	[1]

[1] R/$\overline{W}$ is set together with the slave address.

[2] For explanation, see Table 11.

The PCF2113x operation is controlled by the instructions shown in Table 10 together with their execution time. Details are explained in subsequent sections.

There are 4 types of instructions:

- Designate PCF2113x functions such as display format, data length
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Other functions

In normal use, data transfer instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the ‘read busy flag’ and ‘read address’ instructions will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, check to ensure it is logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 10. An instruction sent while the busy flag is logic 1 will not be executed.

Table 10. Instruction set with parallel bus commands

Instruction	Control and command bits										Description[1]	Required clock cycles
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
H = 0 or 1 (basic and extended functions)												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL), number of display lines (M), single line/MUX 1:9 (SL) and extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	AC							reads the Busy Flag (BF), indicating internal operating is being performed, and the Address Counter (AC)	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data to CGRAM or DDRAM	3
H = 0 (basic functions)												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3

Table 10. Instruction set with parallel bus commands *…continued*

Instruction	Control and command bits										Description[1]	Required clock cycles
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction (I/D) and specifies shift of display (S); these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B)	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor or shifts display (S/C) to right or left (R/L) without changing the DDRAM contents	3
Set CGRAM address	0	0	0	1	ACG						sets CGRAM address; bit DB6 is to be set by the command ‘set DDRAM address’; the descriptions of the commands provide details	3
Set DDRAM address	0	0	1	ADD							sets DDRAM address	3
H = 1 (extended functions)												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	-
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration (L)	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration, columns (P) and rows (Q)	3
Icon control	0	0	0	0	0	0	1	IM	IB	DM	set Icon mode (IM), icon blink (IB), Direct mode (DM)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TC1 and TC2)	3
Set HVgen stages	0	0	0	1	0	0	0	0	S1	S0	set internal V_{LCD} generator voltage multiplier stages (S1 = 1 and S0 = 1 are not allowed)	3
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register VA or in register VB (V)	3

[1] For explanation of symbols, see Table 11.

Table 11. Explanation of symbols

Bit	Logic 0	Logic 1
Co	last control byte	another control byte follows after data/command
RS	select instruction register	select data register
DL	data length: 4 bits	data length: 8 bits
M (no impact if SL = 1)	1 line × 24 character display	2 line × 12 character display
SL	MUX 1:18 (1 line × 24 character or 2 line × 12 character display)	MUX 1:9 (1 line × 12 character display)
H	use basic instruction set	use extended instruction set
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off; character at cursor position does not blink	cursor character blink on; character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
L (no impact if M = 1 or SL = 1)	left/right screen; standard connection	left/right screen; mirrored connection
	1st 12 characters of 24; columns are from 1 to 60	1st 12 characters of 24; columns are from 60 to 1
	2nd 12 characters of 24; columns are from 1 to 60	2nd 12 characters of 24; columns are from 60 to 1
P	column data; left to right; column data is displayed from 1 to 60	column data; right to left; column data is displayed from 60 to 1
Q	row data; top to bottom; row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data; top to bottom; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	Character mode; full display	Icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
DM	Direct mode disabled	Direct mode enabled
V	set VA	set VB

9.1 Clear display

‘Clear display’ writes character code 20h into all DDRAM addresses (the character pattern for character code 20h must be a blank pattern), sets the DDRAM address counter to 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction ‘clear display’ requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM address counter to 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 Bit I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

9.3.2 Bit S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM.

When S = 0, the display does not shift.

9.4 Display control (and partial Power-down mode)

9.4.1 Bit D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D = 1.

When the display is off (D = 0) the chip is in partial Power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards the oscillator can be stopped. If the oscillator is running during partial Power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (pin OSC = V_{SS}).

To ensure $I_{DD} < 1$ µA, pin PD and the parallel bus pins DB7 to DB0 should be connected to V_{DD}, pins RS and R/$\overline{W}$ to V_{DD} or left open-circuit.

Recovery from Power-down mode: connect pin PD back to V_{SS}, if necessary pin OSC back to V_{DD} and send a 'display control' instruction with D = 1.

9.4.2 Bit C

The cursor is displayed when C = 1 and inhibited when C = 0. The cursor is displayed using 5 dots in the 8th line (see Figure 12). Even if the cursor disappears, the display functions like I/D, remain in operation during display data write.

9.4.3 Bit B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{blink} = \frac{f_{osc}}{104448}$ Hz.

The cursor underline and the cursor character blink can be set to display simultaneously.

9.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor display shift'.

9.6 Function set

9.6.1 Bit DL (parallel mode only)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on M, SL and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set M, SL and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

9.6.2 Bit M

Selects either 1 line × 24 character display (M = 0) or 2 line × 12 character display (M = 1).

9.6.3 Bit SL

Selects MUX 1:9, 1 line × 12 character display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2 line × 12 character display mode, however, the second line is not displayed.

9.6.4 Bit H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons, as shown in Section 10.

9.7 Set CGRAM address

'Set CGRAM address' writes bits DB5 to DB0 of the CGRAM address ACG into the address counter (A5h to A0h). Data can then be written to or read from the CGRAM.

Remark: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (A6h to A0h). With the ‘set CGRAM address’ command, only bits DB5 to DB0 are set. Bit DB6 can be set using the ‘set DDRAM address’ command first, or by using the auto-increment feature during CGRAM write. All bits DB6 to DB0 can be read using the ‘read busy flag’ and ‘read address’ command.

When writing to the lower part of the CGRAM, ensure that bit DB6 of the address is not set (e.g. by an earlier DDRAM write or read action).

9.8 Set DDRAM address

‘Set DDRAM address’ writes the DDRAM address ADD into the address counter (A6h to A0h). Data can then be written to or read from the DDRAM.

9.9 Read busy flag and read address

‘Read busy flag and address counter’ reads the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter (A6h to A0h) is read out, into DB6 to DB0. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

‘Write data’ writes binary 8-bit data DB7 to DB0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous ‘set CGRAM address’ or ‘set DDRAM address’ command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits DB4 to DB0 of CGRAM data are valid, bits DB7 to DB5 are ‘not relevant’.

9.11 Read data from CGRAM or DDRAM

‘Read data’ reads binary 8-bit data DB7 to DB0 from the CGRAM or DDRAM.

The most recent ‘set address’ command determines whether the CGRAM or DDRAM is to be read.

The ‘read data’ instruction gates the content of the Data Register (DR) to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the DR:

- ‘Set CGRAM address’
- ‘Set DDRAM address’
- ‘Read data’ from CGRAM or DDRAM

Other instructions (e.g. ‘write data’, ‘cursor/display shift’, ‘clear display’ and ‘return home’) do not modify the data register content.

10. Extended function set instructions and features

10.1 New instructions

H = 1 sets the chip into Extended instruction set mode.

10.2 Icon control

The PCF2113x can drive up to 120 icons. See Figure 18 and Figure 19 for CGRAM to icon mapping.

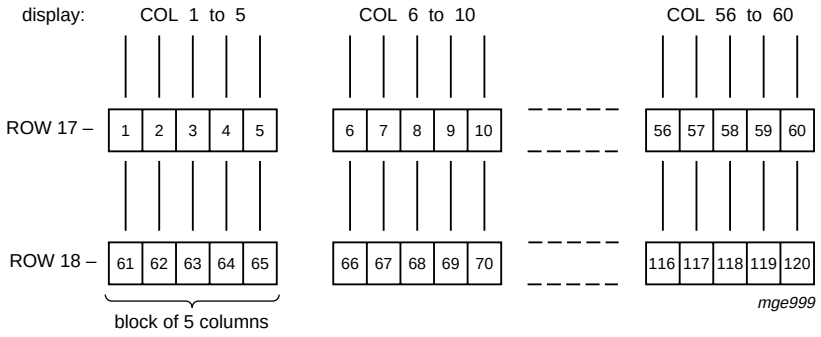


Fig 18. CGRAM to icon mapping (a)

icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

mgg001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.

Data in character codes 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.

Data in character codes 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig 19. CGRAM to icon mapping (b)

10.3 Bit IM

When IM = 0, the chip is in Character mode. In Character mode, characters and icons are driven (MUX 1:18 or MUX 1:9). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register VA.

When IM = 1, the chip is in Icon mode. In Icon mode only the icons are driven (MUX 1:2) and the V_{LCD} generator, if used, produces the V_{LCD} voltage as programmed in register VB.

Table 12. Character/Icon mode operation

IM	Mode	V_{LCD}
0	Character mode	defined in VA
1	Icon mode	defined in VB

10.4 Bit IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, the icon blink is disabled. Icon data is stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

When IB = 1, the icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define icon state when icon blink is not used (see Table 13).

Icon states for the odd phase are stored in CGRAM characters 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 13. Blink effect for icons and cursor character blink

Parameter	Even phase	Odd phase
Cursor character blink	block (all on)	normal (display character)
Icons	state 1; CGRAM character 0 to 2	state 2; CGRAM character 4 to 6

10.5 Direct mode

When DM = 0, the chip is not in the Direct mode. Either the internal V_{LCD} generator or an external voltage may be used to achieve V_{LCD}.

When DM = 1, the chip is in Direct mode. The internal V_{LCD} generator is turned off and the output V_{LCDOUT} is directly connected V_{DD2} (i.e. the V_{LCD} generator supply voltage).

The Direct mode can be used to reduce the current consumption when the required output voltage V_{LCDOUT} is close to the V_{DD2} supply voltage. This can be the case in Icon mode or in MUX 1:9 (depending on LCD liquid properties).

10.6 Voltage multiplier control

10.6.1 Bits S1 and S0

A software configurable voltage multiplier is incorporated in the V_{LCD} generator and can be set via the ‘Set HVgen stages’ command.

The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages, depending on the required output voltage V_{LCD} (see Table 14).

Table 14. S1 and S0 control of voltage multiplier

S1	S0	Description
0	0	set V_{LCD} generator stages to 1 ($2 \times$ voltage multiplier)
0	1	set V_{LCD} generator stages to 2 ($3 \times$ voltage multiplier)
1	0	set V_{LCD} generator stages to 3 ($4 \times$ voltage multiplier)
1	1	do not use

10.7 Screen configuration

10.7.1 Bit L

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120; default.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

10.8 Display configuration

10.8.1 Bit P

The P bit is used to flip the display left to right by mirroring the column data, as shown in Figure 20. This allows the display to be viewed from behind instead of front, enhances the flexibility in the assembly of equipment and avoids complicated data manipulation within the controller.

P = 0: default.

P = 1: mirrors the column data.

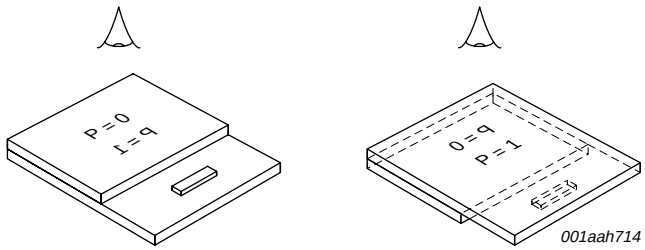


Fig 20. Use of P bit

10.8.2 Bit Q

The Q bit flips the display top to bottom by mirroring the row data.

Q = 0: default.

Q = 1: mirrors the row data.

A combination of Q and P allows the display to be rotated 180 deg, as shown in Figure 21. This is useful for viewing the display from the opposite edge.

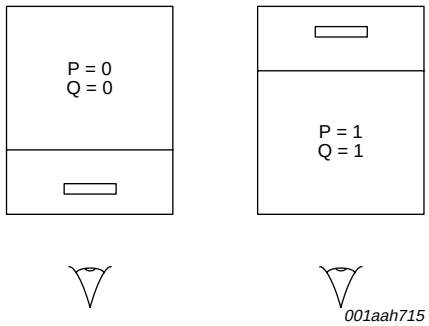


Fig 21. Use of P and Q bits

10.9 Temperature control

Default is bit TC1 = 0 and bit TC2 = 0. Selects the default temperature coefficient for the internally generated V_{LCD} (see Table 15).

Table 15. TC1 and TC2 selection of V_{LCD} temperature coefficient

Bit TC1	Bit TC2	V_{LCD} temperature coefficient TC (typical values)
0	0	TC = –0.16 %/K
1	0	TC = –0.18 %/K
0	1	TC = –0.21 %/K
1	1	TC = –0.24 %/K

10.10 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers, VA and VB hold V_{LCD} values for the Character mode and the Icon mode respectively. The generated V_{LCD} is independent of V_{DD}, allowing battery operation of the chip.

10.10.1 V_{LCD} programming

1. Send ‘function set’ instruction with H = 1
2. Send ‘set V_{LCD}’ instruction to write to voltage register:
   a. If DB[7:6] = 10, then DB[5:0] represents V_{LCD} of Character mode (VA)
   b. If DB[7:6] = 11, then DB[5:0] represents V_{LCD} of Icon mode (VB)
   c. DB[5:0] = 00 0000 switches V_{LCD} generator off (when selected)
   d. During ‘display off’ and power-down the V_{LCD} generator is also disabled
3. Send ‘function set’ instruction with H = 0 to resume normal programming

Section 8.1 shows the relation between V_{LCD} and registers VA and VB.

10.11 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 16.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 16. Reducing current consumption

Original mode	Alternative mode
Character mode	Icon mode (control bit M)
Display on	display off (control bit D)
V_{LCD} generator operating	Direct mode
Any mode	Power-down mode (PD pin)

11. Interfaces to microcontroller

11.1 Parallel interface

The PCF2113x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required (see Section 7).

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for the transaction. The higher order bits (corresponding to bits DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (corresponding to bits DB3 to DB0 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction: see Figure 22, Figure 23 and Figure 24 for examples of bus protocol.

In 4-bit mode, pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

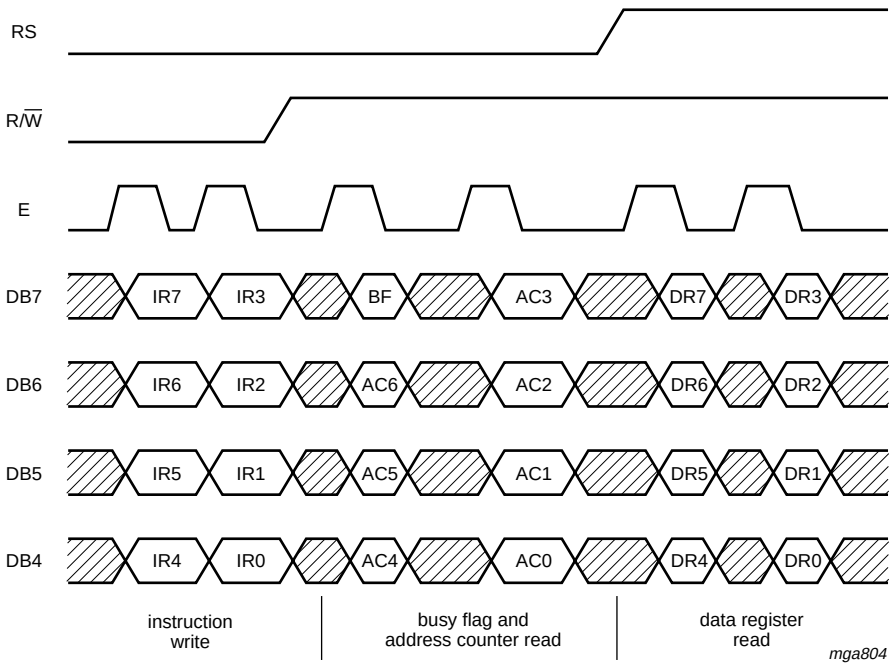
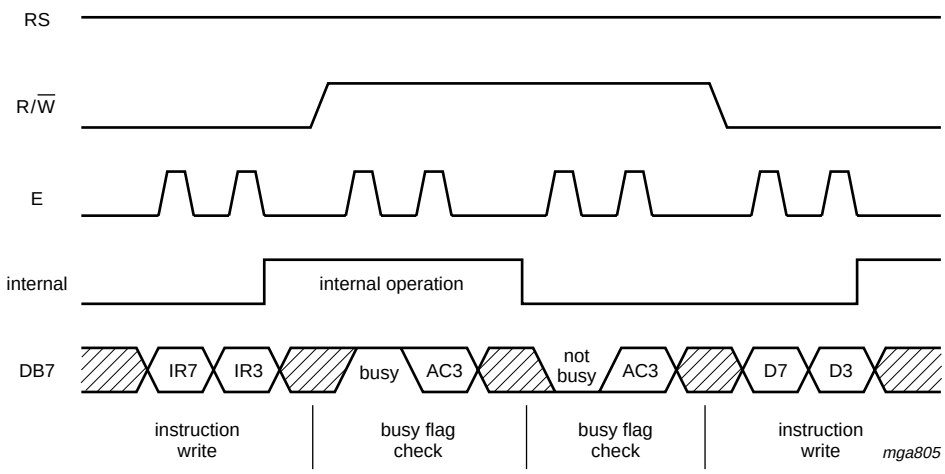


Fig 22. 4-bit transfer example



IR7, IR3: instruction 7th, 3rd bit.

AC3: address counter 3rd bit.

D7, D3: data 7th, 3rd bit.

Fig 23. Example of 4-bit data transfer timing sequence

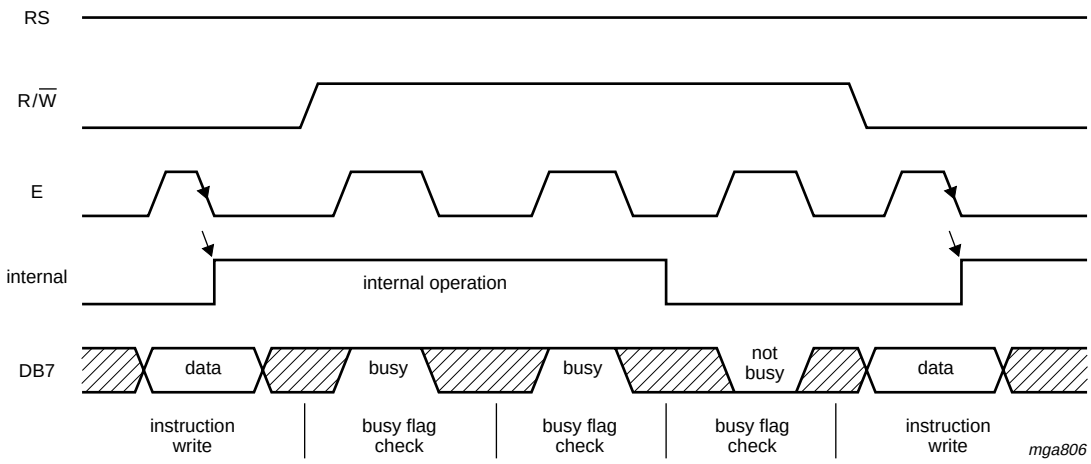


Fig 24. Example of busy flag checking timing sequence

11.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

11.2.1 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2113x read and write cycles is shown in Figure 25, Figure 26 and Figure 27. The slow-down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2113x.

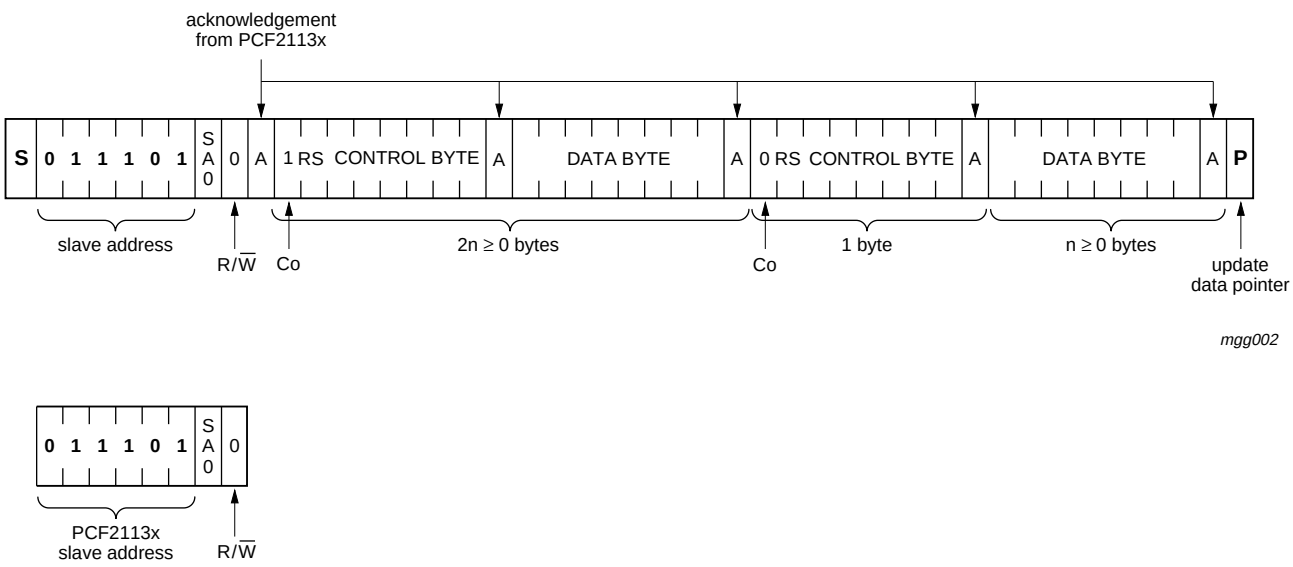
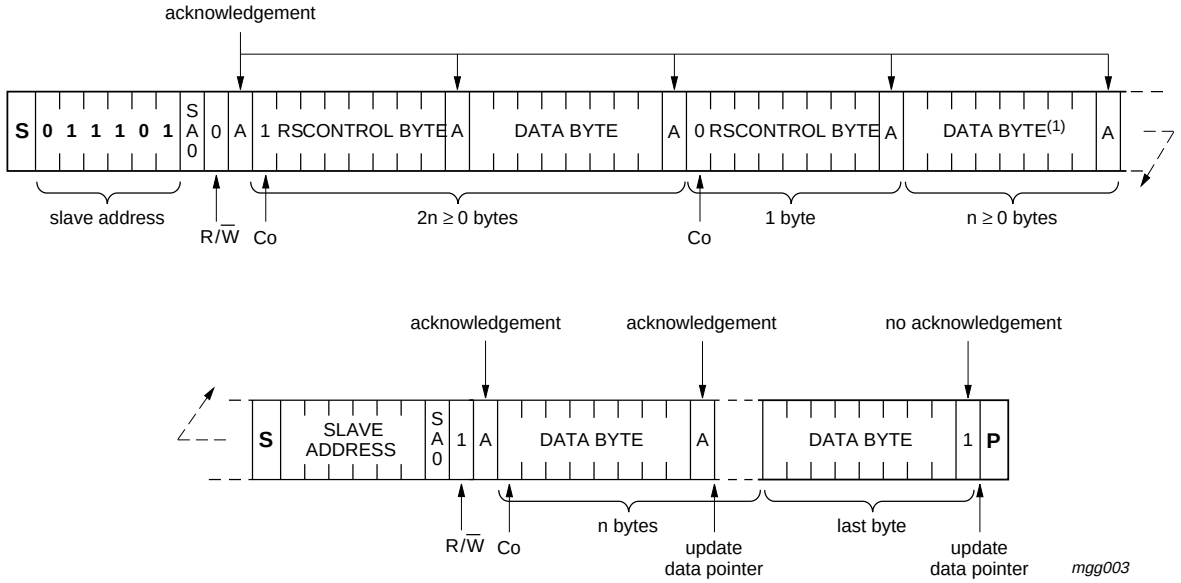


Fig 25. Master transmits to slave receiver; write mode



(1) Last data byte is a dummy byte (may be omitted).

Fig 26. Master reads after setting word address; write word address; set RS; 'read data'

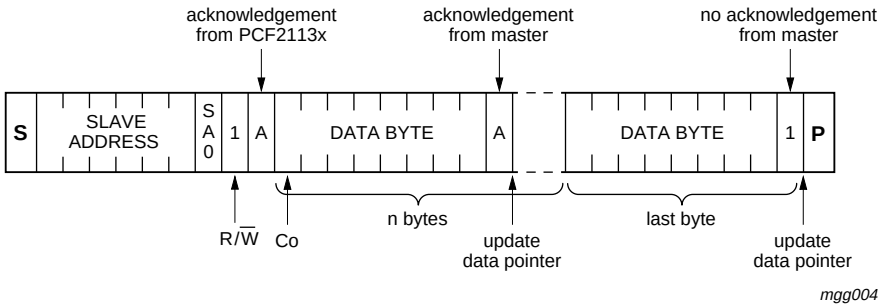


Fig 27. Master reads slave immediately after first byte; read mode (RS previously defined)

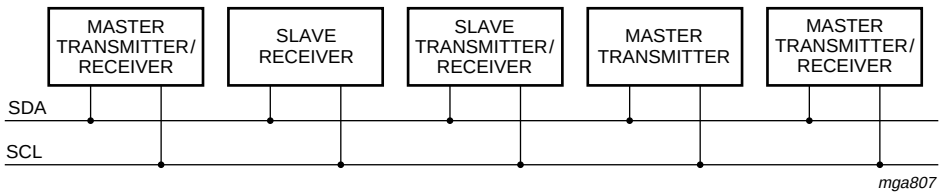


Fig 28. System configuration

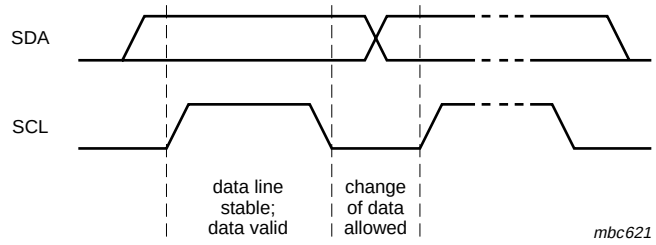


Fig 29. Bit transfer

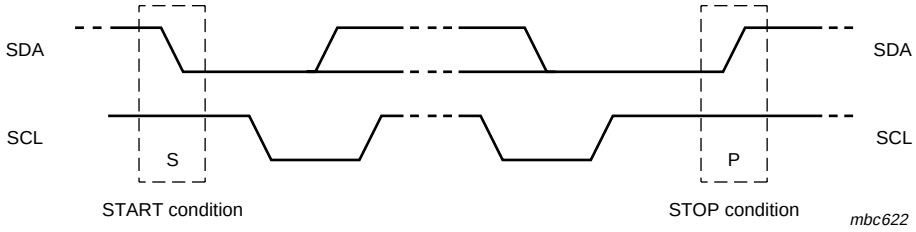


Fig 30. Definition of START and STOP conditions

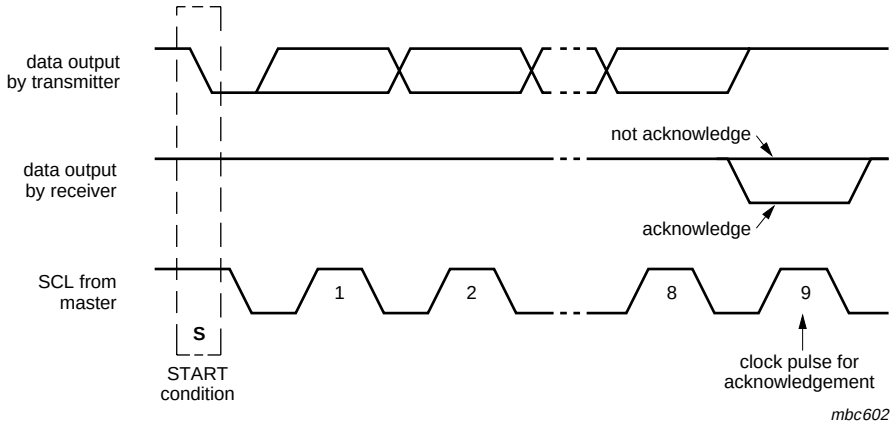


Fig 31. Acknowledgement on the I²C-bus

11.2.2 Definitions

- Transmitter: the device that sends the data to the bus
- Receiver: the device that receives the data from the bus
- Master: the device that initiates and terminates a transfer and generates clock signals
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices

12. Internal circuitry

Table 17. Device protection circuits

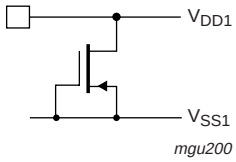
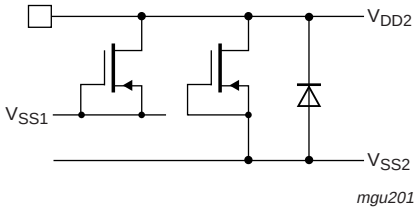
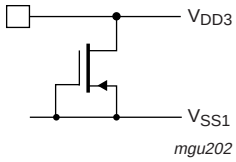
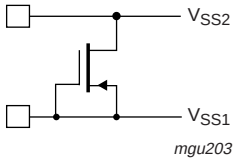
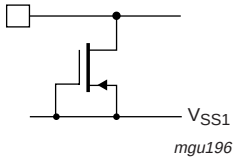
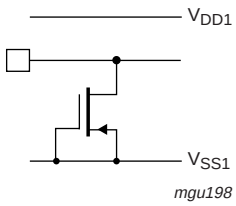
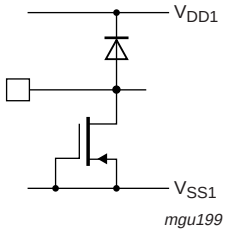
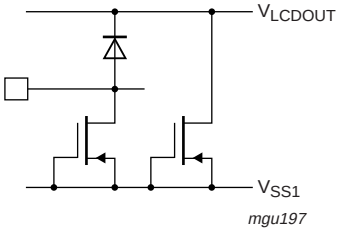
Symbol	Pad	Internal circuit
V_{DD1}	1	
V_{DD2}	109	
V_{DD3}	110	
V_{SS1}	7	
V_{SS2}	8	
$V_{LCDSENSE}$	10	
V_{LCDIN}	11	
V_{LCDOUT}	9	
SCL	96	
SDA	97	

Table 17. Device protection circuits *...continued*

Symbol	Pad	Internal circuit
OSC	2	
PD	3	
T1	5	
T2	6	
T3	4	
E	98	
RS	99	
R/$\overline{W}$	100	
DB0 to DB7	108 to 101	
R1 to R8	94 to 87	
R9 to R16	12 to 19	
R17	95	
R18	20	
C1 to C2	86 to 85	
C3 to C27	82 to 58	
C28 to C52	55 to 31	
C53 to C60	28 to 21	

13. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD1}	supply voltage 1	logic supply		–0.5	+5.5	V
V_{DD2}	supply voltage 2	V_{LCD} generator supply		–0.5	+4.0	V
V_{DD3}	supply voltage 3	analog supply		–0.5	+4.0	V
V_{LCD}	LCD supply voltage			–0.5	+6.5	V
$V_{i(n)}$	voltage on any input	V_{DD} related inputs		–0.5	+5.5	V
$V_{o(n)}$	voltage on any output	V_{LCD} related outputs		–0.5	+6.5	V
I_I	input current	DC level		–10	+10	mA
I_O	output current	DC level		–10	+10	mA
I_{DD}	supply current	on pins V_{DD1}, V_{DD2}, V_{DD3}		-	+50	mA
I_{SS}	ground supply current	on pins V_{SS1} and V_{SS2}		-	–50	mA
$I_{DD(LCD)}$	LCD supply current			-	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		MM	[2]	-	±200	V
		CDM	[3]	-	±2000	V
I_{lu}	latch-up current		[4]	-	100	mA
T_{stg}	storage temperature			–65	+150	°C

[1] HBM: Human Body Model, according to JESD22-A114.

[2] MM: Machine Model, according to JESD22-A115.

[3] CDM: Charged-Device Model, according to JESD22-C101.

[4] Latch-up testing, according to JESD78.

14. Static characteristics

Table 19. Static characteristics

V_{DD1} = 1.8 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD1}	supply voltage 1	logic supply	[1]	1.8	-	5.5	V
V_{DD2}	supply voltage 2	V_{LCD} generator supply; internal V_{LCD} generation (V_{DD2} and V_{DD3} < V_{LCD})		2.2	-	4.0	V
V_{DD3}	supply voltage 3	analog supply; internal V_{LCD} generation (V_{DD2} and V_{DD3} < V_{LCD})		2.2	-	4.0	V
V_{LCD}	LCD supply voltage			2.2	-	6.5	V
V_{POR}	power-on reset voltage		[1][2]	0.9	-	1.6	V
I_{SS}	ground supply current	external V_{LCD}; pins V_{SS1} and V_{SS2}	[3]				
		Character mode; V_{LCD} = 6.5 V; V_{DD1} = 5.5 V; V_{DD2} = V_{DD3} = 4 V		-	70	120	µA
		Character mode; V_{LCD} = 5 V; V_{DD1} = V_{DD2} = V_{DD3} = 3 V	[4]	-	45	80	µA
		Icon mode; V_{LCD} = 2.5 V; V_{DD1} = V_{DD2} = V_{DD3} = 3 V	[4]	-	25	45	µA
		internal V_{LCD}; pins V_{SS1} and V_{SS2}	[3][5]				
		Character mode; V_{LCD} = 6.5 V; V_{DD1} = 5.5 V; V_{DD2} = V_{DD3} = 2.2 V		-	190	400	µA
		Character mode; V_{LCD} = 5 V; V_{DD1} = V_{DD2} = V_{DD3} = 3 V	[4]	-	160	400	µA
		Icon mode; V_{LCD} = 2.5 V; V_{DD1} = V_{DD2} = V_{DD3} = 2.5 V	[4]	-	120	-	µA
		Power-down mode; V_{LCD} = 2.5 V; V_{DD1} = V_{DD2} = V_{DD3} = 3 V; pins RS, PD, R/$\overline{W}$ and DB7 to DB0 = HIGH; in OSC = LOW	[3][4]	-	2	5	µA
Logic							
V_i	input voltage			V_{SS1} − 0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage	on pin OSC		V_{SS1}	-	V_{DD1} − 1.2	V
		on any other pin		V_{SS1}	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage	on pin OSC		V_{DD1} − 0.1	-	V_{DD1}	V
		on any other pin		$0.7V_{DD1}$	-	V_{DD1}	V
I_L	leakage current	V_I = V_{DD1} or V_{SS1}		−1	-	+1	µA

Table 19. Static characteristics *...continued*

V_{DD1} = 1.8 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pins DB7 to DB0							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD1} = 5 V		1.6	4	-	mA
I_{OH}	HIGH-level output current	V_{OH} = 0.4 V; V_{DD1} = 5 V		−1	−8	-	mA
I_{pu}	pull-up current	V_I = V_{SS1}		0.04	0.15	1	µA
I^2C-bus							
Input on pins SDA and SCL							
V_I	input voltage			V_{SS1} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD1}$	-	5.5	V
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}		−1	-	+1	µA
C_I	input capacitance		[6]	-	5	-	pF
Output on pin SDA							
$I_{OL(SDA)}$	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD1} > 2 V		3	-	-	mA
		V_{OL} = $0.2V_{DD1}$; V_{DD1} < 2 V		2	-	-	mA
LCD outputs							
R_O	output resistance	row outputs: pins R1 to R18	[7]	-	10	30	kΩ
		column outputs: pins C1 to C60	[7]	-	15	40	kΩ
ΔV_{bias}	bias voltage variation	pins R1 to R18 and C1 to C60	[8]	-	20	130	mV
ΔV_{LCD}	LCD voltage variation	T_{amb} = 25 °C	[5]				
		V_{LCD} < 3 V		-	-	160	mV
		V_{LCD} < 4 V		-	-	200	mV
		V_{LCD} < 5 V		-	-	260	mV
		V_{LCD} < 6 V		-	-	340	mV

[1] Spikes on V_{DD1} or V_{SS1} which cause (V_{DD1} − V_{SS1}) ≤ 1.6 V can cause a Power-on reset.

[2] Resets all logic when V_{DD1} < V_{POR}; 3 oscillator cycles required.

[3] LCD outputs are open-circuit; inputs at V_{DD1} or V_{SS1}; bus inactive.

[4] T_{amb} = 25 °C; f_{osc} = 200 kHz.

[5] LCD outputs are open-circuit; V_{LCD} generator is on; load current $I_{DD(LCD)}$ = 5 µA (at V_{LCD}).

[6] Tested on a sample basis.

[7] Resistance of output pins (R1 to R18 and C1 to C60) with a load current of 10 µA; outputs measured one at a time; external V_{LCD} = 3 V; V_{DD1} = V_{DD2} = V_{DD3} = V_{LCD}.

[8] LCD outputs are open-circuit; external V_{LCD}.

15. Dynamic characteristics

Table 20. Dynamic characteristics

V_{DD1} = 1.8 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{fr(LCD)}$	LCD frame frequency	internal clock; V_{DD} = 5.0 V		45	95	147	Hz
f_{osc}	oscillator frequency		[1]	140	250	450	kHz
$f_{osc(ext)}$	external oscillator frequency			140	-	450	kHz
$t_{d(startup)(OSC)}$	start-up delay time on pin OSC	oscillator, after power down	[2]	-	200	300	µs
$t_{w(pd)}$	power-down pulse width			1	-	-	µs
$t_{w(spike)}$	spike pulse width	on pin PD	[2]	-	-	90	ns
Timing characteristics of parallel interface [3]							
Write operation (writing data from microcontroller to PCF2113x); see Figure 32							
$t_{cy(en)}$	enable cycle time			500	-	-	ns
$t_{w(en)}$	enable pulse width			220	-	-	ns
$t_{su(A)}$	address set-up time			50	-	-	ns
$t_{h(A)}$	address hold time			25	-	-	ns
$t_{su(D)}$	data input set-up time			60	-	-	ns
$t_{h(D)}$	data input hold time			25	-	-	ns
Read operation (reading data from PCF2113x to microcontroller); see Figure 33							
$t_{cy(en)}$	enable cycle time			500	-	-	ns
$t_{w(en)}$	enable pulse width			220	-	-	ns
$t_{su(A)}$	address set-up time			50	-	-	ns
$t_{h(A)}$	address hold time			25	-	-	ns
$t_{d(DV)}$	data input valid delay time	V_{DD1} > 2.2 V		-	-	150	ns
		V_{DD1} > 1.5 V		-	-	250	ns
$t_{h(D)}$	data input hold time			5	-	-	ns
Timing characteristics of I^2C-bus interface [3]; see Figure 34							
f_{SCL}	SCL frequency			-	-	400	Hz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
t_r	rise time of both SDA and SCL signals		[2][4]	15 + 0.1C_b	-	300	ns
t_f	fall time of both SDA and SCL signals		[2][4]	15 + 0.1C_b	-	300	ns
C_b	capacitive load for each bus line		[4]	-	-	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs

Table 20. Dynamic characteristics *...continued*

V_{DD1} = 1.8 V to 5.5 V; V_{DD2} = V_{DD3} = 2.2 V to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	on bus	-	-	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs

[1] Not available at any pin.

[2] Tested on a sample basis.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] C_b = total capacitance of one bus line in pF.

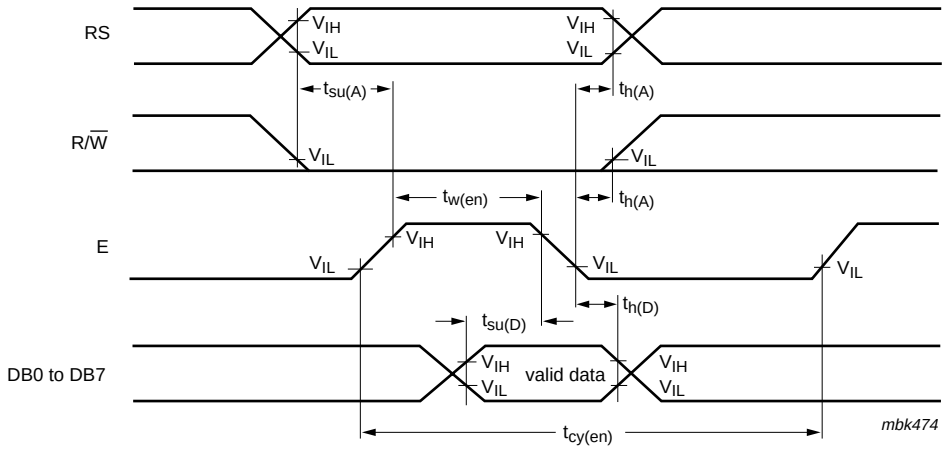


Fig 32. Parallel bus write operation sequence; writing data from microcontroller to PCF2113x

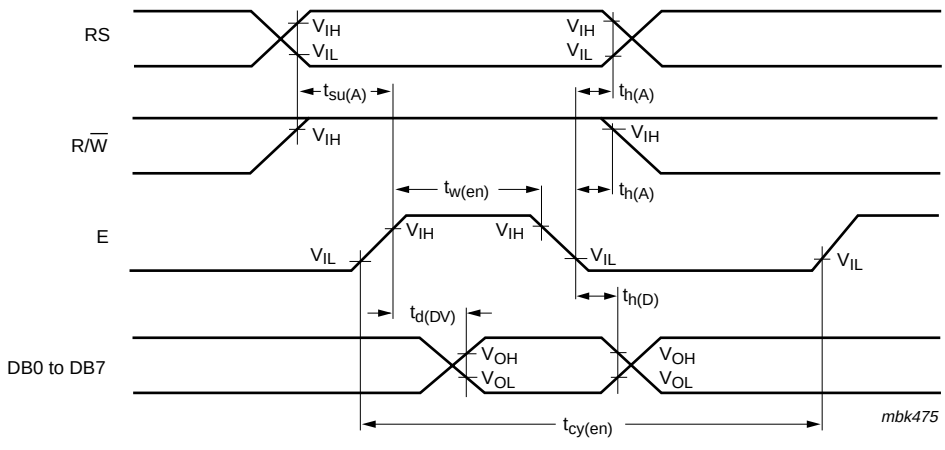


Fig 33. Parallel bus read operation sequence; writing data from PCF2113x to microcontroller

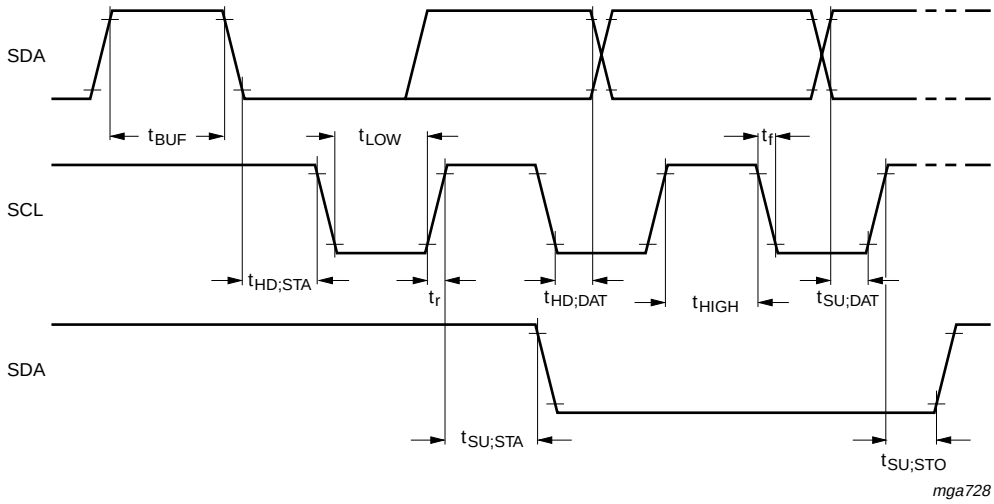


Fig 34. I²C-bus timing diagram

16. Application information

16.1 Application diagrams

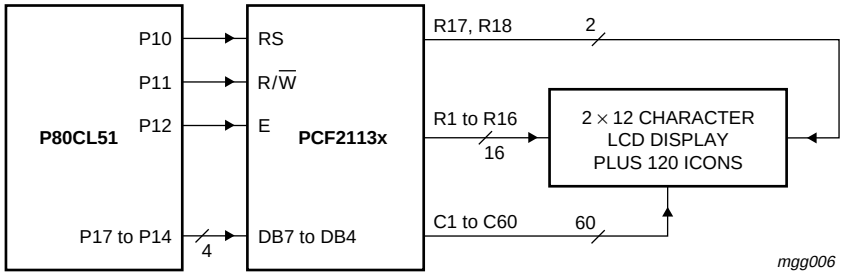


Fig 35. Direct connection to 8-bit microcontroller; 4-bit bus

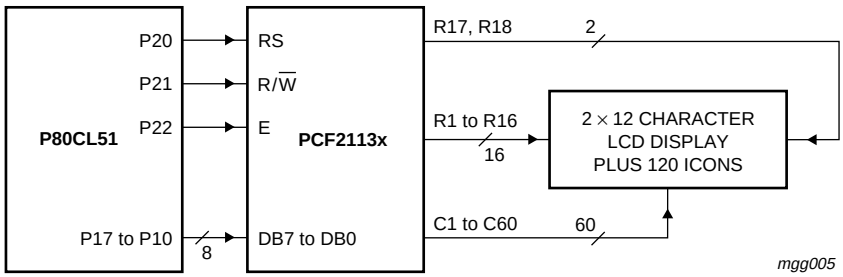


Fig 36. Direct connection to 8-bit microcontroller; 8-bit bus

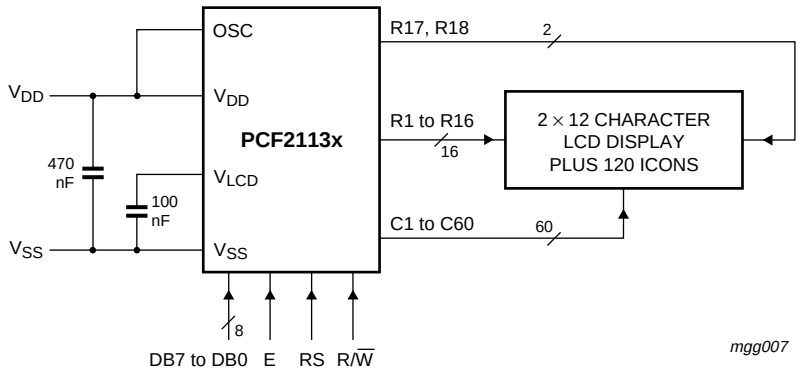


Fig 37. Typical application using parallel interface

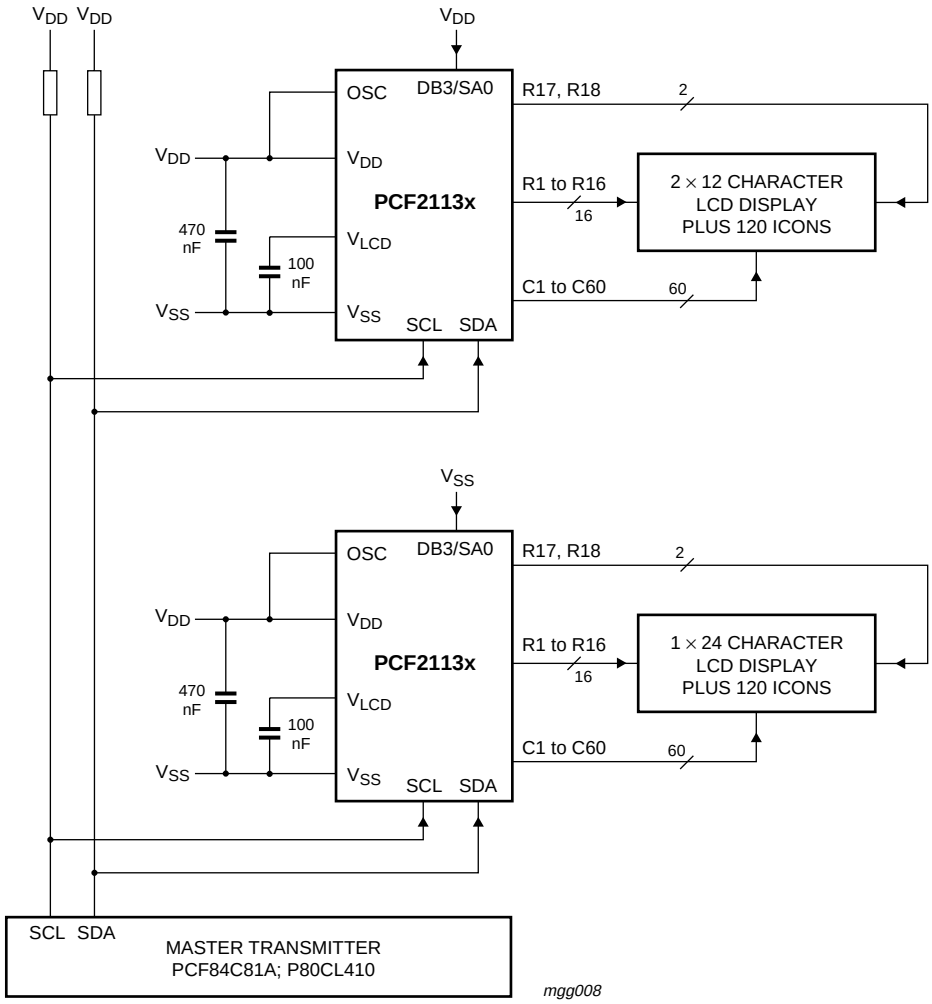


Fig 38. Application using I²C-bus interface

16.2 General application information

The required minimum value for the external capacitors in an application with the PCF2113x are: $C_{ext} \geq 100$ nF between V_{LCD} and V_{SS}, and $C_{ext} \geq 470$ nF between V_{DD} and V_{SS}. Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended Indium Tin Oxide (ITO) track resistance is to be minimized for the I/O and supply connections. Optimized values for these tracks are below 50 Ω for the supply and below 100 Ω for the I/O connections. Higher track resistances reduce performance and increase current consumption.

To avoid accidental triggering of power-on reset (especially in COG applications), the supplies must be adequately decoupled. Depending on power supply quality, V_{DD1} may have to be risen above the specified minimum.

16.3 4-bit operation, 1-line display using internal reset

The program must set functions prior to a 4-bit operation (see Table 21). When power is turned on, 8-bit operation is automatically selected and the PCF2113x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 21 step 3). Thus, DB4 to DB7 of the ‘function set’ are written twice.

Table 21. 4-bit operation, 1-line display example using internal reset

Step	Instruction						Display	Operation
1	internal power supply on (PCF2113x is initialized by the internal reset)							initialized; no display appears
2	function set							sets a 4-bit operation; in this instance operation is handled as 8-bit by initialization and only this instruction completes with one write
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		
	0	0	0	0	1	0		
3	function set							sets to 4-bit operation, selects 1-line display and V_{LCD} = VA; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	1	0		
	0	0	0	0	0	0		
4	display control							turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	_	
	0	0	1	1	1	0		
5	entry mode set							sets mode to increment address by 1 and to shift the cursor to the right at the time of write to the DDRAM/CGRAM; display is not shifted
	0	0	0	0	0	0	_	
	0	0	0	1	1	0		
6	‘write data’ to CGRAM/DDRAM							writes ’P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	P_	
	1	0	0	0	0	0		

16.4 8-bit operation, 1-line display using internal reset

Table 22 and Table 23 show an example of a 1-line display in 8-bit operation. The PCF2113x functions must be set by the ‘function set’ instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays

when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

Table 22. 8-bit operation, 1-line display example; using internal reset (character set 'A')

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	power supply on (PCF2113x is initialized by the internal reset)											initialized; no display appears
2	function set											sets to 8-bit operation, selects 1-line display and V_{LCD} = VA
	0	0	0	0	1	1	0	0	0	0		
3	display control											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	
4	entry mode set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DDRAM/CGRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	'write data' to CGRAM/DDRAM											writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	P_	
6	'write data' to CGRAM/DDRAM											writes 'H'
	1	0	0	1	0	0	1	0	0	0	PH_	
7 to 10	:											writes 'ILIP'
	:											
11	'write data' to CGRAM/DDRAM											writes 'S'
	1	0	0	1	0	1	0	0	1	1	PHILIPS_	
12	entry mode set											sets mode for display shift at time of write
	0	0	0	0	0	0	0	1	1	1	PHILIPS_	
13	'write data' to CGRAM/DDRAM											writes space
	1	0	0	0	1	0	0	0	0	0	HILIPS _	
14	'write data' to CGRAM/DDRAM											writes 'M'
	1	0	0	1	0	0	1	1	0	1	HILIPS M_	
15 to 19	:											writes 'ICROK'
	:											
20	'write data' to CGRAM/DDRAM											writes 'O'
	1	0	0	1	0	0	1	1	1	1	MICROKO_	
21	cursor/display shift											shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0	MICROKO	
22	cursor/display shift											shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0	MICROKO	
23	'write data' to CGRAM/DDRAM											writes 'C' correction; the display moves to the left
	1	0	0	1	0	0	0	0	1	1	ICROCO	
24	cursor/display shift											shifts the display and cursor to the right
	0	0	0	0	0	1	1	1	0	0	MICROCO	

Table 22. 8-bit operation, 1-line display example; using internal reset (character set 'A') *...continued*

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
25	cursor/display shift											shifts only the cursor to the right
	0	0	0	0	0	1	0	1	0	0	MICROCO_	
26	'write data' to CGRAM/DDRAM											writes 'M'
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	
27	return home											returns both display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	PHILIPS M	

Table 23. 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	power supply on (PCF2113x is initialized by the internal reset)											initialized; no display appears
2	function set											sets to 8-bit operation, selects 1-line display and V_{LCD} = VA
	0	0	0	0	1	1	0	0	0	0		
3	display control											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	
4	entry mode set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DDRAM/CGRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	set CGRAM address											sets the CGRAM address to position of character '0'; the CGRAM is selected
	0	0	0	1	0	0	0	0	0	0	_	
6	'write data' to CGRAM/DDRAM											writes data to CGRAM for icon even phase; icon appears
	1	0	0	0	0	0	1	0	1	0	_	
7						:						
						:						
8	sets CGRAM address											sets the CGRAM address to position of character '0'; the CGRAM is selected
	0	0	0	1	1	1	0	0	0	0	_	
9	'write data' to CGRAM/DDRAM											writes data to CGRAM for icon odd phase
	1	0	0	0	0	0	1	0	1	0	_	
10						:						
						:						
11	function set											sets H = 1: Extended instruction set
	0	0	0	0	1	1	0	0	0	1	_	
12	icon control											icons blink
	0	0	0	0	0	0	1	0	1	0	_	
13	function set											sets H = 0
	0	0	0	0	1	1	0	0	0	0	_	
14	set DDRAM address											sets the DDRAM to the first position; DDRAM is selected
	0	0	1	0	0	0	0	0	0	0	_	

Table 23. 8-bit operation, 1-line display and icon example; using internal reset (character set 'A') *...continued*

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
15	'write data' to CGRAM/DDRAM											writes 'P'; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	P_	
16	'write data' to CGRAM/DDRAM											writes 'H'
	1	0	0	1	0	0	1	0	0	0	PH_	
17						:						writes 'ILIPS'
						:						
22	return home											returns both display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	PHILIPS	

16.5 8-bit operation, 2-line display

For a 2-line display the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 24). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

Table 24. 8-bit operation, 2-line display example; using internal reset

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	power supply on (PCF2113x is initialized by the internal reset)											initialized; no display appears
2	function set											sets to 8-bit operation, selects 1-line display and V_{LCD} = VA
	0	0	0	0	1	1	0	1	0	0		
3	display control											turns on display and cursor; entire display is blank after initialization
	0	0	0	0	0	0	1	1	1	0	_	
4	entry mode set											sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DDRAM/CGRAM; display is not shifted
	0	0	0	0	0	0	0	1	1	0	_	
5	'write data' to CGRAM/DDRAM											writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	1	0	1	0	0	0	0	P_	
6 to 10						:						writes 'HILIP'
						:						
11	'write data' to CGRAM/DDRAM											writes 'S'
	1	0	0	1	0	1	0	0	1	1	PHILIPS_	
12	sets DDRAM address											sets DDRAM to position the cursor at the start of the 2nd line
	0	0	1	1	0	0	0	0	0	0	PHILIPS	
											_	

Table 24. 8-bit operation, 2-line display example; using internal reset *…continued*

Step	Instruction										Display	Operation
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
13	‘write data’ to CGRAM/DDRAM											writes ‘M’
	1	0	0	1	0	0	1	1	0	1	PHILIPS M_	
14 to 18						:						writes ‘ICROC’
						:						
19	‘write data’ to CGRAM/DDRAM											writes ‘O’
	1	0	0	1	0	0	1	1	1	1	PHILIPS MICROCO_	
20	entry mode set											sets mode for display shift at the time of write
	0	0	0	0	0	0	0	1	1	1	PHILIPS MICROCO_	
21	‘write data’ to CGRAM/DDRAM											writes ‘M’; display is shifted to the left; the 1st and 2nd lines shift together
	1	0	0	1	0	0	1	1	0	1	HILIPS ICROCOM_	
22	return home											returns both the display and cursor to the original position (address 0)
	0	0	0	0	0	0	0	0	1	0	PHILIPS MICROCOM	

16.6 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 25).

Table 25. Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}) [1]

Step	I²C-bus byte									Display	Operation
1	I²C-bus start										initialized; no display appears
2	slave address for write										during the acknowledge cycle SDA is pulled down by the PCF2113x
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	0		
3	send a control byte for ‘function set’										control byte sets RS for the following data bytes
	Co	RS	0	0	0	0	0	0	Ack		
	0	0	0	0	0	0	0	0	1		
4	function set										selects 1-line display and V_{LCD} = VA; SCL pulse during acknowledge cycle starts execution of instruction
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	1	X	0	0	0	0	1		
5	display control										turns on display and cursor; entire display shows character 20h (blank in ASCII-like character sets)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	
	0	0	0	0	1	1	1	0	1		
6	entry mode set										sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	
	0	0	0	0	0	1	1	0	1		

Table 25. Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}) [1] *…continued*

Step	I²C-bus byte									Display	Operation
7	I²C-bus start									_	to write data to DDRAM, RS must be set to 1 so a control byte is needed
8	slave address for write										
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack	_	
	0	1	1	1	0	1	0	0	1		
9	send a control byte for 'write data'										
	Co	RS	0	0	0	0	0	0	Ack	_	
	0	1	0	0	0	0	0	0	1		
10	'write data' to DDRAM										writes 'P'; the DDRAM is selected at power-up; the cursor is incremented by 1 and shifted to the right
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	P_	
	0	1	0	1	0	0	0	0	1		
11	'write data' to DDRAM										writes 'H'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PH_	
	0	1	0	0	1	0	0	0	1		
12 to 15						:					writes 'ILIP'
						:					
16	'write data' to DDRAM										writes 'S'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS_	
	0	1	0	1	0	0	1	1	1		
17	(optional I²C-bus stop) I²C-bus start + slave address for write (as step 8)									PHILIPS_	
18	control byte										
	Co	RS	0	0	0	0	0	0	Ack	PHILIPS_	
	1	0	0	0	0	0	0	0	1		
19	return home										sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS	
	0	0	0	0	0	0	1	0	1		
20	I²C-bus start									PHILIPS	
21	slave address for read										during the acknowledge cycle the content of DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed, so the content of the DR was unknown; the R/$\overline{W}$ has to be set to 1 while still in the I²C-bus write mode
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack	PHILIPS	
	0	1	1	1	0	1	0	1	1		
22	control byte for read										DDRAM content is read from the following instructions
	Co	RS	0	0	0	0	0	0	Ack	PHILIPS	
	0	1	1	0	0	0	0	0	1		

Table 25. Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}) [1] …continued

Step	I²C-bus byte									Display	Operation
23	‘read data’: 8 × SCL + master acknowledge [2]									PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	X	X	X	X	X	X	X	X	0		
24	‘read data’: 8 × SCL + master acknowledge [2]									PHILIPS	8 × SCL; code of letter ‘H’ is read first; during master acknowledge, code of ‘I’ is loaded into the I²C-bus interface
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	0	1	0	0	0	0		
25	‘read data’: 8 × SCL + master acknowledge [2]									PHILIPS	no master acknowledge; -after the content of the I²C-bus interface register is shifted out no internal action is performed; -no new data is loaded into the interface register; -data register is not updated; -address counter is not incremented and cursor is not shifted
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	0	1	0	0	1	1		
26	I²C-bus stop									PHILIPS	

[1] X = not relevant.

[2] SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 26. Initialization by instruction, 8-bit interface [1]

Step	Instruction										Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	internal reset					:					starting from power-on or unknown state
2	wait 2 ms					:					
3	0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bit long). Busy Flag (BF) cannot be checked before this instruction
4	wait 2 ms					:					
5	0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bit long). BF cannot be checked before this instruction
6	wait more than 40 µs					:					
7	0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bit long). BF cannot be checked before this instruction
8						:					BF can be checked after the following instructions; when BF is not checked the waiting time between instructions is the specified instruction time (see Table 10)
9	0	0	0	0	1	1	0	M	0	H	function set (interface is 8 bit long); specify the number of display lines
10	0	0	0	0	0	0	1	0	0	0	display off

Table 26. Initialization by instruction, 8-bit interface [1] *…continued*

Step	Instruction										Description
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
11	0	0	0	0	0	0	0	0	0	1	clear display
12	0	0	0	0	0	0	0	1	I/D	S	entry mode set
						:					
13	initialization ends										

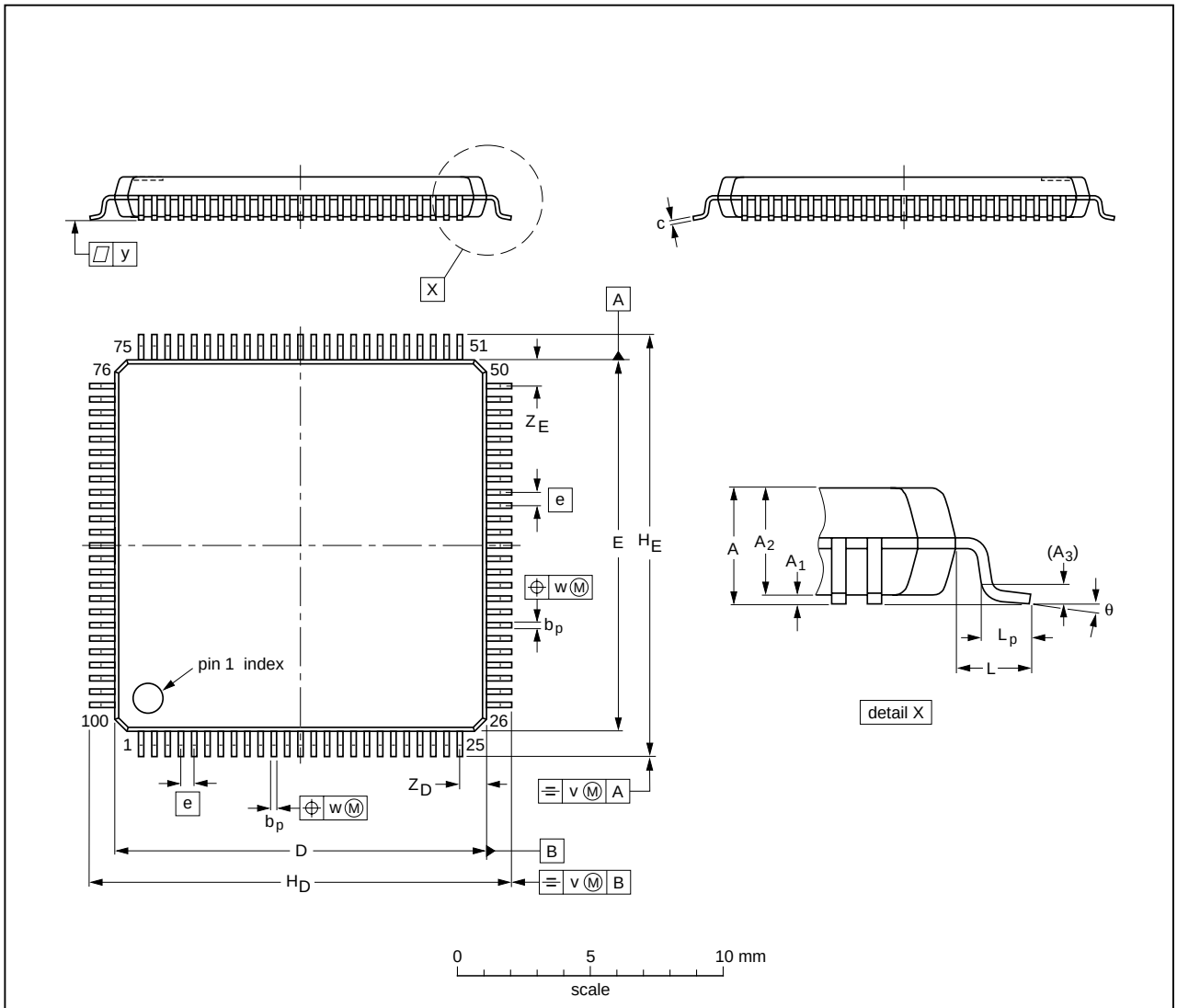
[1] X = not relevant.

Table 27. Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

Step	Instruction						Description
1	internal reset			:			starting from power-on or unknown state
				:			
2	wait 2 ms			:			
				:			
3	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
	0	0	0	0	1	1	function set (interface is 8 bit long)
4	wait 2 ms			:			
				:			
5	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
	0	0	0	0	1	1	function set (interface is 8 bit long)
6	wait more than 40 µs			:			
				:			
7	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
	0	0	0	0	1	1	function set (interface is 8 bit long)
8				:			BF can be checked after the following instructions; when BF is not checked the waiting time between instructions is the specified instruction time (see Table 10)
				:			
9	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bit long)
	0	0	0	0	1	0	interface is 8 bit long
10	0	0	0	0	1	0	function set (interface is 4 bit long)
	0	0	0	M	0	H	specify number of display lines
11	0	0	0	0	0	0	
	0	0	1	0	0	0	display off
12	0	0	0	0	0	0	
	0	0	0	0	0	1	clear display
13	0	0	0	0	0	0	
	0	0	0	1	I/D	S	entry mode set
				:			
14	initialization ends						

17. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 39. Package outline SOT407-1 (LQFP100)

18. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

19. Packing information

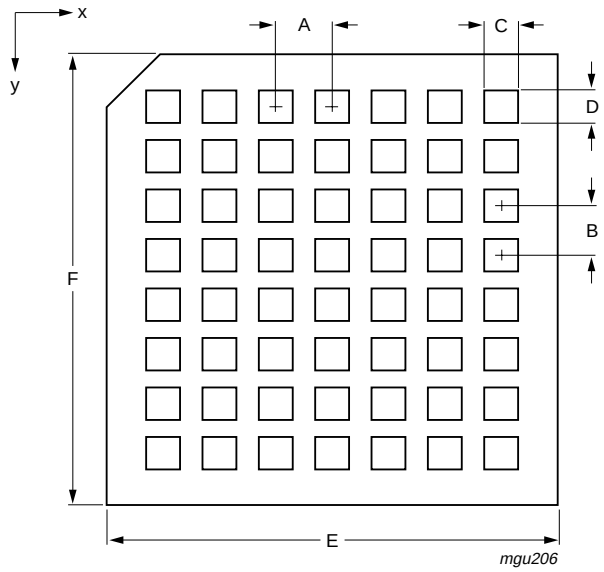


Fig 40. Tray details

Table 28. Tray dimensions (see Figure 40)

Symbol	Description	Value
A	pocket pitch in x direction	6.35 mm
B	pocket pitch in y direction	5.59 mm
C	pocket width in x direction	3.82 mm
D	pocket width in y direction	3.66 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
x	number of pockets, x direction	7
y	number of pockets, y direction	8

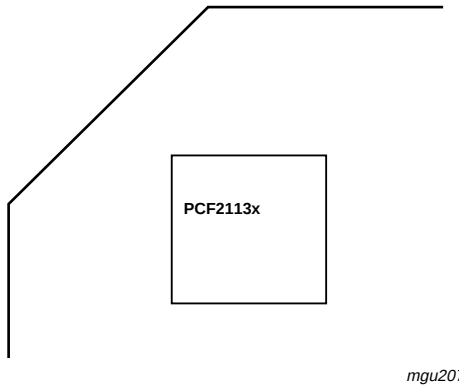


Fig 41. Tray alignment

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram (Figure 3) for the orientation and position of the type name on the die surface.

20. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

20.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

20.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

20.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

20.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 42) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 29 and 30

Table 29. SnPb eutectic process (from J-STD-020C)

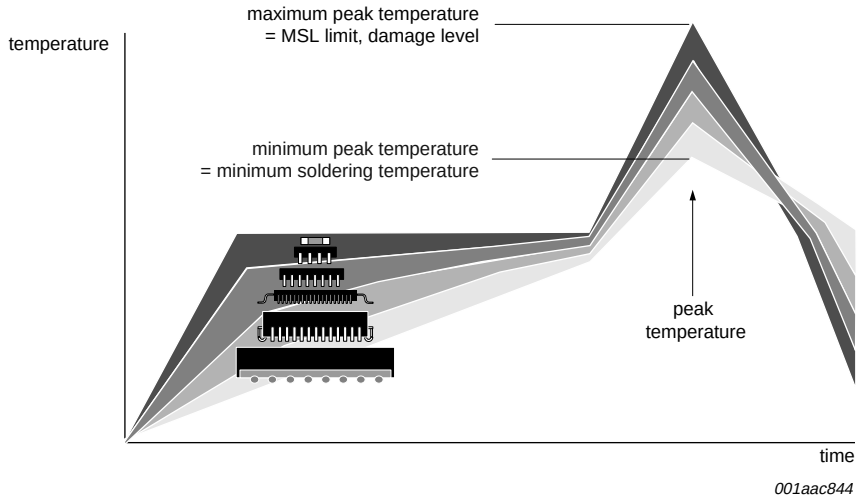
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 30. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 42.



MSL: Moisture Sensitivity Level

Fig 42. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

21. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2113_FAM_4	20080304	Product data sheet	-	PCF2113_FAM_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 3, Figure 13, Figure 20 and Figure 21: new graphics. • Table 2 added: marking codes table. • Table 4: adjusted die size. • Table 18 and Table 19: adjusted values. • Table 25: changed byte settings.			
PCF2113_FAM_3 (9397 750 06995)	20011219	Product specification	-	PCF2113_FAM_2
PCF2113_FAM_2 (9397 750 01753)	19970404	Preliminary data sheet	-	PCF2113_FAM_1
PCF2113_FAM_1	19961021	Preliminary specification	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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