



**THE DATASHEET OF  
PCF2111CT/1,118**



# PCF21xxC family

LCD drivers

Rev. 3 — 6 May 2015

Product data sheet

## 1. General description

The PCF21xxC family are single-chip, silicon gate CMOS LCD driver circuits. A 3-line bus (C-bus) structure enables serial data transfer with microcontrollers.

## 2. Features and benefits

- Supply voltage 2.25 V to 6.0 V
- Low current consumption
- Serial data input
- C-bus control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments: 40 (PCF2100C), 64 (PCF2111C) and 32 (PCF2112C)
- Multiplex rate: 1:2 (PCF2100C and PCF2111C) and 1:1 (PCF2112C)
- Word length: 22 bits (PCF2100C) and 34 bits (PCF2111C and PCF2112C)

## 3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1



### 3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF2100CT/F1	PCF2100CT/F1,112	935195690112	tube	1
	PCF2100CT/F1,118	935195690118	tape and reel, 13 inch	1
PCF2111CT/1	PCF2111CT/1,112	935278772112	tube	1
	PCF2111CT/1,118	935278772118	tape and reel, 13 inch	1
PCF2112CT/1	PCF2112CT/1,112	935279199112	tube	1
	PCF2112CT/1,118	935279199118	tape and reel, 13 inch	1

## 4. Marking

Table 3. Marking codes

Type number	Marking code
PCF2100CT	PCF2100CT
PCF2111CT	PCF2111CT
PCF2112CT	PCF2112CT

## 5. Block diagram

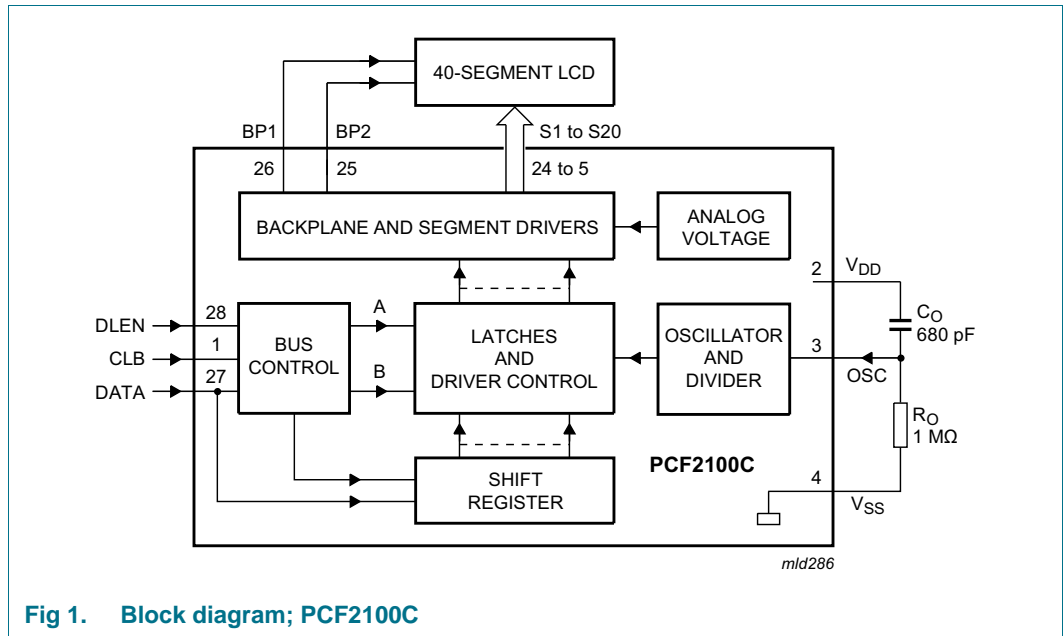


Fig 1. Block diagram; PCF2100C

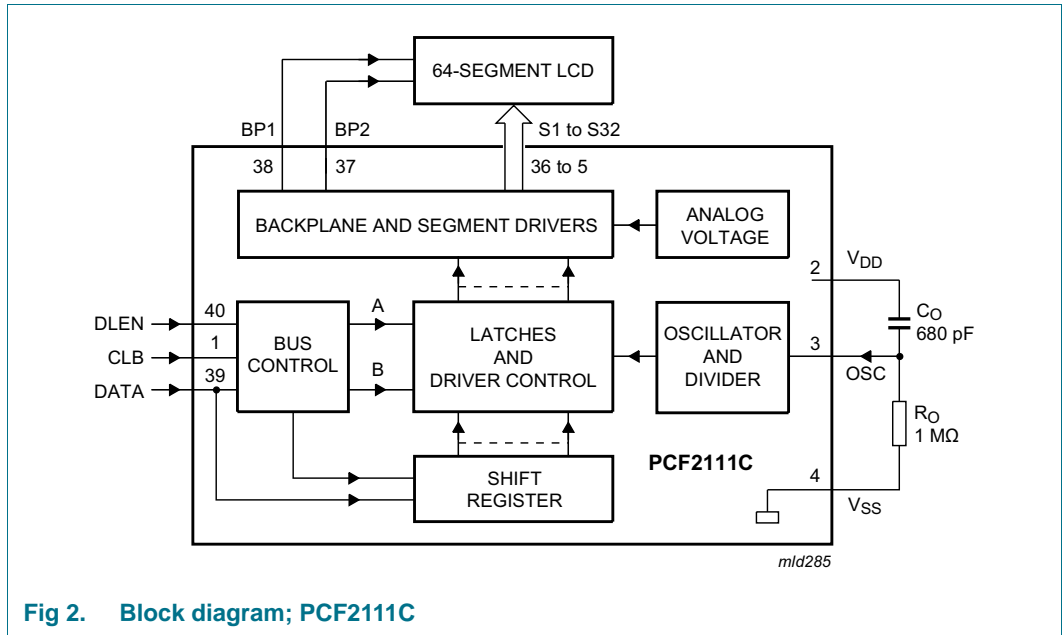


Fig 2. Block diagram; PCF2111C

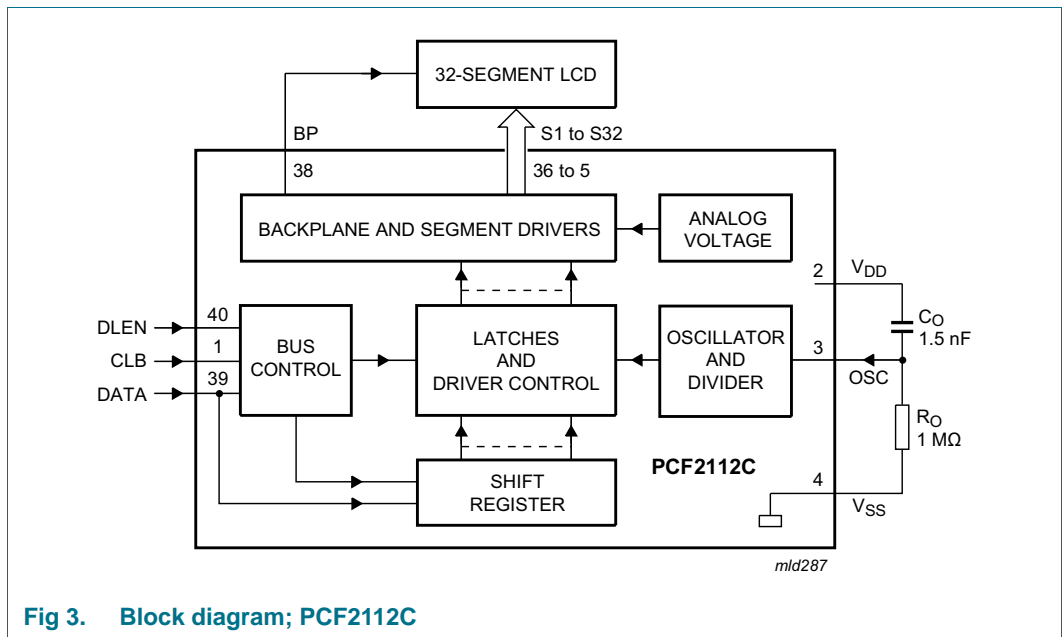
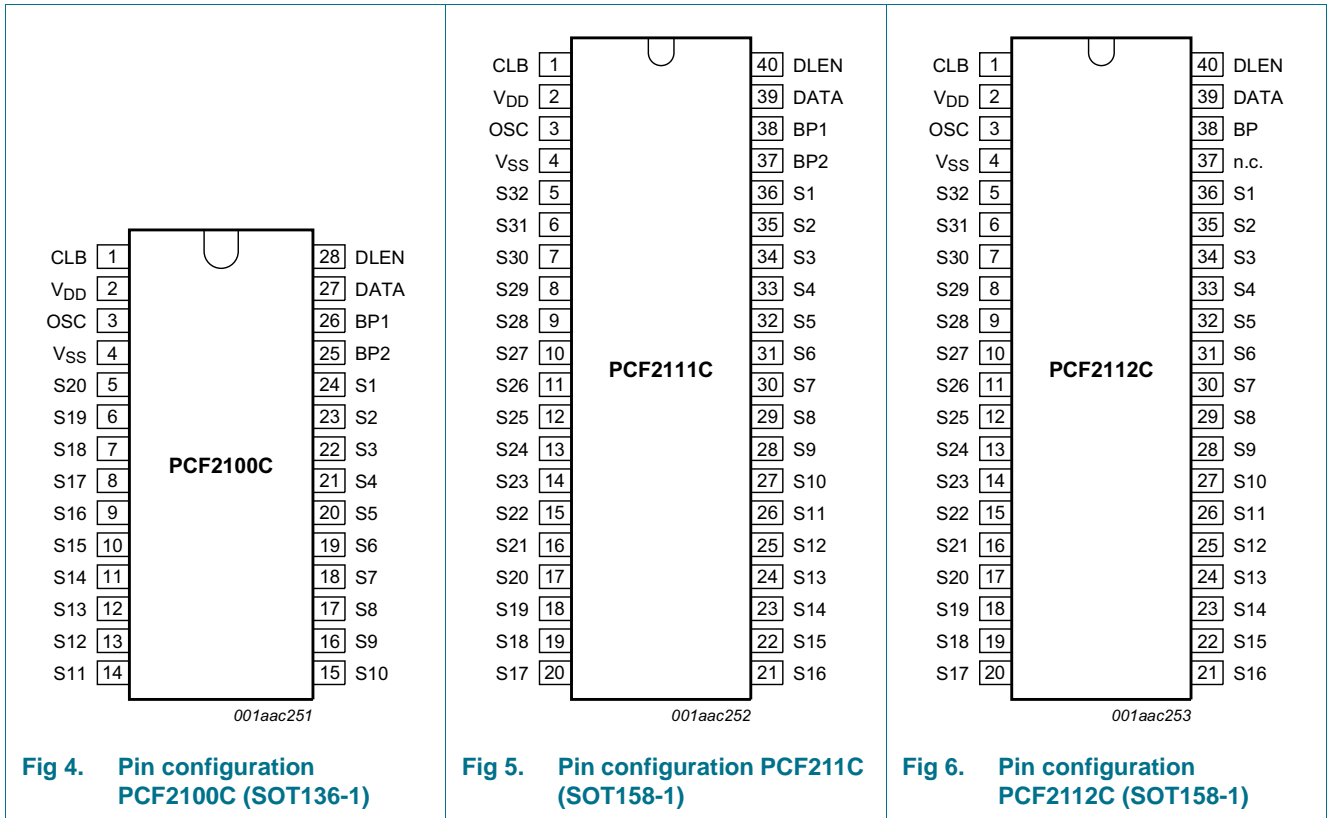


Fig 3. Block diagram; PCF2112C

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 4. Pin description**

Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.

Symbol	Pin			Description
	PCF2100C	PCF2111C	PCF2112C	
CLB	1	1	1	clock burst input (C-bus)
$V_{DD}$	2	2	2	supply voltage
OSC	3	3	3	oscillator input
$V_{SS}$	4	4	4	supply voltage ground
S32	-	5	5	LCD driver output
S31	-	6	6	
S30	-	7	7	
S29	-	8	8	
S28	-	9	9	
S27	-	10	10	
S26	-	11	11	
S25	-	12	12	

**Table 4. Pin description ...continued**  
 Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.

Symbol	Pin			Description
	PCF2100C	PCF2111C	PCF2112C	
S24	-	13	13	LCD driver output
S23	-	14	14	
S22	-	15	15	
S21	-	16	16	
S20	5	17	17	
S19	6	18	18	
S18	7	19	19	
S17	8	20	20	
S16	9	21	21	
S15	10	22	22	
S14	11	23	23	
S13	12	24	24	
S12	13	25	25	
S11	14	26	26	
S10	15	27	27	
S9	16	28	28	
S8	17	29	29	
S7	18	30	30	
S6	19	31	31	
S5	20	32	32	
S4	21	33	33	
S3	22	34	34	
S2	23	35	35	
S1	24	36	36	
BP2	25	37	-	backplane driver output 2
n.c.	-	-	37	not connected
BP1	26	38	-	backplane driver output 1
BP	-	-	38	backplane driver output
DATA	27	39	39	data input line (C-bus)
DLEN	28	40	40	data input line enable (C-bus)

## 7. Functional description

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH; see [Figure 7](#).

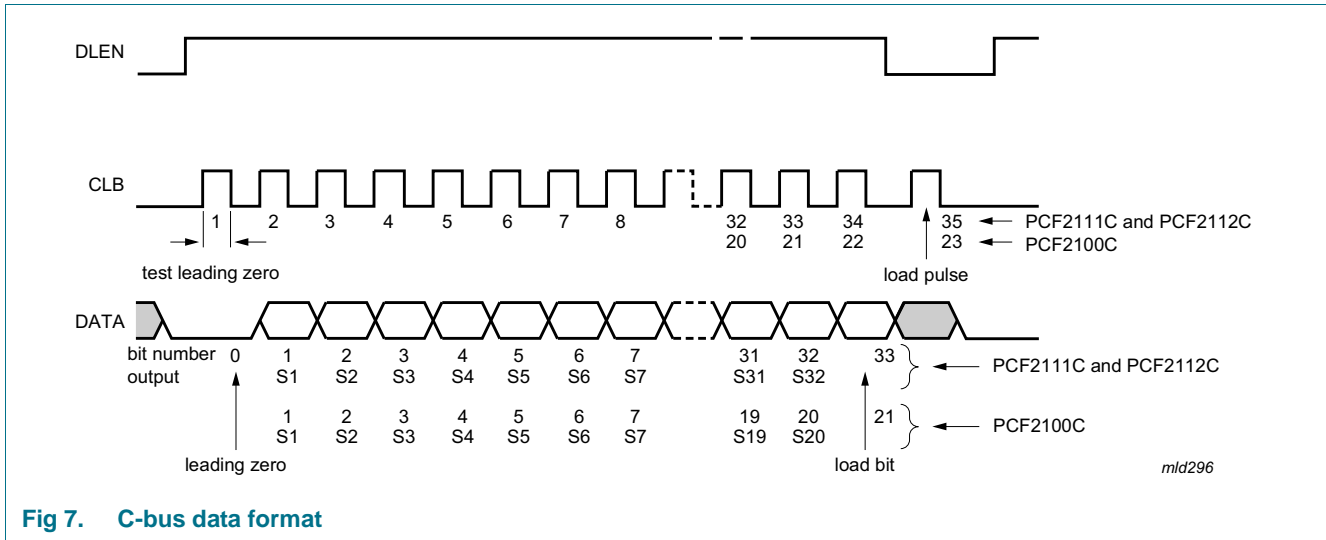


Fig 7. C-bus data format

### 7.1 PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

### 7.2 PCF2111C

When DATA bit 33 is a HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

### 7.3 PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

### 7.4 Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

7.5 Timing

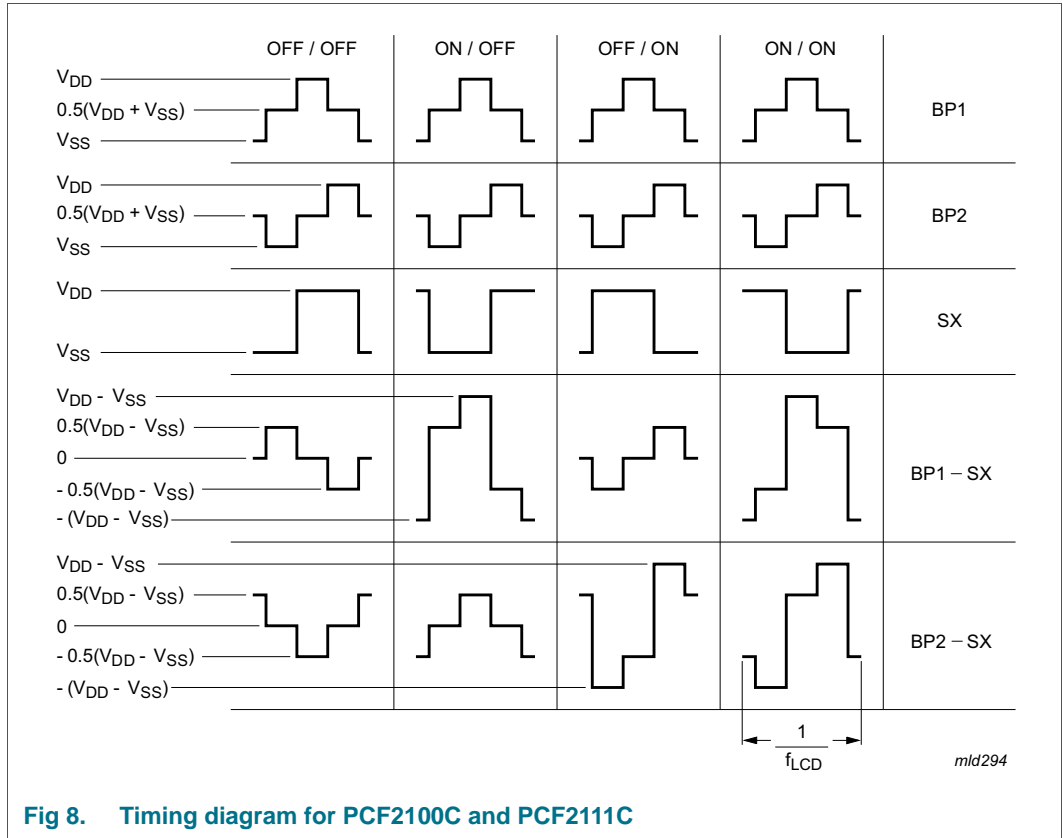


Fig 8. Timing diagram for PCF2100C and PCF2111C

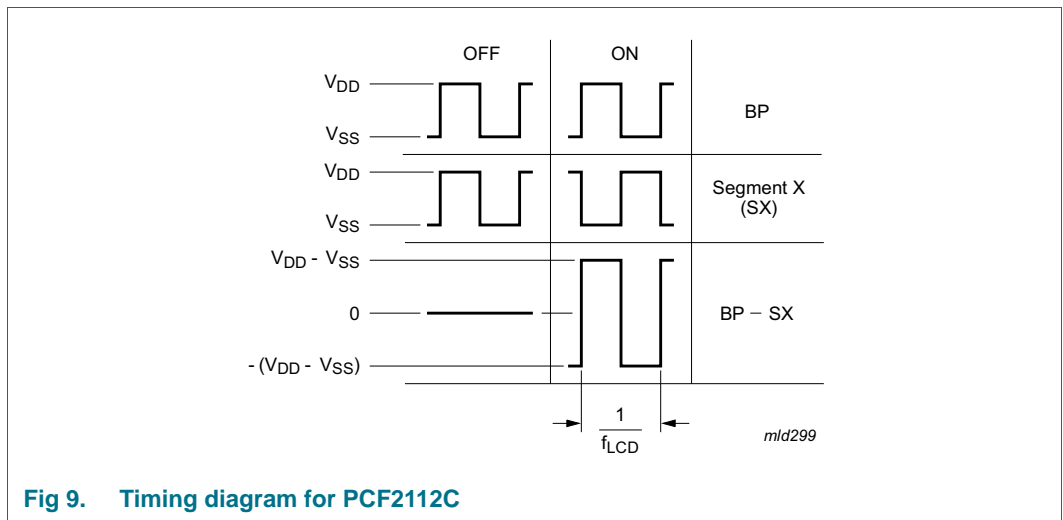
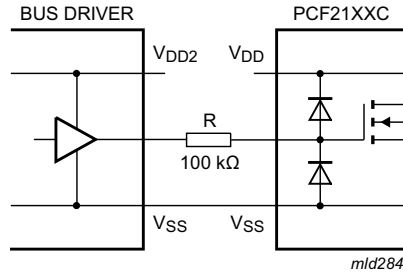


Fig 9. Timing diagram for PCF2112C

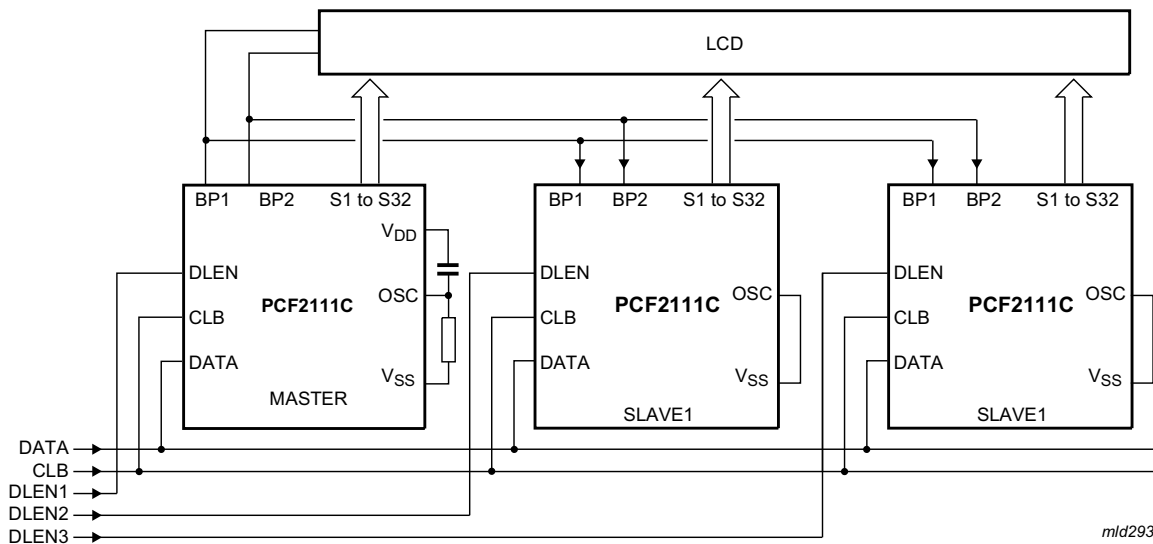
7.6 Input circuitry



$V_{SS}$  line is common. In systems where it is expected that  $V_{DD2} > V_{DD1} + 0.5\text{ V}$ , a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current  $\leq 40\ \mu\text{A}$ .

Fig 10. Input circuitry

7.7 Expansion



By connecting OSC to  $V_{SS}$  the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21xxC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig 11. Expansion possibility (using PCF2111C)

## 8. Safety notes

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

### CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage ( $V_{LCD}$ ) is on while the IC supply voltage ( $V_{DD}$ ) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts,  $V_{LCD}$  and  $V_{DD}$  must be applied or removed together.

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+8.0	V
$V_I$	input voltage	on pins DLEN, CLB, DATA and OSC	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$V_O$	output voltage	on pins BP1, BP2 and S1 to S32	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$I_{DD}$	supply current		-50	+50	mA
$I_{SS}$	ground supply current		-50	+50	mA
$I_I$	input current		-20	+20	mA
$I_O$	output current		-25	+25	mA
$P_{tot}$	total power dissipation		[1] -	500	mW
$P_{out}$	power dissipation per output		-	100	mW
$V_{ESD}$	electrostatic discharge voltage	HBM	[2] -	±2000	V
$I_{lu}$	latch-up current		[3] -	100	mA
$T_{amb}$	ambient temperature	operating device	-40	+85	°C
$T_{stg}$	storage temperature		[4] -65	+150	°C

[1] Derate by 7.7 mW/K when  $T_{amb} > 60$  °C.

[2] Pass level; Human Body Model (HBM), according to [Ref. 7 "JESD22-A114"](#).

[3] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature ( $T_{amb(max)}$ ).

[4] According to the store and transport requirements (see [Ref. 13 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{DD} = 2.25\text{ V to }6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+80\text{ °C}$ ;  $R_O = 1\text{ M}\Omega$ ;  $C_O = 680\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Supply</b>							
$V_{DD}$	supply voltage		2.25	-	6.0	V	
$I_{DD}$	supply current		[1]	-	20	50	$\mu\text{A}$
		$T_{amb} = 25\text{ °C}$	[1]	-	20	30	$\mu\text{A}$
$V_{POR}$	power-on reset voltage		[2]	-	1.0	1.6	V
<b>Inputs CLB, DATA and DLEN</b>							
$V_{IL}$	LOW-level input voltage		-	-	0.8	V	
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V	
$I_{LI}$	input leakage current	$V_I = V_{SS}\text{ or }V_{DD}$	-	-	$\pm 1$	$\mu\text{A}$	
$C_i$	input capacitance		[3]	-	-	10	pF
<b>Input OSC</b>							
$I_{osc}$	oscillator start-up current	$V_I = V_{SS}$	0.5	1.2	5.0	$\mu\text{A}$	
<b>LCD outputs</b>							
$V_{BP}$	voltage on pin BP		-	$\pm 20$	-	mV	
$Z_{O(BP)}$	backplane driver output impedance	$V_{DD} = 5\text{ V}$	[4]	-	0.5	5.0	$\text{k}\Omega$
$Z_{O(S)}$	segment driver output impedance	$V_{DD} = 5\text{ V}$	[4]	-	1	7	$\text{k}\Omega$

[1] Outputs open; C-bus inactive; see [Figure 13](#).

[2] Resets all logic, when  $V_{DD} < V_{POR}$ .

[3] Periodically sampled (not 100 % tested).

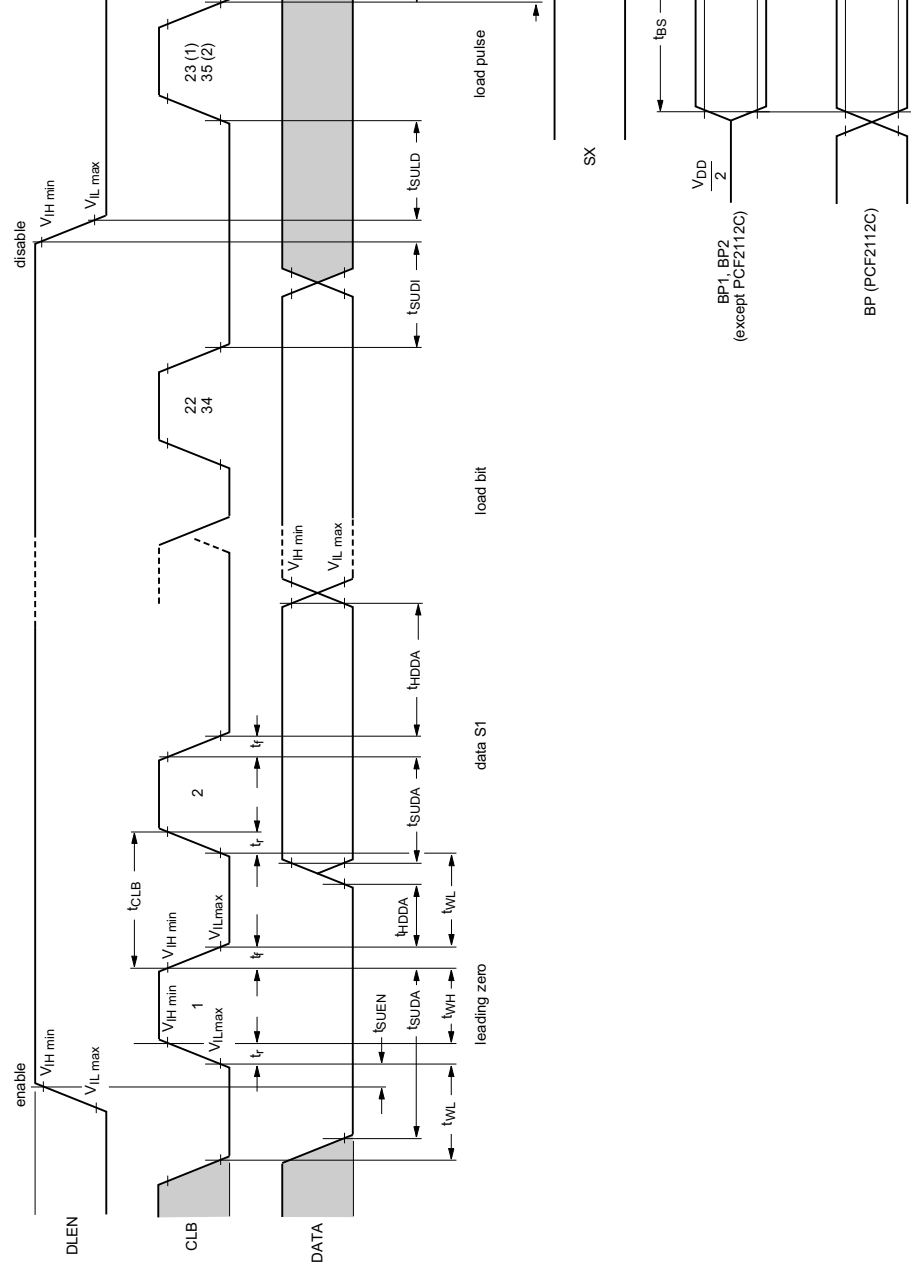
[4] Outputs measured one at a time.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{DD} = 2.25\text{ V to }6.0\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+80\text{ °C}$ ;  $R_O = 1\text{ M}\Omega$ ;  $C_O = 680\text{ pF}$ ; all timing values are referenced to  $V_{IH}$  and  $V_{IL}$  levels with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ ; unless otherwise specified.

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
<b>Inputs CLB, DATA and DLEN; see Figure 12</b>						
t <sub>SUDA</sub>	data setup time		3	-	-	μs
t <sub>HDDA</sub>	data hold time		3	-	-	μs
t <sub>SUEN</sub>	enable setup time		1	-	-	μs
t <sub>SUDI</sub>	disable setup time		2	-	-	μs
t <sub>SULD</sub>	load pulse setup time		2.5	-	-	μs
t <sub>BUSY</sub>	busy time		3	-	-	μs
t <sub>WH</sub>	CLB HIGH time		1	-	-	μs
t <sub>WL</sub>	CLB LOW time		5	-	-	μs
t <sub>CLB</sub>	CLB cycle time		10	-	-	μs
t <sub>r</sub>	rise time		-	-	10	μs
t <sub>f</sub>	fall time		-	-	10	μs
<b>LCD timing; see Figure 12 to Figure 17</b>						
f <sub>LCD</sub>		PCF2100C, PCF2111C	60	75	100	Hz
		PCF2112C; C <sub>O</sub> = 1.5 nF	30	35	50	Hz
t <sub>BS</sub>	transfer time	with test loads; V <sub>DD</sub> = 5 V	-	20	100	μs
t <sub>PLCD</sub>	driver delay time	with test loads; V <sub>DD</sub> = 5 V	-	20	100	μs



- (1) Load pulse 23 for PCF2100C; see [Figure 7](#).
- (2) Load pulse 35 for PCF2111C and PCF212C; see [Figure 7](#).

**Fig 12. C-bus timing**

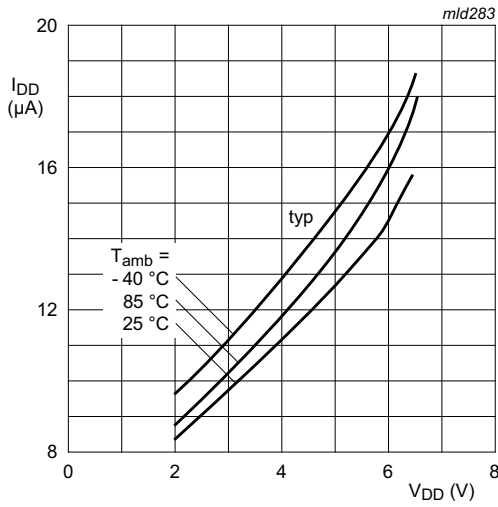


Fig 13. Supply current as a function of supply voltage

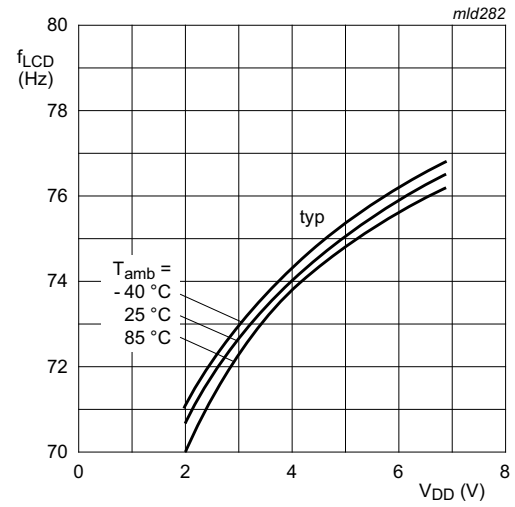


Fig 14. Display frequency as a function of supply voltage;  $C_O = 680 \text{ pF}$  (except PCF2112C)

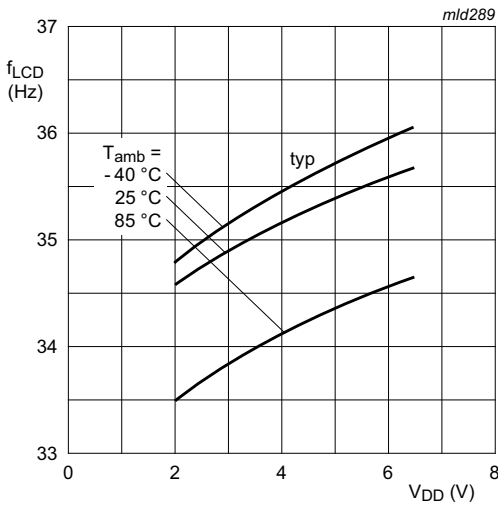


Fig 15. Display frequency as a function of supply voltage;  $C_O = 1.5 \text{ nF}$  (only PCF2112C)

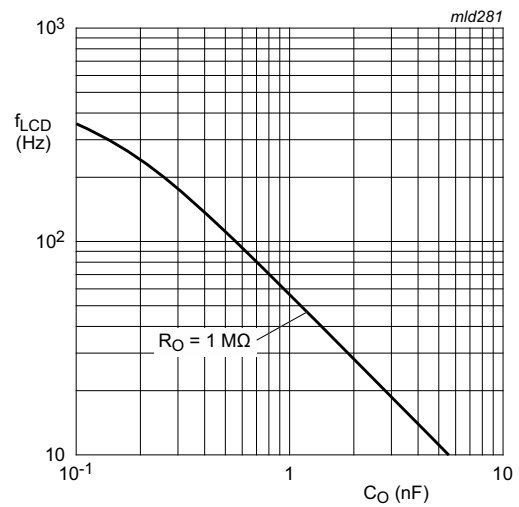


Fig 16. Display frequency as a function of  $R_O$  and  $C_O$ ;  $T_{amb} = 25 \text{ °C}$ ;  $V_{DD} = 5 \text{ V}$

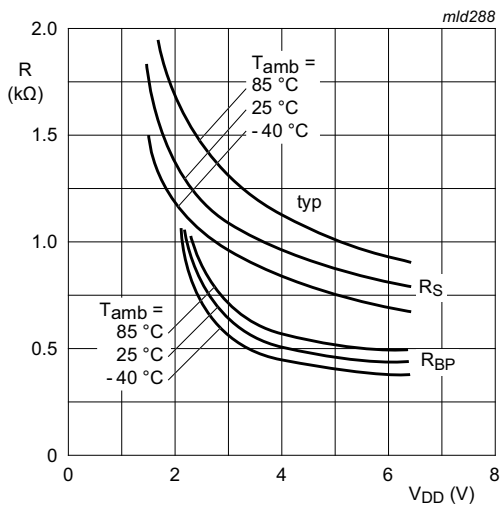


Fig 17. Output resistance of backplane and segments as a function of supply voltage

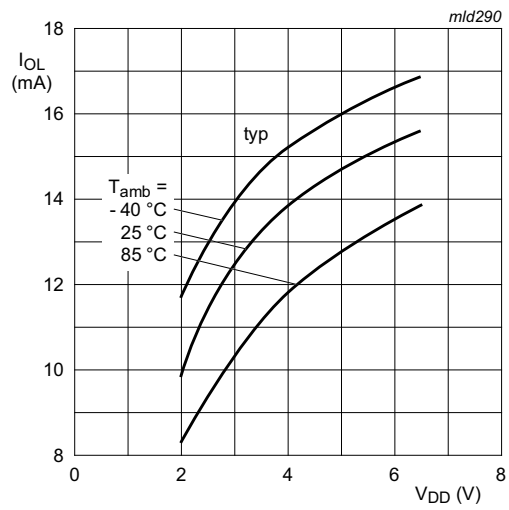


Fig 18. LOW-level output current as a function of supply voltage (only PCF2112C)

## 12. Package outline

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1

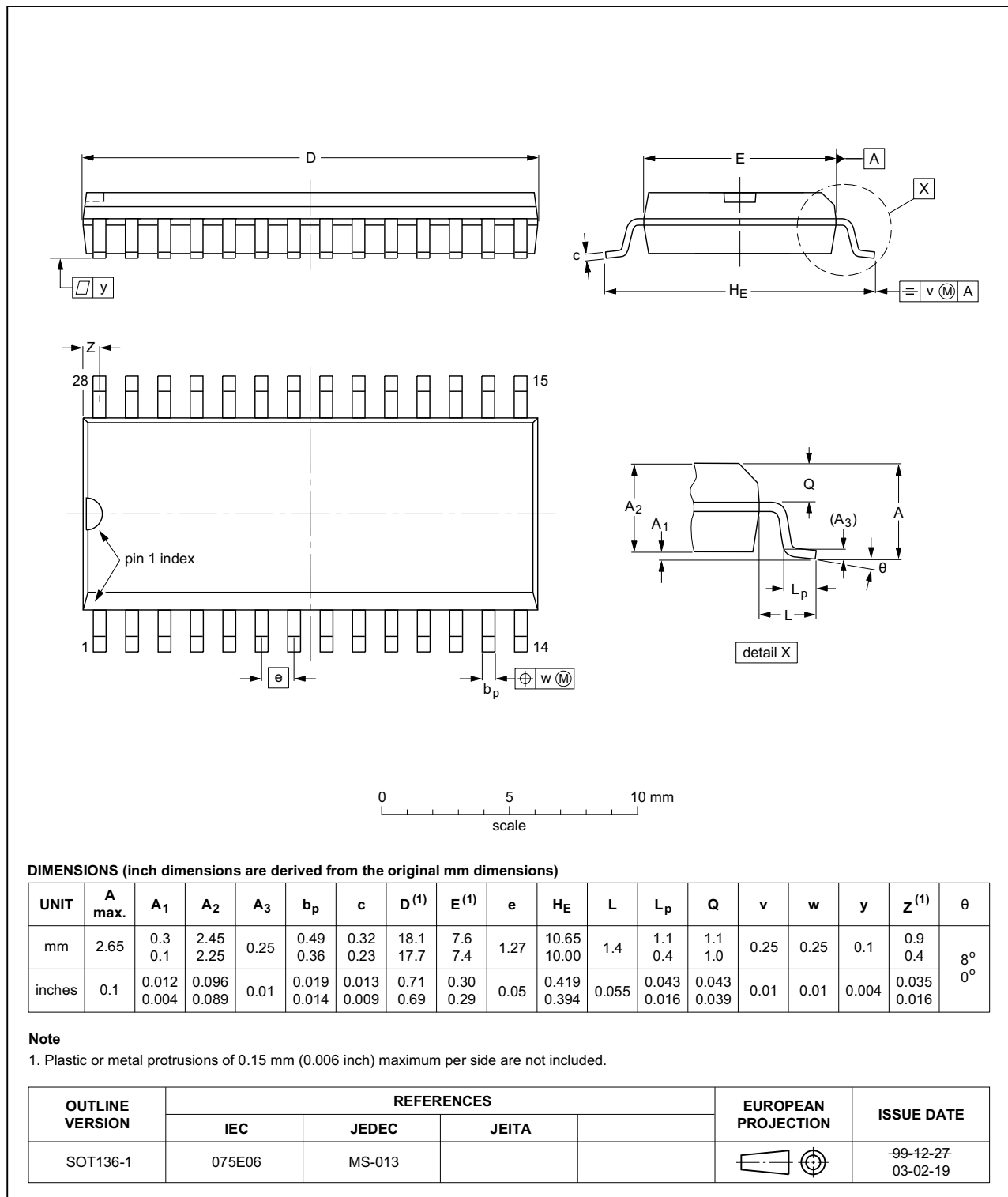


Fig 19. Package outline SOT136-1 (SO28)

VSO40: plastic very small outline package; 40 leads

SOT158-1

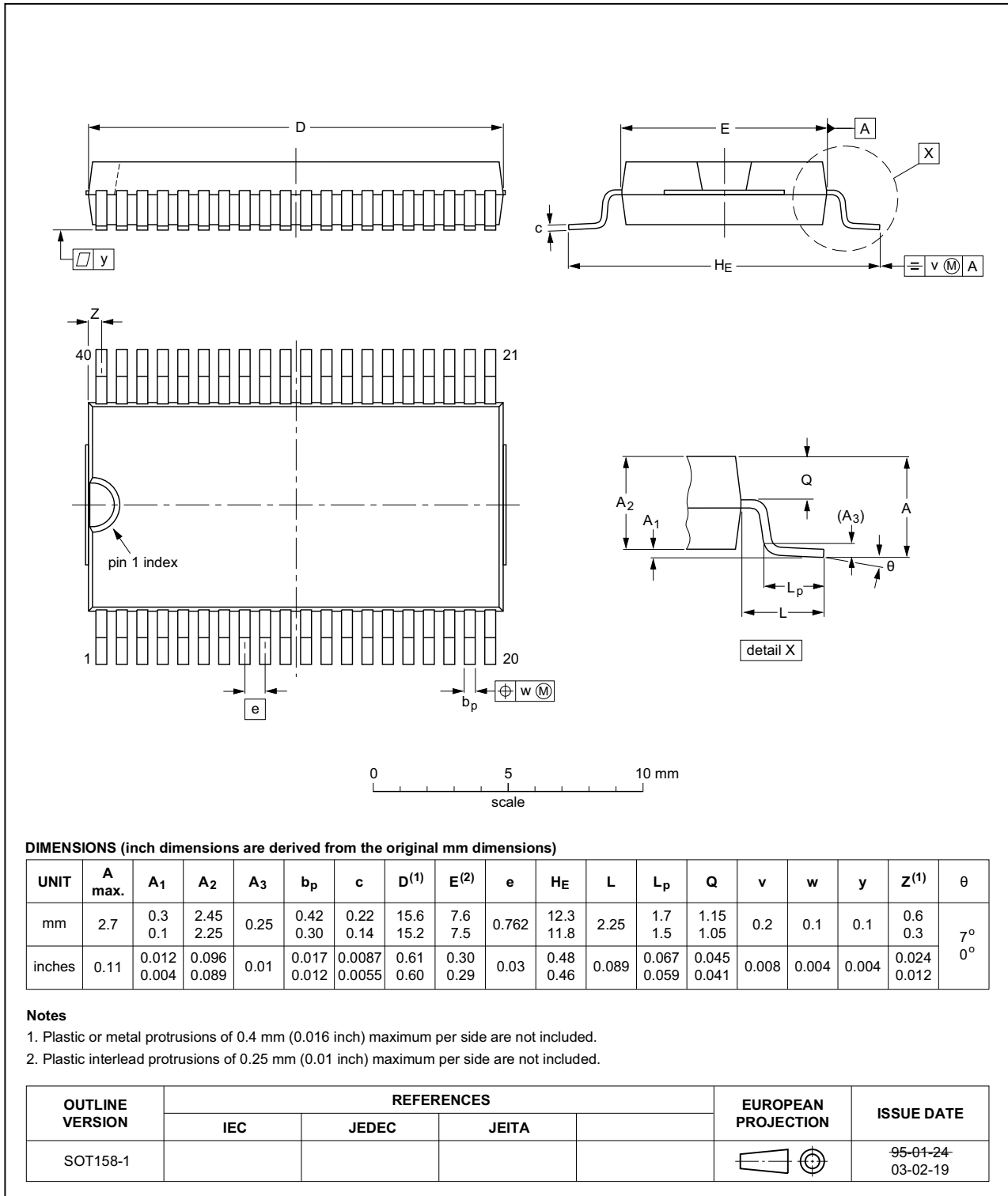


Fig 20. Package outline SOT158-1 (VSO40)

## 13. Handling information

---

All input and output pins meet the requirements of the *MIL-STD-883 class 2*, method 3015 ElectroStatic Discharge (ESD) test. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 14. Packing information

---

### 14.1 Tape and reel information

For tape and reel packing information, see [Ref. 10 "SOT136-1\\_118"](#) and [Ref. 11 "SOT158-1\\_118"](#).

## 15. Soldering of SMD packages

---

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation

- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 21](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

**Table 8. SnPb eutectic process (from J-STD-020D)**

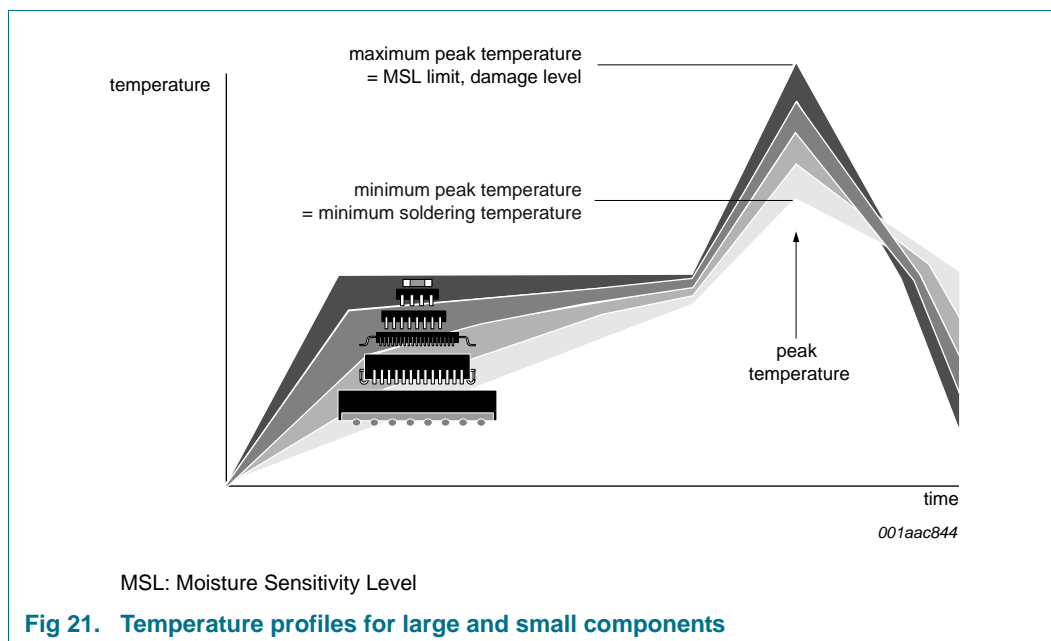
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 9. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 21](#).



For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10853** — ESD and EMC sensitivity of IC
- [3] **AN11267** — EMC and system level ESD design guidelines for LCD drivers
- [4] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [5] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [6] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [7] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **SOT136-1\_118** — SO28; Reel dry pack; SMD, 13", packing information
- [11] **SOT158-1\_118** — VSO40; Reel pack; SMD, 13", packing information
- [12] **UM10204** — I<sup>2</sup>C-bus specification and user manual
- [13] **UM10569** — Store and transport requirements

## 17. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF21XXC_FAM v.3	20150506	Product data sheet	-	PCF21XXC_FAMILY v.2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Changed <a href="#">Figure 16</a>.</li></ul>			
PCF21XXC_FAMILY v.2	19970328	Product specification	-	PCF21XXC_FAMILY v.1
PCF21XXC_FAMILY v.1	19950503	-	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 20. Tables

---

Table 1.	Ordering information	1
Table 2.	Ordering options	2
Table 3.	Marking codes	2
Table 4.	Pin description	4
Table 5.	Limiting values	9
Table 6.	Static characteristics	10
Table 7.	Dynamic characteristics	11
Table 8.	SnPb eutectic process (from J-STD-020D)	18
Table 9.	Lead-free process (from J-STD-020D)	18
Table 10.	Revision history	20

## 21. Figures

Fig 1.	Block diagram; PCF2100C	2
Fig 2.	Block diagram; PCF2111C	3
Fig 3.	Block diagram; PCF2112C	3
Fig 4.	Pin configuration PCF2100C (SOT136-1)	4
Fig 5.	Pin configuration PCF211C (SOT158-1)	4
Fig 6.	Pin configuration PCF2112C (SOT158-1)	4
Fig 7.	C-bus data format	6
Fig 8.	Timing diagram for PCF2100C and PCF2111C	7
Fig 9.	Timing diagram for PCF2112C	7
Fig 10.	Input circuitry	8
Fig 11.	Expansion possibility (using PCF2111C)	8
Fig 12.	C-bus timing	12
Fig 13.	Supply current as a function of supply voltage	13
Fig 14.	Display frequency as a function of supply voltage; $C_O = 680 \text{ pF}$ (except PCF2112C)	13
Fig 15.	Display frequency as a function of supply voltage; $C_O = 1.5 \text{ nF}$ (only PCF2112C)	13
Fig 16.	Display frequency as a function of $R_O$ and $C_O$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$ ; $V_{DD} = 5 \text{ V}$	13
Fig 17.	Output resistance of backplane and segments as a function of supply voltage	14
Fig 18.	LOW-level output current as a function of supply voltage (only PCF2112C)	14
Fig 19.	Package outline SOT136-1 (SO28)	15
Fig 20.	Package outline SOT158-1 (VSO40)	16
Fig 21.	Temperature profiles for large and small components	19

## 22. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
3.1	Ordering options .....	2
<b>4</b>	<b>Marking</b> .....	<b>2</b>
<b>5</b>	<b>Block diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>6</b>
7.1	PCF2100C .....	6
7.2	PCF2111C .....	6
7.3	PCF2112C .....	6
7.4	Bus control logic .....	6
7.5	Timing .....	7
7.6	Input circuitry .....	8
7.7	Expansion .....	8
<b>8</b>	<b>Safety notes</b> .....	<b>9</b>
<b>9</b>	<b>Limiting values</b> .....	<b>9</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>10</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>11</b>
<b>12</b>	<b>Package outline</b> .....	<b>15</b>
<b>13</b>	<b>Handling information</b> .....	<b>17</b>
<b>14</b>	<b>Packing information</b> .....	<b>17</b>
14.1	Tape and reel information .....	17
<b>15</b>	<b>Soldering of SMD packages</b> .....	<b>17</b>
15.1	Introduction to soldering .....	17
15.2	Wave and reflow soldering .....	17
15.3	Wave soldering .....	18
15.4	Reflow soldering .....	18
<b>16</b>	<b>References</b> .....	<b>19</b>
<b>17</b>	<b>Revision history</b> .....	<b>20</b>
<b>18</b>	<b>Legal information</b> .....	<b>21</b>
18.1	Data sheet status .....	21
18.2	Definitions .....	21
18.3	Disclaimers .....	21
18.4	Trademarks .....	22
<b>19</b>	<b>Contact information</b> .....	<b>22</b>
<b>20</b>	<b>Tables</b> .....	<b>23</b>
<b>21</b>	<b>Figures</b> .....	<b>24</b>
<b>22</b>	<b>Contents</b> .....	<b>25</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 6 May 2015

Document identifier: PCF21XXC\_FAM







## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View PCF2111CT/1,118 on WIN SOURCE](#)

 [NXP / Nexperia Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management