# PCA9553

## 4-bit I²C-bus LED driver with programmable blink rates

Rev. 06 — 29 December 2008 Product data sheet

## 1. General description

The PCA9553 LED blinker blinks LEDs in I²C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I²C-bus master's (MCU, MPU, DSP, chip set, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I²C-bus and uses up one of the master's timers. The PCA9553 LED blinker instead requires only the initial set-up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle). From then on, only one command from the bus master is required to turn each individual open-drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 100 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Due to pin limitations, the PCA9553 is not featured with hardware address pins. The PCA9553/01 and the PCA9553/02 have different fixed I²C-bus addresses allowing operation of both on the same bus.

## 2. Features

- 4 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.172 Hz and 44 Hz (5.82 seconds and 0.023 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- 4 open-drain outputs directly drive LEDs to 25 mA
- Controlled edge rates to minimize ground bounce
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 Hz to 400 kHz clock frequency

- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8), HVSON8

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PCA9553D/01 | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| PCA9553D/02 | | | |
| PCA9553DP/01 | TSSOP8[1] | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| PCA9553DP/02 | | | |
| PCA9553TK[2] | HVSON8 | plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm | SOT908-1 |
| PCA9553TK/02 | | | |

[1] Also known as MSOP8.

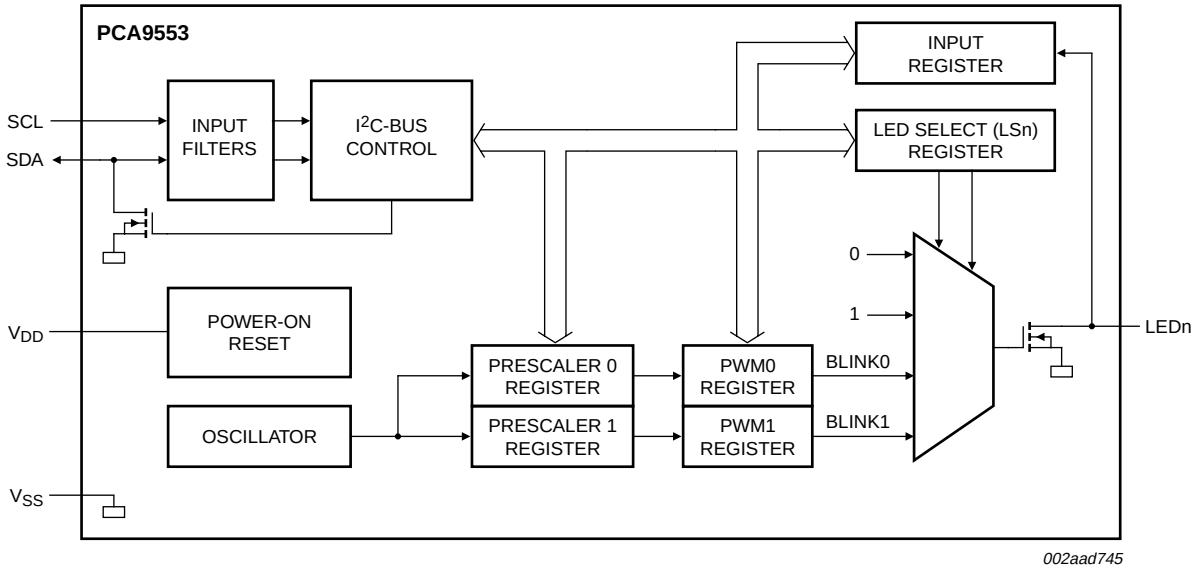
[2] PCA9553TK uses version /01 address.

## 4. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| PCA9553D/01 | 9553/1 |
| PCA9553D/02 | 9553/2 |
| PCA9553DP/01 | P53/1 |
| PCA9553DP/02 | P53/2 |
| PCA9553TK | P53/1 |
| PCA9553TK/02 | P53/2 |

## 5. Block diagram




Only one I/O shown for clarity.

**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

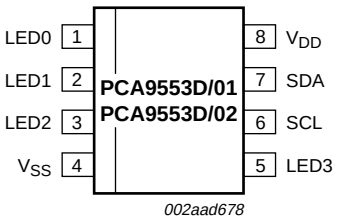



Fig 2. Pin configuration for SO8

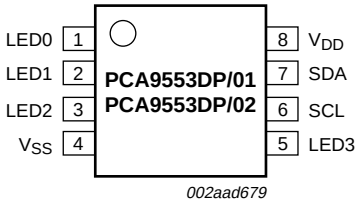
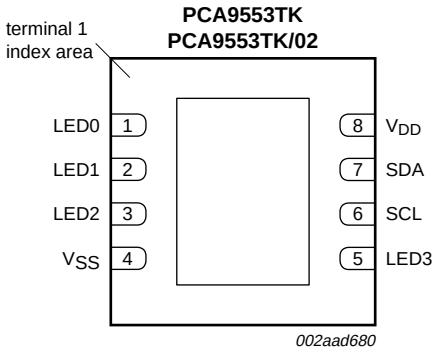



Fig 3. Pin configuration for TSSOP8




Transparent top view

Fig 4. Pin configuration for HVSON8

## 6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|---|---|---|
| LED0 | 1 | LED driver 0 |
| LED1 | 2 | LED driver 1 |
| LED2 | 3 | LED driver 2 |
| $V_{SS}$ | 4[1] | supply ground |
| LED3 | 5 | LED driver 3 |
| SCL | 6 | serial clock line |
| SDA | 7 | serial data line |
| $V_{DD}$ | 8 | supply voltage |

[1] HVSON8 package die supply ground is connected to both $V_{SS}$ pin and exposed center pad. $V_{SS}$ pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

# 7. Functional description

Refer to Figure 1 “Block diagram”.

## 7.1 Device address

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9553/01 is shown in Figure 5 and PCA9553/02 in Figure 6.

PCA9553TK uses the version /01 address.

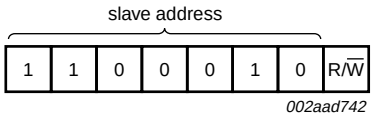



**Fig 5. PCA9553/01 slave address**

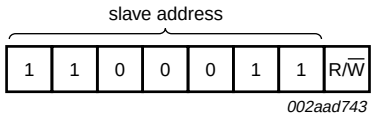
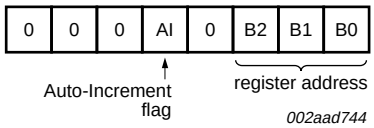



**Fig 6. PCA9553/02 slave address**

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

## 7.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9553 which will be stored in the Control register.




Reset state: 00h

**Fig 7. Control register**

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the Auto-Increment flag is set, the three low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to ‘000’ after the last register is accessed.

When the Auto-Increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from ‘0’ (B2 B1 B0 ≠ 0 0 0).

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

Table 4. Control register definition

| B2 | B1 | B0 | Register name | Type | Register function |
|---|---|---|---|---|---|
| 0 | 0 | 0 | INPUT | read | input register |
| 0 | 0 | 1 | PSC0 | read/write | frequency prescaler 0 |
| 0 | 1 | 0 | PWM0 | read/write | PWM register 0 |
| 0 | 1 | 1 | PSC1 | read/write | frequency prescaler 1 |
| 1 | 0 | 0 | PWM1 | read/write | PWM register 1 |
| 1 | 0 | 1 | LS0 | read/write | LED selector |

## 7.3 Register descriptions

### 7.3.1 INPUT - Input register

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

Table 5. INPUT - Input register description

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | INPUT[7] | INPUT[6] | INPUT[5] | INPUT[4] | LED3 | LED2 | LED1 | LED0 |
| Default | 0 | 0 | 0 | 0 | X | X | X | X |

**Remark:** The default value ‘X’ is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to $V_{DD}$.

### 7.3.2 PSC0 - Frequency Prescaler 0

PSC0 is used to program the period of the PWM output.

The period of BLINK0 = (PSC0 + 1) / 44.

Table 6. PSC0 - Frequency Prescaler 0 register description

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | PSC0[7] | PSC0[6] | PSC0[5] | PSC0[4] | PSC0[3] | PSC0[2] | PSC0[1] | PSC0[0] |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 7.3.3 PWM0 - Pulse Width Modulation 0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

The duty cycle of BLINK0 = (256 – PWM0) / 256.

Table 7. PWM0 - Pulse Width Modulation 0 register description

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | PWM0 [7] | PWM0 [6] | PWM0 [5] | PWM0 [4] | PWM0 [3] | PWM0 [2] | PWM0 [1] | PWM0 [0] |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.4 PSC1 - Frequency Prescaler 1

PSC1 is used to program the period of the PWM output.

The period of BLINK1 = (PSC1 + 1) / 44.

**Table 8. PSC1 - Frequency Prescaler 1 register description**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | PSC1[7] | PSC1[6] | PSC1[5] | PSC1[4] | PSC1[3] | PSC1[2] | PSC1[1] | PSC1[0] |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 7.3.5 PWM1 - Pulse Width Modulation 1

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

The duty cycle of BLINK1 = (256 – PWM1) / 256.

**Table 9. PWM1 - Pulse Width Modulation 1 register description**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | PWM1 [7] | PWM1 [6] | PWM1 [5] | PWM1 [4] | PWM1 [3] | PWM1 [2] | PWM1 [1] | PWM1 [0] |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.3.6 LS0 - LED selector register

The LS0 LED select register determines the source of the LED data.

00 = output is set LOW (LED on)

01 = output is set high-impedance (LED off; default)

10 = output blinks at PWM0 rate

11 = output blinks at PWM1 rate

**Table 10. LS0 - LED selector register bit description**

*Legend: * default value.*

| Register | Bit | Value | Description |
|---|---|---|---|
| **LS0 - LED0 to LED3 selector** | | | |
| LS0 | 7:6 | 01* | LED3 selected |
| | 5:4 | 01* | LED2 selected |
| | 3:2 | 01* | LED1 selected |
| | 1:0 | 01* | LED0 selected |

### 7.4 Pins used as general purpose I/Os

LED pins not used to control LEDs can be used as general purpose I/Os.

For use as input: Set LEDn to high-impedance (01) and then read the pin state via the Input register.

For use as output: Connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the 'LED selector' register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

### 7.5 Power-on reset

When power is applied to $V_{DD}$, an internal Power-On Reset (POR) holds the PCA9553 in a reset condition until $V_{DD}$ has reached $V_{POR}$. At that point, the reset condition is released and the PCA9553 registers are initialized to their default states, with all outputs in the OFF state. Thereafter, $V_{DD}$ must be lowered below 0.2 V to reset the device.

## 8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

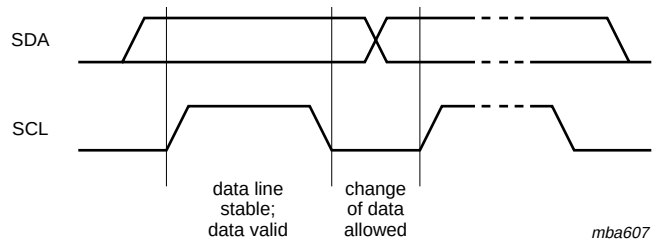



**Fig 8. Bit transfer**

#### 8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

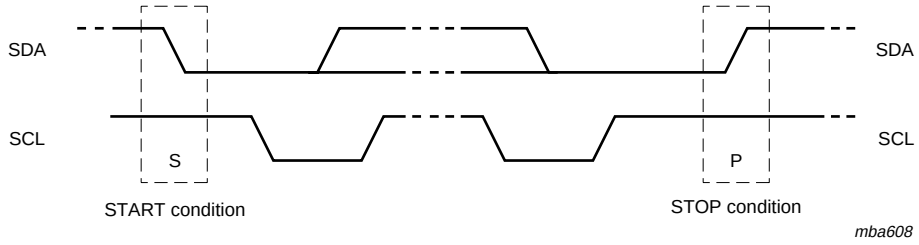



**Fig 9. Definition of START and STOP conditions**

## 8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

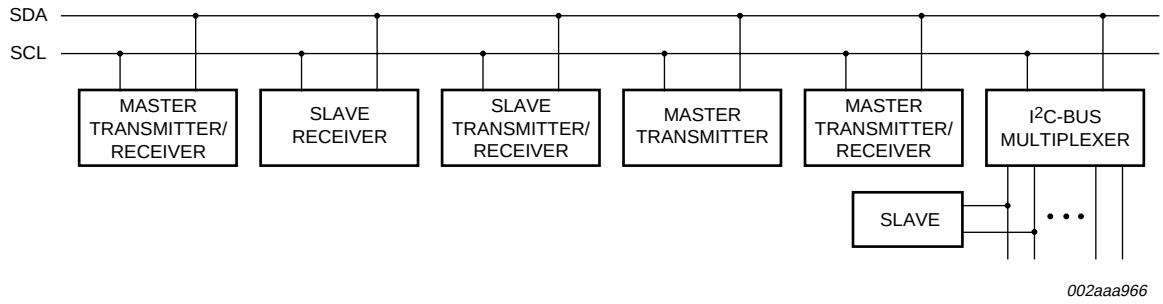



**Fig 10. System configuration**

## 8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

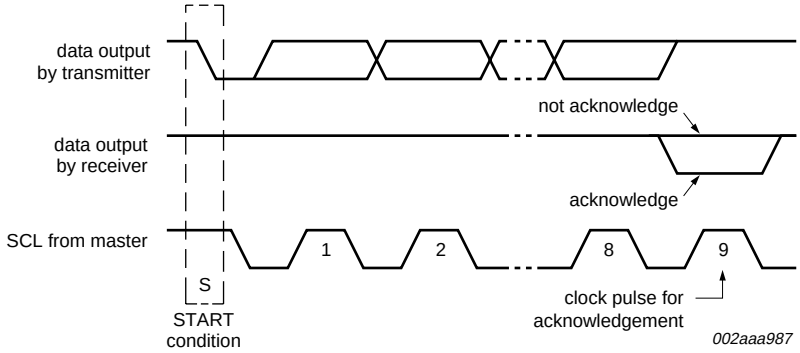



**Fig 11. Acknowledgement on the I²C-bus**

## 8.4 Bus transactions

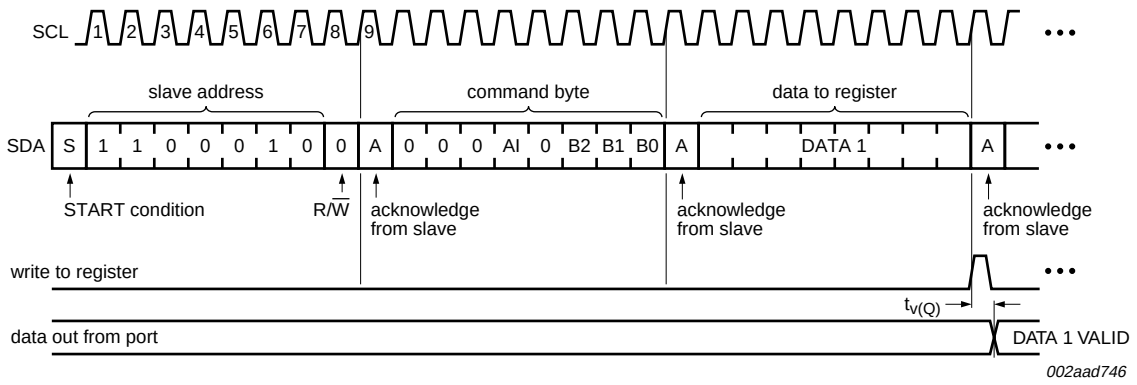



**Fig 12. Write to register**

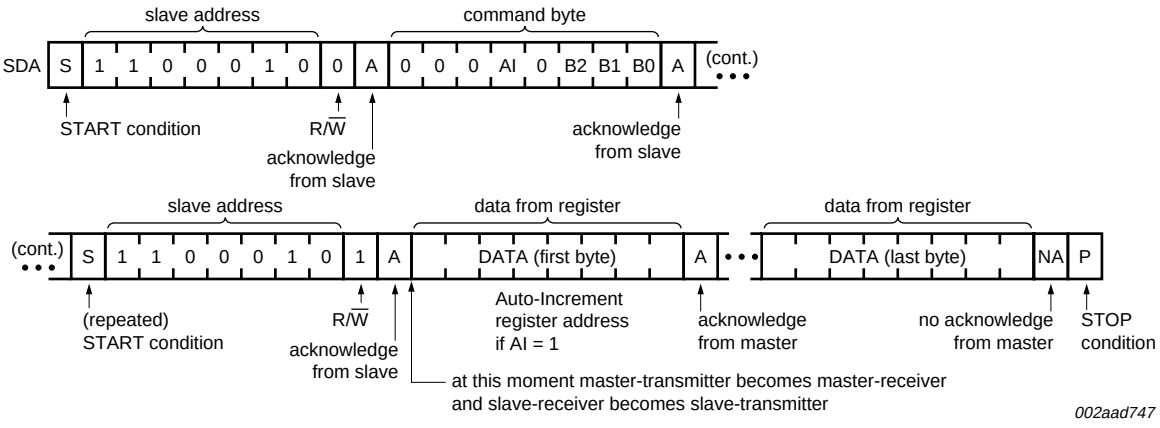
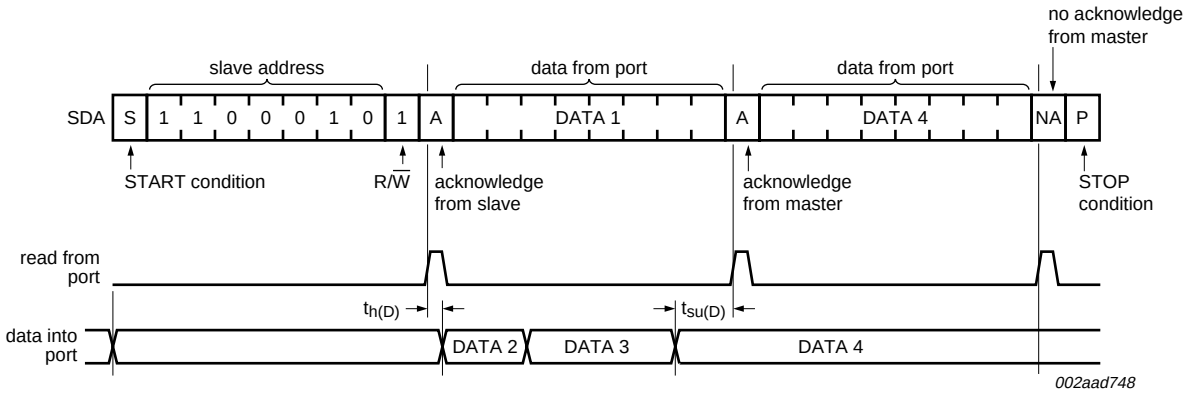



**Fig 13. Read from register**




This figure assumes the command byte has previously been programmed with 00h.

PCA9553/01 shown.

**Fig 14. Read input port register**

# 9. Application design-in information

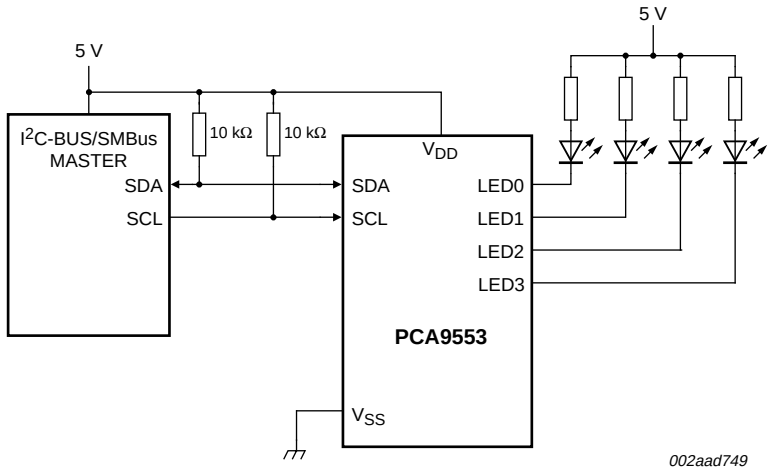



**Fig 15. Typical application**

## 9.1 Minimizing $I_{DD}$ when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to $V_{DD}$ through a resistor as shown in Figure 15. Since the LED acts as a diode, when the LED is off the I/O $V_I$ is about 1.2 V less than $V_{DD}$. The supply current, $I_{DD}$, increases as $V_I$ becomes lower than $V_{DD}$ and is specified as $\Delta I_{DD}$ in Table 13 “Static characteristics”.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to $V_{DD}$ when the LED is off. Figure 16 shows a high value resistor in parallel with the LED. Figure 17 shows $V_{DD}$ less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O $V_I$ at or above $V_{DD}$ and prevents additional supply current consumption when the LED is off.

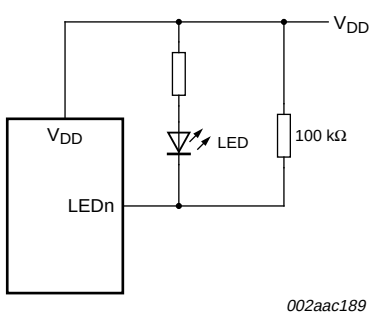



Fig 16. High value resistor in parallel with the LED

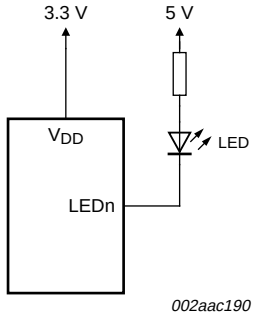



Fig 17. Device supplied by a lower voltage

## 9.2 Programming example

The following example shows how to set LED0 and LED1 off. It will then set LED2 to blink at 1 Hz, 50 % duty cycle. LED3 will be set to blink at 4 Hz, 25 % duty cycle. PCA9553/01 is used in this example.

Table 11. Programming PCA9553

| Program sequence | I²C-bus |
|---|---|
| START | S |
| PCA9553 address | C4h |
| PSC0 subaddress + Auto-Increment | 11h |
| Set prescaler PSC0 to achieve a period of 1 second: $Blink\ period = 1 = \frac{PSC0 + 1}{44}$ PSC0 = 43 | 2Bh |
| Set PWM0 duty cycle to 50 %: $\frac{256 - PWM0}{256} = 0.5$ PWM0 = 128 | 80h |
| Set prescaler PSC1 to achieve a period of 0.25 seconds: $Blink\ period = 0.25 = \frac{PSC1 + 1}{44}$ PSC1 = 10 | 0Ah |
| Set PWM1 output duty cycle to 25 %: $\frac{256 - PWM1}{256} = 0.25$ PWM1 = 192 | C0h |
| Set LED0 on, LED1 off, LED2 set to blink at PSC0, PWM0, LED3 set to blink at PSC1, PWM1 | E4h |
| STOP | P |

## 10. Limiting values

**Table 12. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +6.0 | V |
| $V_{I/O}$ | voltage on an input/output pin | | $V_{SS}$ – 0.5 | 5.5 | V |
| $I_{O(LEDn)}$ | output current on pin LEDn | | - | ±25 | mA |
| $I_{SS}$ | ground supply current | | - | 100 | mA |
| $P_{tot}$ | total power dissipation | | - | 400 | mW |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating | –40 | +85 | °C |

## 11. Static characteristics

**Table 13. Static characteristics**

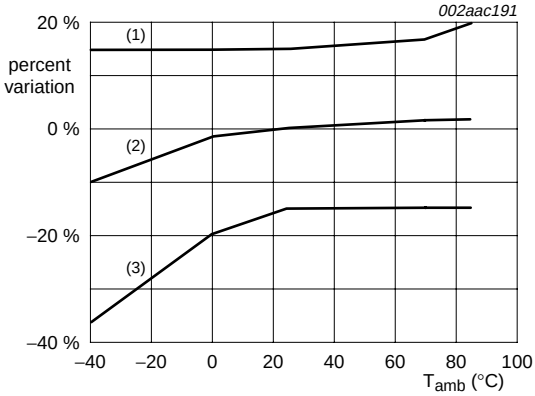
*$V_{DD}$ = 2.3 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 2.3 | - | 5.5 | V |
| $I_{DD}$ | supply current | operating mode; $V_{DD}$ = 5.5 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | | - | 350 | 500 | µA |
| $I_{stb}$ | standby current | Standby mode; $V_{DD}$ = 5.5 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | | - | 1.9 | 3.0 | µA |
| $\Delta I_{DD}$ | additional quiescent supply current | Standby mode; $V_{DD}$ = 5.5 V; every LED I/O at $V_I$ = 4.3 V; $f_{SCL}$ = 0 kHz | | - | - | 325 | µA |
| $V_{POR}$ | power-on reset voltage | no load; $V_I = V_{DD}$ or $V_{SS}$ | [2] | - | 1.7 | 2.2 | V |
| **Input SCL; input/output SDA** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | −0.5 | - | $+0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | 5.5 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 3 | 6.5 | - | mA |
| $I_L$ | leakage current | $V_I = V_{DD} = V_{SS}$ | | −1 | - | +1 | µA |
| $C_i$ | input capacitance | $V_I = V_{SS}$ | | - | 3.7 | 5 | pF |
| **I/Os** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | −0.5 | - | +0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | | 2.0 | - | 5.5 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | | | | |
| | | $V_{DD}$ = 2.3 V | [3] | 9 | - | - | mA |
| | | $V_{DD}$ = 3.0 V | [3] | 12 | - | - | mA |
| | | $V_{DD}$ = 5.0 V | [3] | 15 | - | - | mA |
| | | $V_{OL}$ = 0.7 V | | | | | |
| | | $V_{DD}$ = 2.3 V | [3] | 15 | - | - | mA |
| | | $V_{DD}$ = 3.0 V | [3] | 20 | - | - | mA |
| | | $V_{DD}$ = 5.0 V | [3] | 25 | - | - | mA |
| $I_{LI}$ | input leakage current | $V_{DD}$ = 3.6 V; $V_I$ = 0 V or $V_{DD}$ | | −1 | - | +1 | µA |
| $C_{io}$ | input/output capacitance | | | - | 2.1 | 5 | pF |

[1] Typical limits at $V_{DD}$ = 3.3 V, $T_{amb}$ = 25 °C.

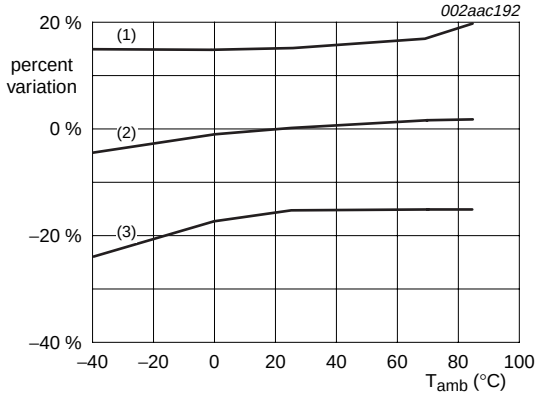
[2] $V_{DD}$ must be lowered to 0.2 V in order to reset part.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.




(1) maximum
(2) average
(3) minimum

**Fig 18. Typical frequency variation over process at $V_{DD}$ = 2.3 V to 3.0 V**




(1) maximum
(2) average
(3) minimum

**Fig 19. Typical frequency variation over process at $V_{DD}$ = 3.0 V to 5.5 V**

## 12. Dynamic characteristics

**Table 14. Dynamic characteristics**

| Symbol | Parameter | Conditions | | Standard-mode I²C-bus | | Fast-mode I²C-bus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 4.7 | - | 1.3 | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 4.0 | - | 0.6 | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 4.7 | - | 0.6 | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 4.0 | - | 0.6 | - | µs |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | 0 | - | ns |
| $t_{VD;ACK}$ | data valid acknowledge time | | [1] | - | 600 | - | 600 | ns |
| $t_{VD;DAT}$ | data valid time | LOW-level | [2] | - | 600 | - | 600 | ns |
| | | HIGH-level | [2] | - | 1500 | - | 600 | ns |
| $t_{SU;DAT}$ | data set-up time | | | 250 | - | 100 | - | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 4.0 | - | 0.6 | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | | | - | 1000 | $20 + 0.1C_b$ [3] | 300 | ns |
| $t_f$ | fall time of both SDA and SCL signals | | | - | 300 | $20 + 0.1C_b$ [3] | 300 | ns |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | | - | 50 | - | 50 | ns |
| **Port timing** | | | | | | | | |
| $t_{v(Q)}$ | data output valid time | | | - | 200 | - | 200 | ns |
| $t_{su(D)}$ | data input set-up time | | | 100 | - | 100 | - | ns |
| $t_{h(D)}$ | data input hold time | | | 1 | - | 1 | - | µs |

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data output to be valid following SCL LOW.

[3] $C_b$ = total capacitance of one bus line in pF.

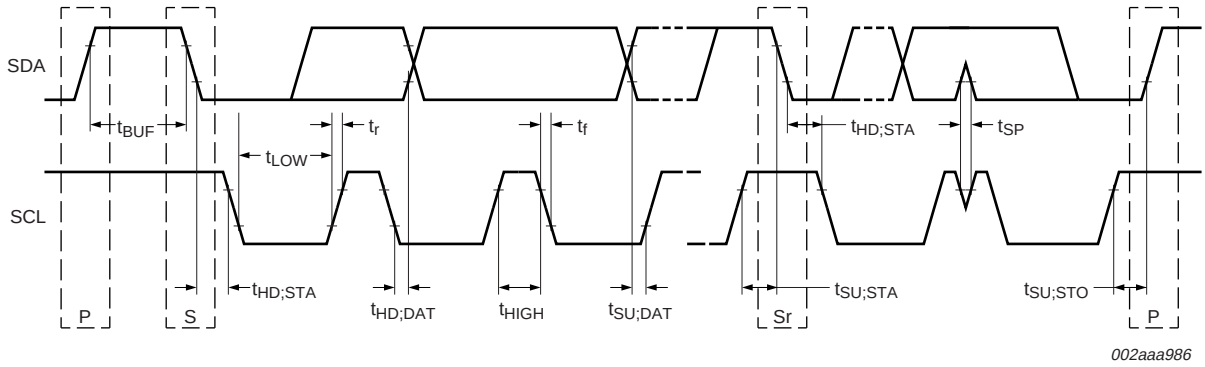
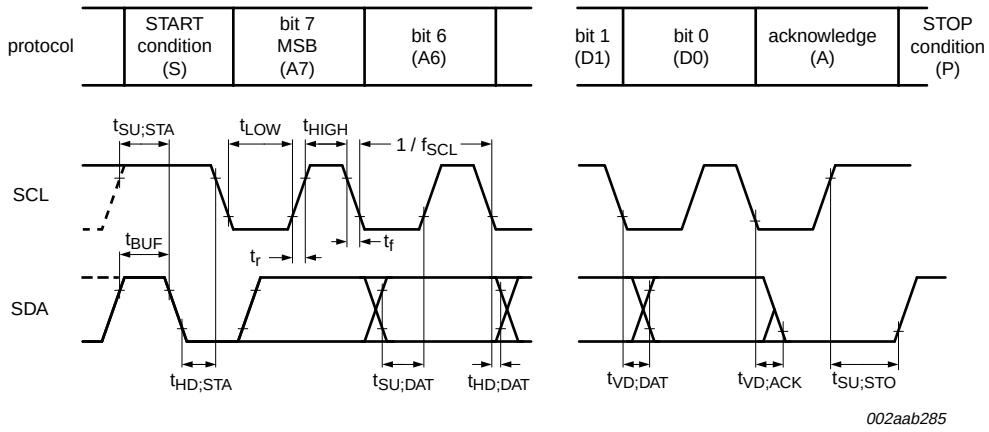


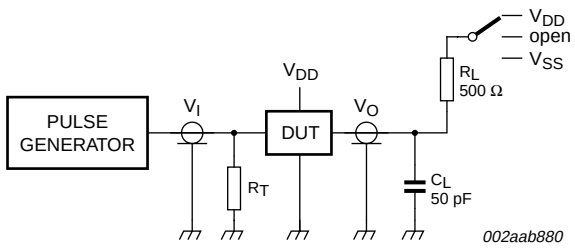

**Fig 20. Definition of timing**




Rise and fall times refer to $V_{IL}$ and $V_{IH}$.

**Fig 21. I²C-bus timing diagram**

## 13. Test information




$R_L$ = load resistor for LEDn. $R_L$ for SDA and SCL > 1 kΩ (3 mA or less current).

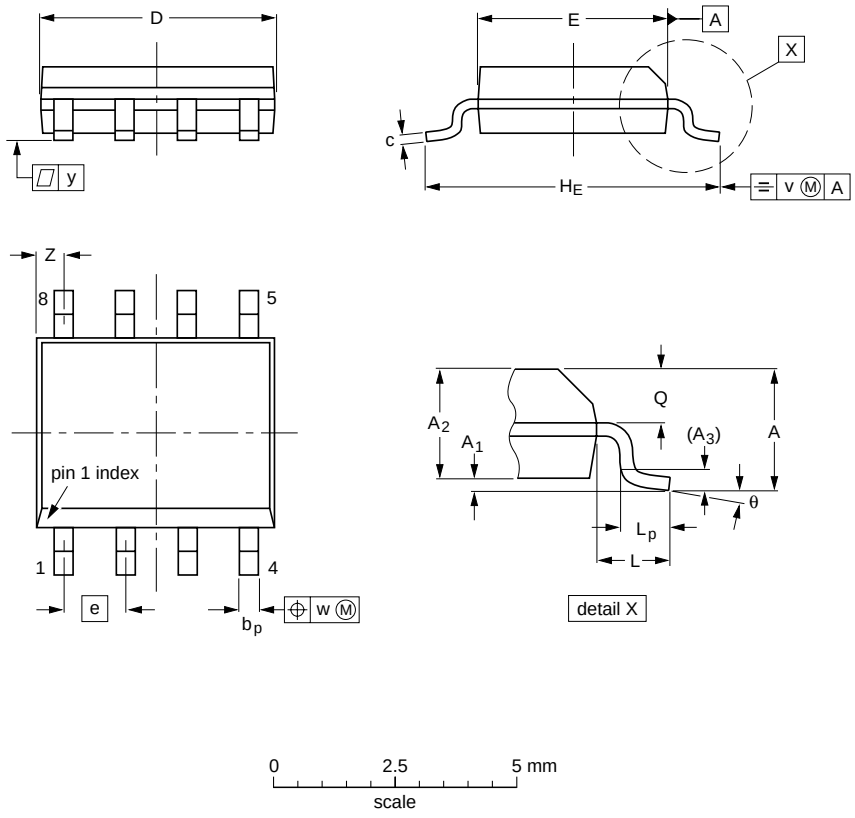
$C_L$ = load capacitance includes jig and probe capacitance.

$R_T$ = termination resistance should be equal to the output impedance $Z_o$ of the pulse generators.

**Fig 22. Test circuitry for switching times**

## 14. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

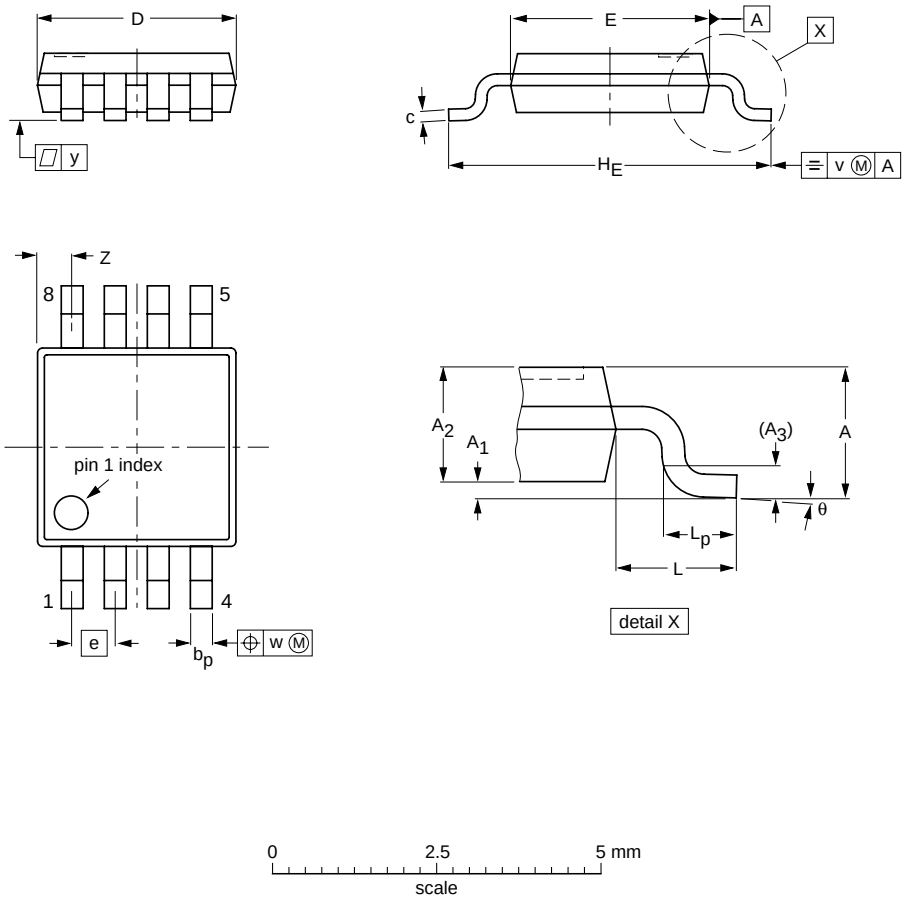
**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 23. Package outline SOT96-1 (SO8)**

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.45<br>0.25 | 0.28<br>0.15 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 5.1<br>4.7 | 0.94 | 0.7<br>0.4 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 6°<br>0° |

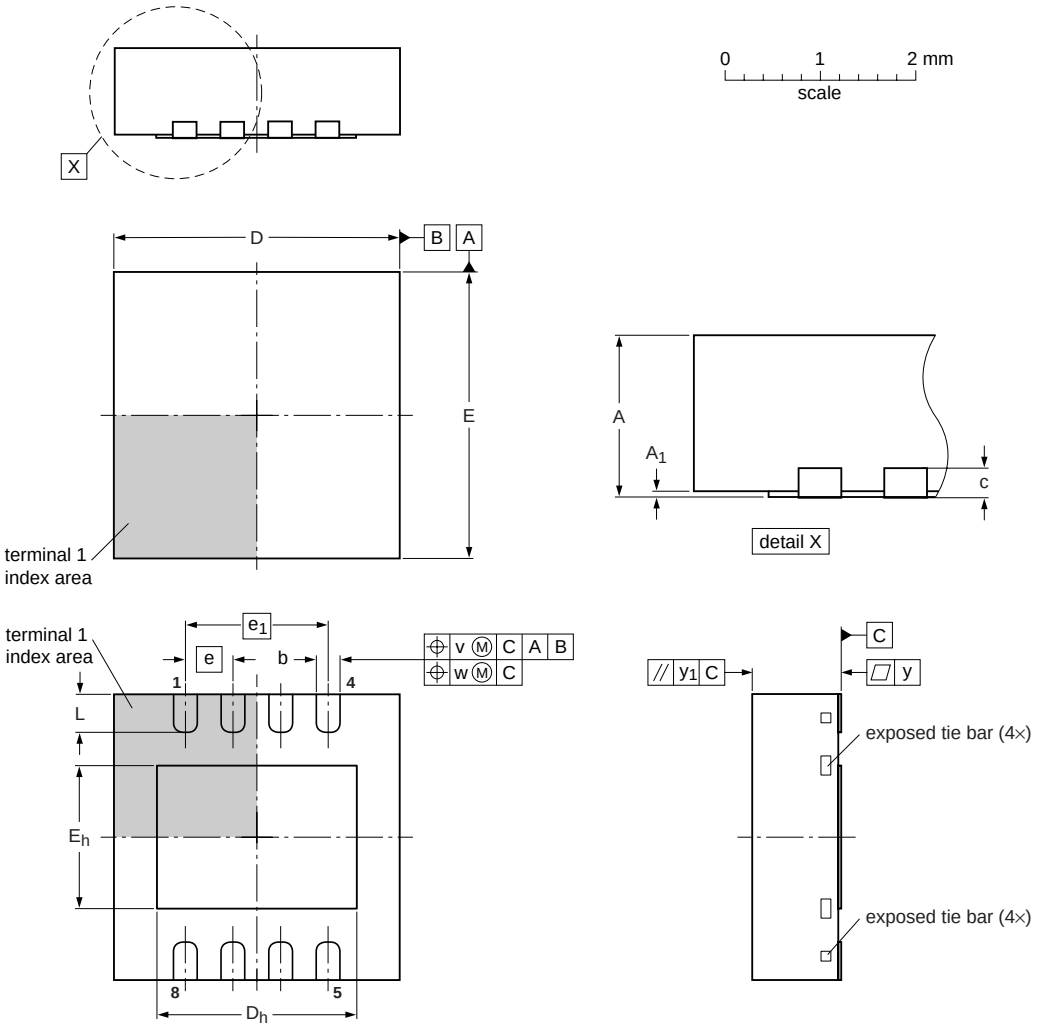
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~<br>03-02-18 |

**Fig 24. Package outline SOT505-1 (TSSOP8)**

**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm** **SOT908-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.3<br>0.2 | 0.2 | 3.1<br>2.9 | 2.25<br>1.95 | 3.1<br>2.9 | 1.65<br>1.35 | 0.5 | 1.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT908-1 | | MO-229 | | | | ~~05-09-26~~<br>05-10-05 |

**Fig 25. Package outline SOT908-1 (HVSON8)**

# 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

**Table 15. SnPb eutectic process (from J-STD-020C)**

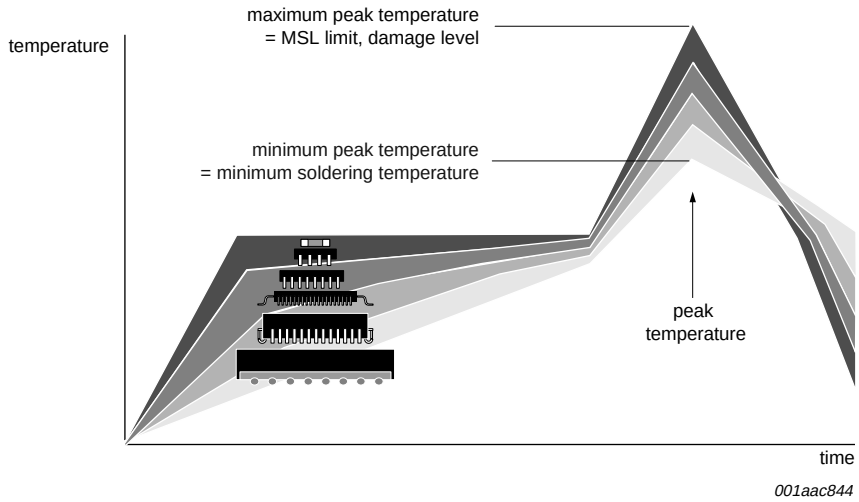
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 16. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.




MSL: Moisture Sensitivity Level

**Fig 26. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Abbreviations

**Table 17. Abbreviations**

| Acronym | Description |
|---|---|
| AI | Auto-Increment |
| CDM | Charged-Device Model |
| DSP | Digital Signal Processor |
| ESD | ElectroStatic Discharge |
| GPIO | General Purpose Input/Output |
| HBM | Human Body Model |
| I²C-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| LED | Light Emitting Diode |
| MCU | MicroController Unit |
| MM | Machine Model |
| MPU | MicroProcessor Unit |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| PWM | Pulse Width Modulation |
| SMBus | System Management Bus |

## 18. Revision history

**Table 18. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9553_6 | 20081229 | Product data sheet | - | PCA9553_5 |
| Modifications: | • Table 2 “Marking codes”:<br>– marking code for type number PCA9553D/01 changed from “P9553/1” to “9553/1”<br>– marking code for type number PCA9553D/02 changed from “P9553/2” to “9553/2”<br>– marking code for type number PCA9553TK changed from “P53” to “P53/1” | | | |
| PCA9553_5 | 20080422 | Product data sheet | - | PCA9553_4 |
| PCA9553_4 | 20060818 | Product data sheet | - | PCA9553_3 |
| PCA9553_3 (9397 750 13728) | 20041001 | Product data sheet | - | PCA9553_2 |
| PCA9553_2 (9397 750 11464) | 20030502 | Product data | ECN 853-2397 29856 dated 2003 Apr 24 | PCA9553_1 |
| PCA9553_1 (9397 750 10859) | 20021213 | Product data | ECN 853-2397 29264 dated 2002 Dec 09 | |

# 19. Legal information

## 19.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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