THE DATASHEET OF

PCA9552PW

PCA9552

16-bit I²C-bus LED driver with programmable blink rates

Rev. 5.1 — 25 May 2023 Product data sheet

1 General description

The PCA9552 LED blinker blinks LEDs in I²C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I²C-bus controller's (MCU, MPU, DSP, chip set, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O expanders like the PCF8574 or PCA9554, the bus controller must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I²C-bus and uses up one of the controller's timers. The PCA9552 LED blinker instead requires only the initial setup command to program BLINK RATE 1 and BLINK RATE 2 (that is, the frequency and duty cycle) for each individual output. From then on, only one command from the bus controller is required to turn each individual open-drain output on, off, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 200 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active LOW hardware reset pin ($\overline{\text{RESET}}$) and Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9552 allow eight devices to operate on the same bus.

2 Features

- 16 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.172 Hz and 44 Hz (5.82 seconds and 0.023 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active LOW reset input
- 16 open-drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

- Packages offered: SO24, TSSOP24, HVQFN24

3 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9552D	PCA9552D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9552PW	PCA9552	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9552BS	9552	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

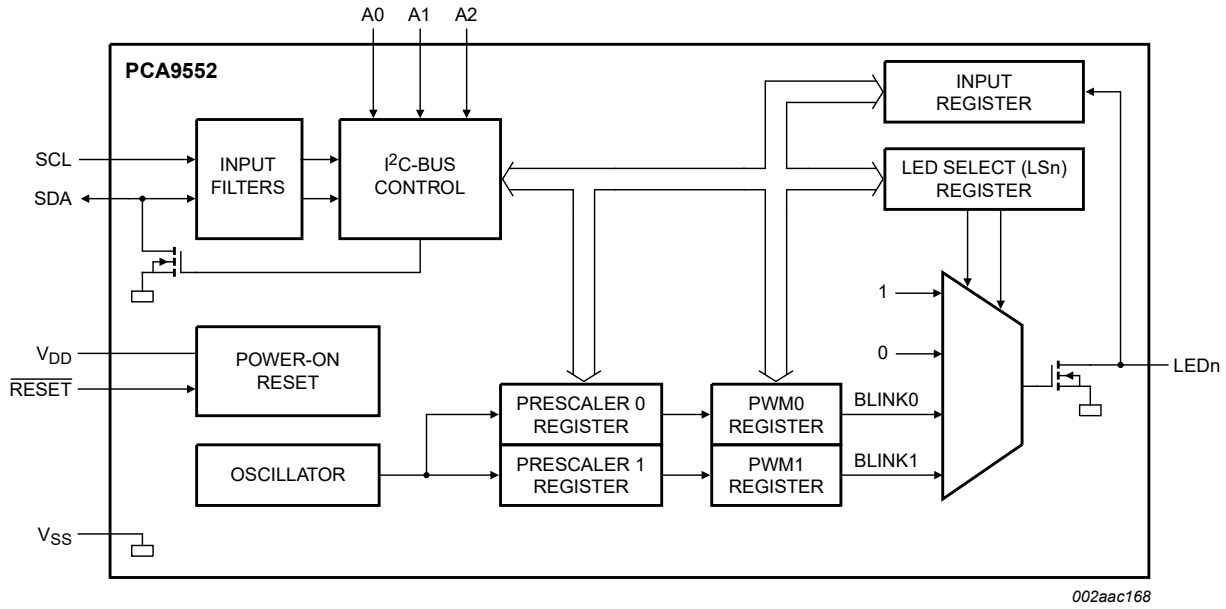
3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PCA9552D	PCA9552D,118	SO24	REEL 13" Q1 NDP	1000	T_{amb} = -40 °C to +85 °C
PCA9552PW	PCA9552PW,118	TSSOP24	REEL 13" Q1 NDP	2500	T_{amb} = -40 °C to +85 °C
PCA9552BS	PCA9552BS,118	HVQFN24	REEL 13" Q1 NDP	6000	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

4 Block diagram



Remark: Only one I/O shown for clarity.

Figure 1. Block diagram of PCA9552

5 Pinning information

5.1 Pinning

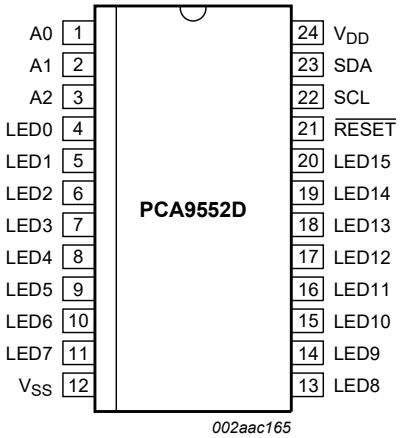


Figure 2. Pin configuration for SO24

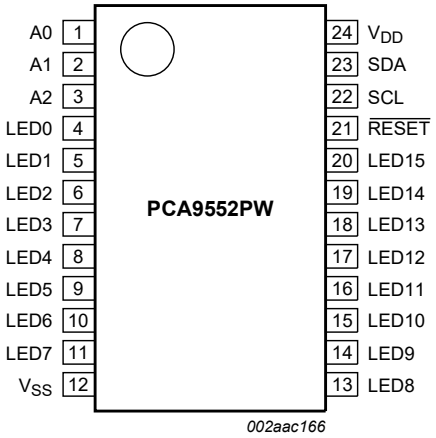


Figure 3. Pin configuration for TSSOP24

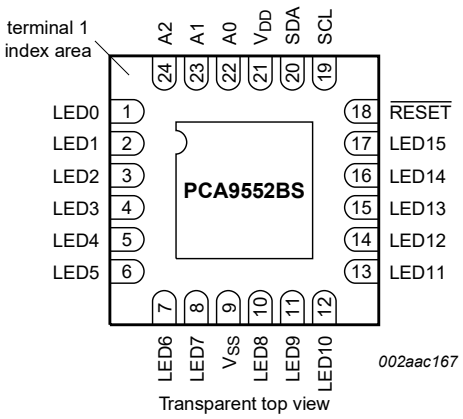


Figure 4. Pin configuration for HVQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO24, TSSOP24	HVQFN24	
A0	1	22	address input 0
A1	2	23	address input 1
A2	3	24	address input 2
LED0	4	1	LED driver 0
LED1	5	2	LED driver 1
LED2	6	3	LED driver 2
LED3	7	4	LED driver 3
LED4	8	5	LED driver 4
LED5	9	6	LED driver 5
LED6	10	7	LED driver 6
LED7	11	8	LED driver 7
V_{SS}	12	9[1]	ground supply
LED8	13	10	LED driver 8
LED9	14	11	LED driver 9
LED10	15	12	LED driver 10
LED11	16	13	LED driver 11
LED12	17	14	LED driver 12
LED13	18	15	LED driver 13
LED14	19	16	LED driver 14
LED15	20	17	LED driver 15
$\overline{\text{RESET}}$	21	18	active LOW reset input
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{DD}	24	21	supply voltage

[1] HVQFN package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6 Functional description

Refer to Figure 1.

6.1 Device address

Following a START condition, the bus controller must output the address of the target it is accessing. The address of the PCA9552 is shown in Figure 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

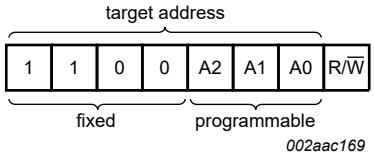
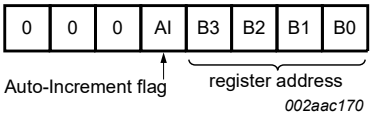


Figure 5. PCA9552 address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control Register

Following the successful acknowledgement of the target address, the bus controller will send a byte to the PCA9552, which will be stored in the Control Register. This register can be read and written via the I²C-bus.



Reset state: 00h

Figure 6. Control Register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the Auto-Increment flag (AI) is set, the four low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '0000' after the last register is accessed.

When the Auto-Increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B3 B2 B1 B0 ≠ 0000).

Only the 4 least significant bits are affected by the AI flag. Unused bits must be programmed with zeroes.

6.2.1 Control Register definition

Table 4. Register summary

B3	B2	B1	B0	Symbol	Access	Description
0	0	0	0	INPUT0	read only	input register 0
0	0	0	1	INPUT1	read only	input register 1
0	0	1	0	PSC0	read/write	frequency prescaler 0
0	0	1	1	PWM0	read/write	PWM register 0
0	1	0	0	PSC1	read/write	frequency prescaler 1
0	1	0	1	PWM1	read/write	PWM register 1
0	1	1	0	LS0	read/write	LED0 to LED3 selector
0	1	1	1	LS1	read/write	LED4 to LED7 selector
1	0	0	0	LS2	read/write	LED8 to LED11 selector
1	0	0	1	LS3	read/write	LED12 to LED15 selector

6.3 Register descriptions

6.3.1 INPUT0 - Input register 0

The Input register 0 reflects the state of the device pins (inputs LED0 to LED7). Writes to this register will be acknowledged but will have no effect.

Table 5. INPUT0 - input register 0 description

Bit	7	6	5	4	3	2	1	0
Symbol	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Default	X	X	X	X	X	X	X	X

Remark: The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to V_{DD}.

6.3.2 INPUT1 - Input register 1

The Input register 1 reflects the state of the device pins (inputs LED8 to LED15). Writes to this register will be acknowledged but will have no effect.

Table 6. INPUT1 - input register 1 description

Bit	7	6	5	4	3	2	1	0
Symbol	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8
Default	X	X	X	X	X	X	X	X

Remark: The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to V_{DD}.

6.3.3 PCS0 - Frequency Prescaler 0

PSC0 is used to program the period of the PWM output.

The period of BLINK0 = (PSC0 + 1) / 44.

Table 7. PSC0 - Frequency Prescaler 0 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PSC0[7]	PSC0[6]	PSC0[5]	PSC0[4]	PSC0[3]	PSC0[2]	PSC0[1]	PSC0[0]
Default	1	1	1	1	1	1	1	1

6.3.4 PWM0 - Pulse Width Modulation 0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

The duty cycle of BLINK0 = (256 - PWM0) / 256.

Table 8. PWM0 - Pulse Width Modulation 0 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PWM0 [7]	PWM0 [6]	PWM0 [5]	PWM0 [4]	PWM0 [3]	PWM0 [2]	PWM0 [1]	PWM0 [0]

Table 8. PWM0 - Pulse Width Modulation 0 register description...*continued*

Bit	7	6	5	4	3	2	1	0
Default	1	0	0	0	0	0	0	0

6.3.5 PCS1 - Frequency Prescaler 1

PSC1 is used to program the period of the PWM output.

The period of BLINK1 = (PSC1 + 1) / 44.

Table 9. PSC1 - Frequency Prescaler 1 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PSC1[7]	PSC1[6]	PSC1[5]	PSC1[4]	PSC1[3]	PSC1[2]	PSC1[1]	PSC1[0]
Default	1	1	1	1	1	1	1	1

6.3.6 PWM1 - Pulse Width Modulation 1

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

The duty cycle of BLINK1 = (256 - PWM1) / 256.

Table 10. PWM1 - Pulse Width Modulation 1 register description

Bit	7	6	5	4	3	2	1	0
Symbol	PWM1 [7]	PWM1 [6]	PWM1 [5]	PWM1 [4]	PWM1 [3]	PWM1 [2]	PWM1 [1]	PWM1 [0]
Default	1	0	0	0	0	0	0	0

6.3.7 LS0 to LS3 - LED selector registers

The LSn LED select registers determine the source of the LED data.

00 = output is set LOW (LED on)
01 = output is set high-impedance (LED off; default)
10 = output blinks at PWM0 rate
11 = output blinks at PWM1 rate

Table 11. LS0 to LS3 - LED selector registers bit description

*Legend: * default value*

Register	Bit	Value	Description
LS0 - LED0 to LED3 selector			
LS0	7:6	01*	LED3 selected
	5:4	01*	LED2 selected
	3:2	01*	LED1 selected
	1:0	01*	LED0 selected
LS1 - LED4 to LED7 selector			
LS1	7:6	01*	LED7 selected

Table 11. LS0 to LS3 - LED selector registers bit description...*continued*

*Legend: * default value*

Register	Bit	Value	Description
	5:4	01*	LED6 selected
	3:2	01*	LED5 selected
	1:0	01*	LED4 selected
LS2 - LED8 to LED11 selector			
LS2	7:6	01*	LED11 selected
	5:4	01*	LED10 selected
	3:2	01*	LED9 selected
	1:0	01*	LED8 selected
LS3 - LED12 to LED15 selector			
LS3	7:6	01*	LED15 selected
	5:4	01*	LED14 selected
	3:2	01*	LED13 selected
	1:0	01*	LED12 selected

6.4 Pins used as GPIOs

LED pins not used to control LEDs can be used as general purpose I/Os (GPIOs).

For use as input, set LEDn to high-impedance (01) and then read the pin state via the input register.

For use as output, connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the 'LED selector' register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

6.5 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9552 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9552 registers are initialized to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

6.6 External RESET

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9552 registers and I²C-bus state machine will be held in their default states until the $\overline{\text{RESET}}$ input is once again HIGH.

This input requires a pull-up resistor to V_{DD} if no active connection is used.

7 Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

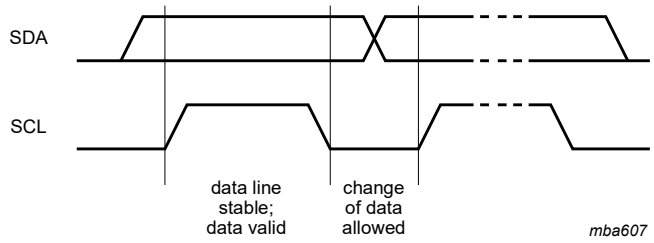


Figure 7. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8.)

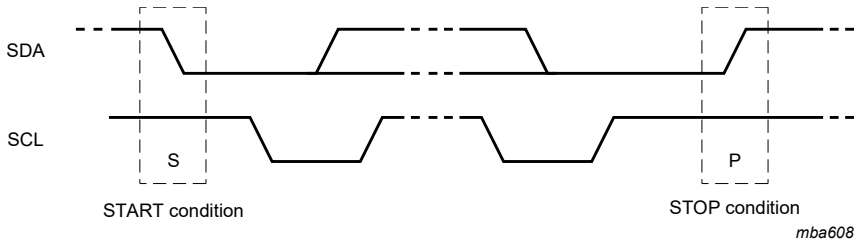


Figure 8. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'controller' and the devices which are controlled by the controller are the 'targets' (see Figure 9).

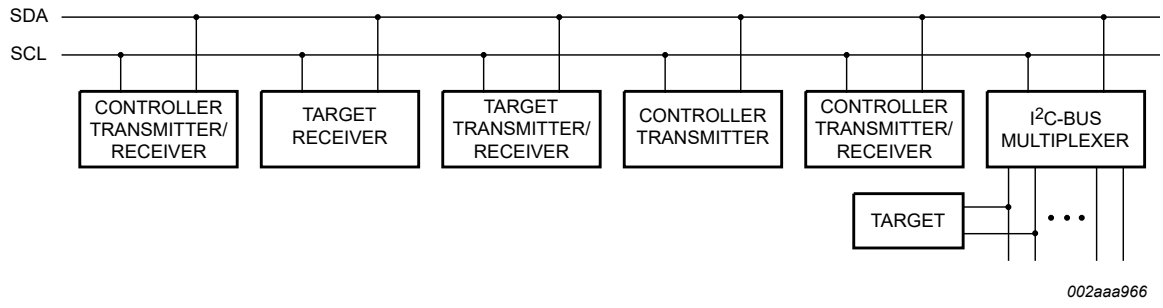


Figure 9. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra acknowledge related clock pulse.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

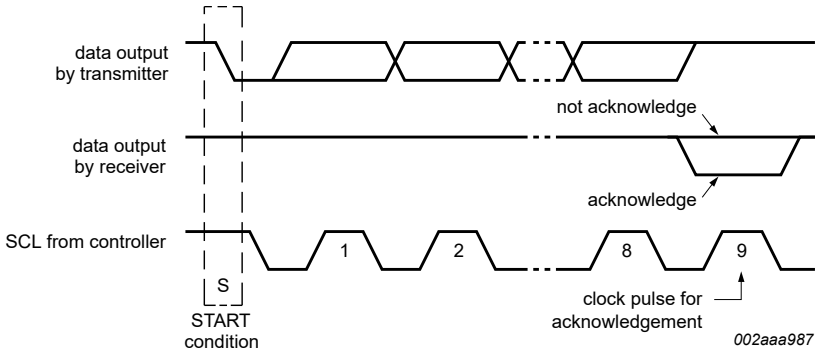


Figure 10. Acknowledgement on the I²C-bus

7.4 Bus transactions

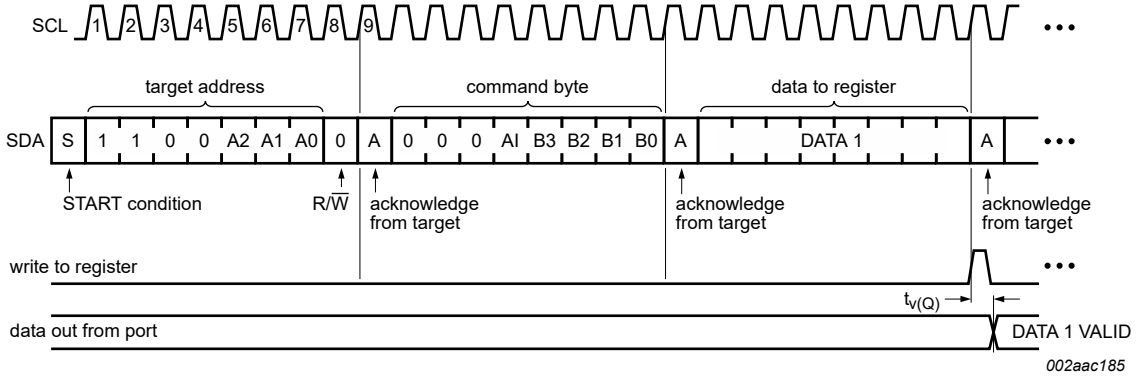


Figure 11. Write to register

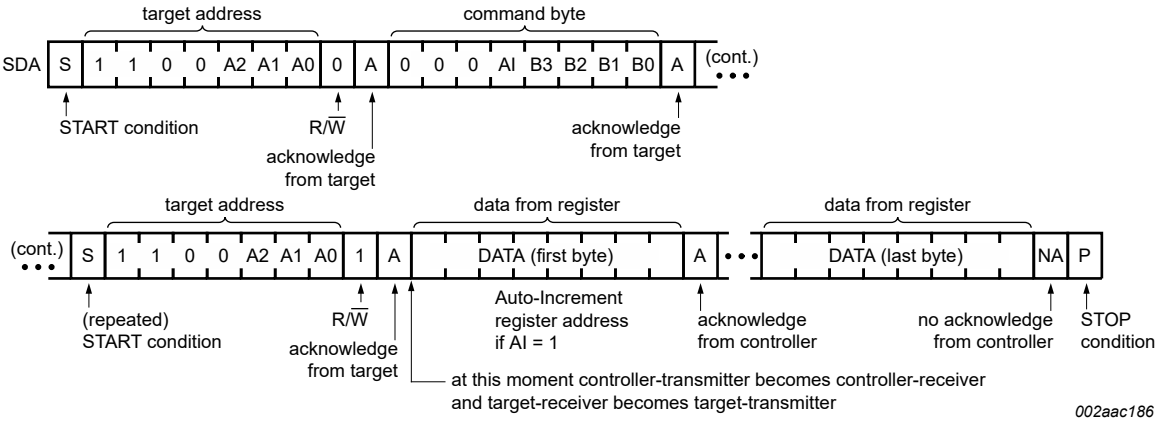
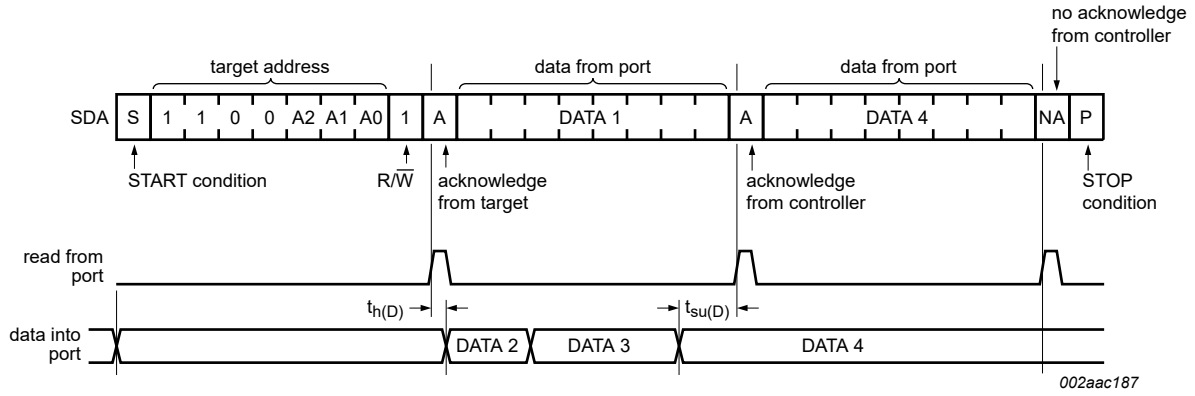


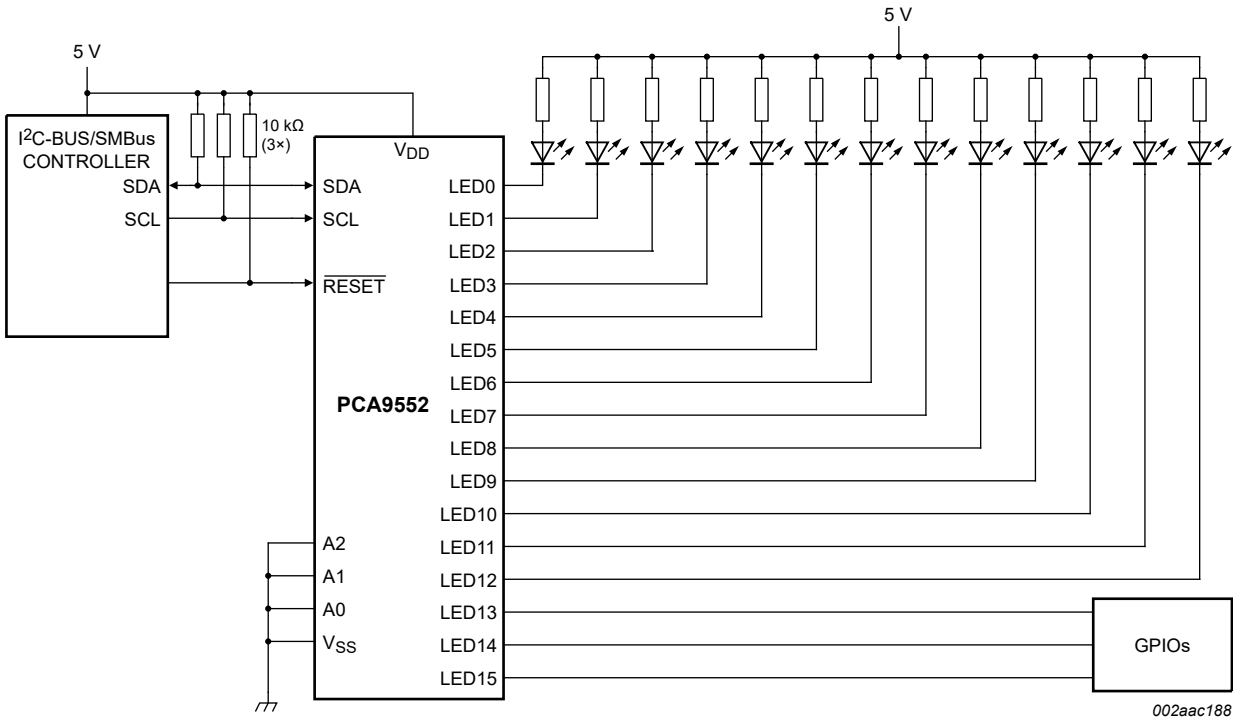
Figure 12. Read from register



Remark: This figure assumes the command byte has previously been programmed with 00h.

Figure 13. Read Input Port register

8 Application design-in information



LED0 to LED12 are used as LED drivers.

LED13 to LED15 are used as regular GPIOs.

Figure 14. Typical application

8.1 Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 15. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD} and is specified as ΔI_{stb} in Table 14.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 15 shows a high value resistor in parallel with the LED. Figure 16 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the input/output V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

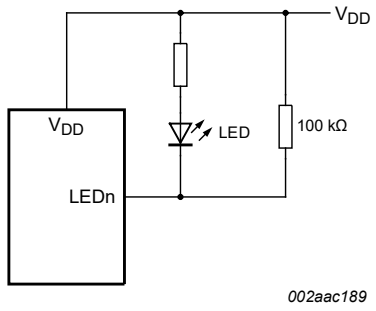


Figure 15. High value resistor in parallel with the LED

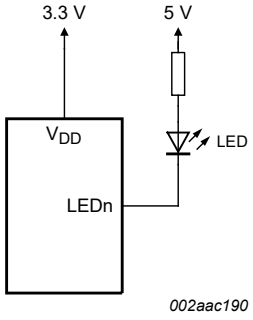


Figure 16. Device supplied by a lower voltage

8.2 Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50 % duty cycle. LED6 and LED7 will be set to blink at 4 Hz and at a 25 % duty cycle. LED8 to LED15 will be set to off.

Table 12. Programming PCA9552

Program sequence	I²C-bus
START	S
PCA9552 address with A0 to A2 = LOW	C0h
PSC0 subaddress + Auto-Increment	12h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{PSC0+1}{44}$ PSC0 = 43	2Bh
Set PWM0 duty cycle to 50 %: $\frac{256-PWM0}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to achieve a period of 0.25 seconds: $\text{Blink period} = 0.25 = \frac{PSC1+1}{44}$ PSC1 = 10	0Ah
Set PWM1 output duty cycle to 25 %: $\frac{256-PWM1}{256} = 0.25$ PWM1 = 192	C0h
Set LED0 to LED3 on	00h
Set LED4 and LED5 to PWM0, and LED6 or LED7 to PWM1	FAh
Set LED8 to LED11 off	55h
Set LED12 to LED15 off	55h
STOP	P

9 Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin	LEDn used as an I/O		V_{SS} - 0.5	5.5	V
$I_{O(LEDn)}$	output current on pin LEDn	LEDn used as an I/O		-	± 25	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	400	mW
T_{stg}	storage temperature			-65	+150	° C
T_{amb}	ambient temperature	operating		-40	+85	° C

10 Static characteristics

Table 14. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 ° C to +85 ° C; unless otherwise specified.

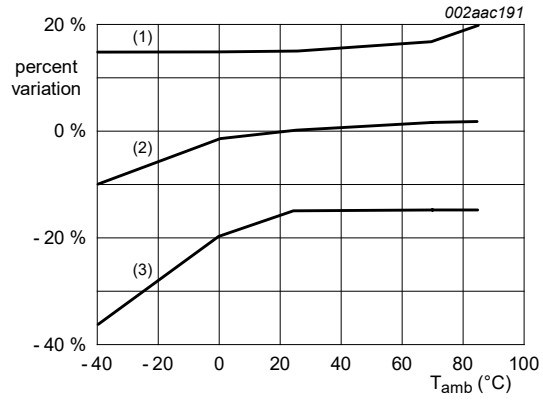
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		-	350	550	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz		-	2.1	5.0	µA
ΔI_{stb}	additional standby current	Standby mode; V_{DD} = 5.5 V; every LED I/O at V_I = 4.3 V; f_{SCL} = 0 kHz		-	-	2	mA
V_{POR}	power-on reset voltage[2]	V_{DD} = 3.3 V; no load; V_I = V_{DD} or V_{SS}		-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			-0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	6.5	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}		-1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	4.4	5	pF
I/Os							
V_{IL}	LOW-level input voltage			-0.5	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V	[3]	9	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V	[3]	12	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V	[3]	15	-	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	[3]	15	-	-	mA

Table 14. Static characteristics...*continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 ° C to +85 ° C; unless otherwise specified.

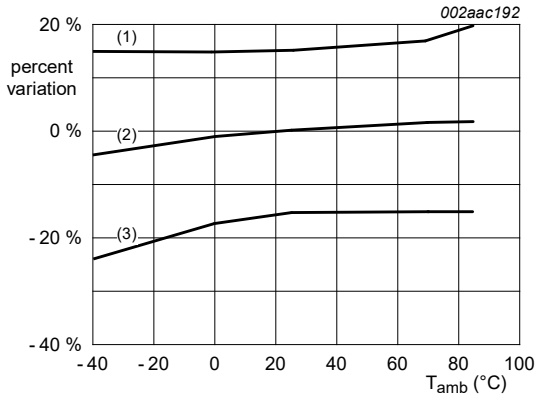
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	[3]	20	-	-	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V	[3]	25	-	-	mA
I_{LI}	input leakage current	V_{DD} = 3.6 V; V_I = 0 V or V_{DD}		-1	-	+1	µA
C_{io}	input/output capacitance			-	2.6	5	pF
Select inputs A0, A1, A2; $\overline{\text{RESET}}$							
V_{IL}	LOW-level input voltage			-0.5	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{LI}	input leakage current			-1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	2.3	5	pF

[1] All typical values at 3.3 V and 25 °C.
[2] V_{DD} must be lowered to 0.2 V in order to reset part.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal ([LED0 to LED7] and [LED8 to LED15]) must be limited to a maximum current of 100 mA for a device total of 200 mA.



1. maximum
2. average
3. minimum

Figure 17. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V



1. maximum
2. average
3. minimum

Figure 18. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

11 Dynamic characteristics

Table 15. Dynamic characteristics

Symbol	Parameter	Conditions		Standard mode I²C-bus		Fast mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs

Table 15. Dynamic characteristics...*continued*

Symbol	Parameter	Conditions		Standard mode I²C-bus		Fast mode I²C-bus		Unit
				Min	Max	Min	Max	
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time		[1]	-	600	-	600	ns
$t_{VD;DAT}$	data valid time	LOW-level	[2]	-	600	-	600	ns
		HIGH-level	[2]	-	1500	-	600	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$[3]	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$[3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time			-	250	-	250	ns
$t_{su(D)}$	data input setup time			100	-	100	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs
Reset								
$t_{w(rst)}$	reset pulse width			10	-	10	-	ns
$t_{rec(rst)}$	reset recovery time			0	-	0	-	ns
t_{rst}	reset time		[4][5]	400	-	400	-	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3] C_b = total capacitance of one bus line in pF.
[4] Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
[5] Upon reset, the full delay will be the sum of t_{rst} and the RC time constant of the SDA bus.

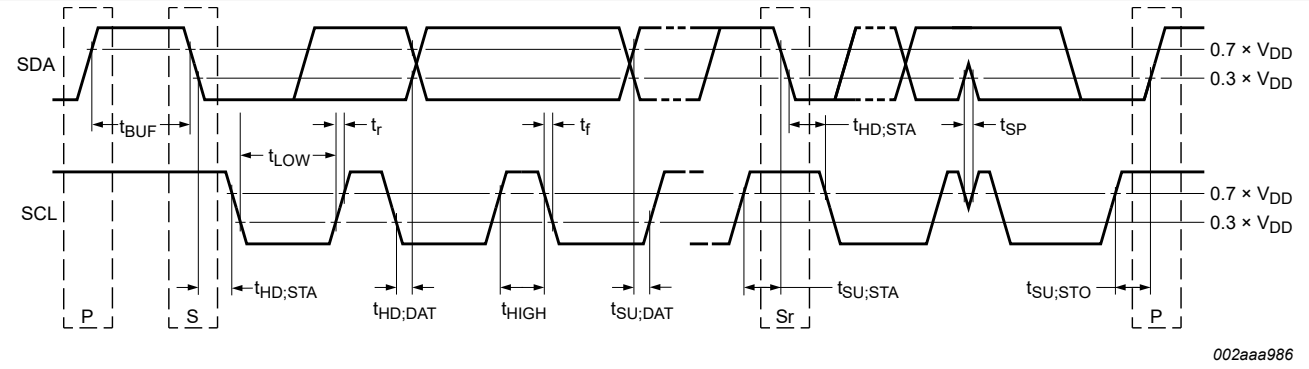
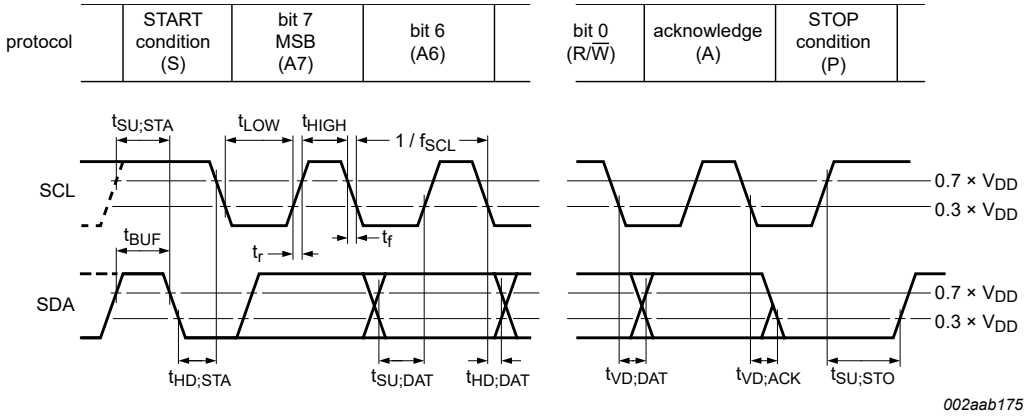


Figure 19. Definition of timing on the I²C-bus



Rise and fall times refer to V_{IL} and V_{IH}.

Figure 20. I²C-bus timing diagram

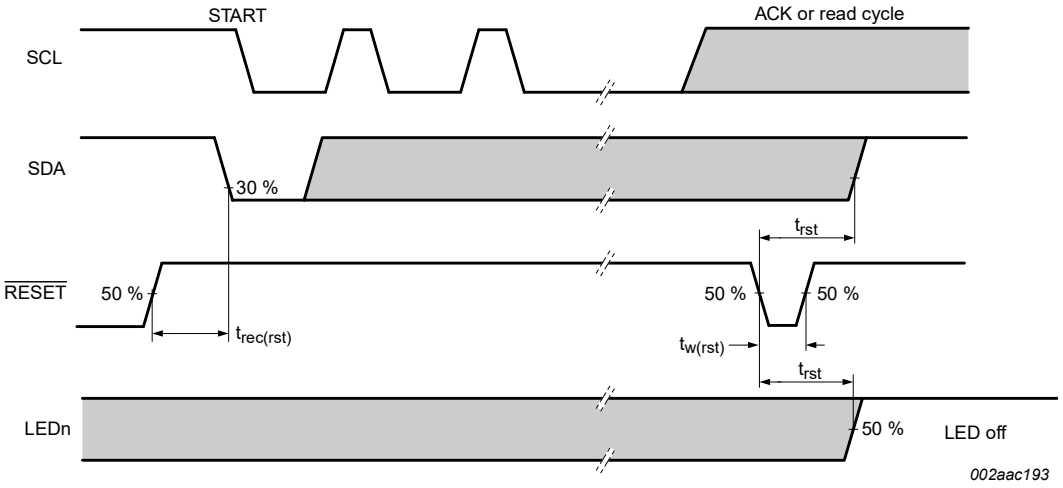
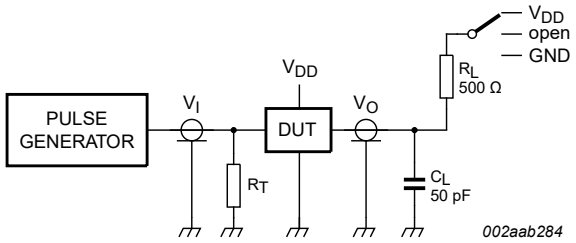


Figure 21. Reset timing

12 Test information



R_L = load resistor for LEDn. R_L for SDA and SCL > 1 kΩ (3 mA or less current)

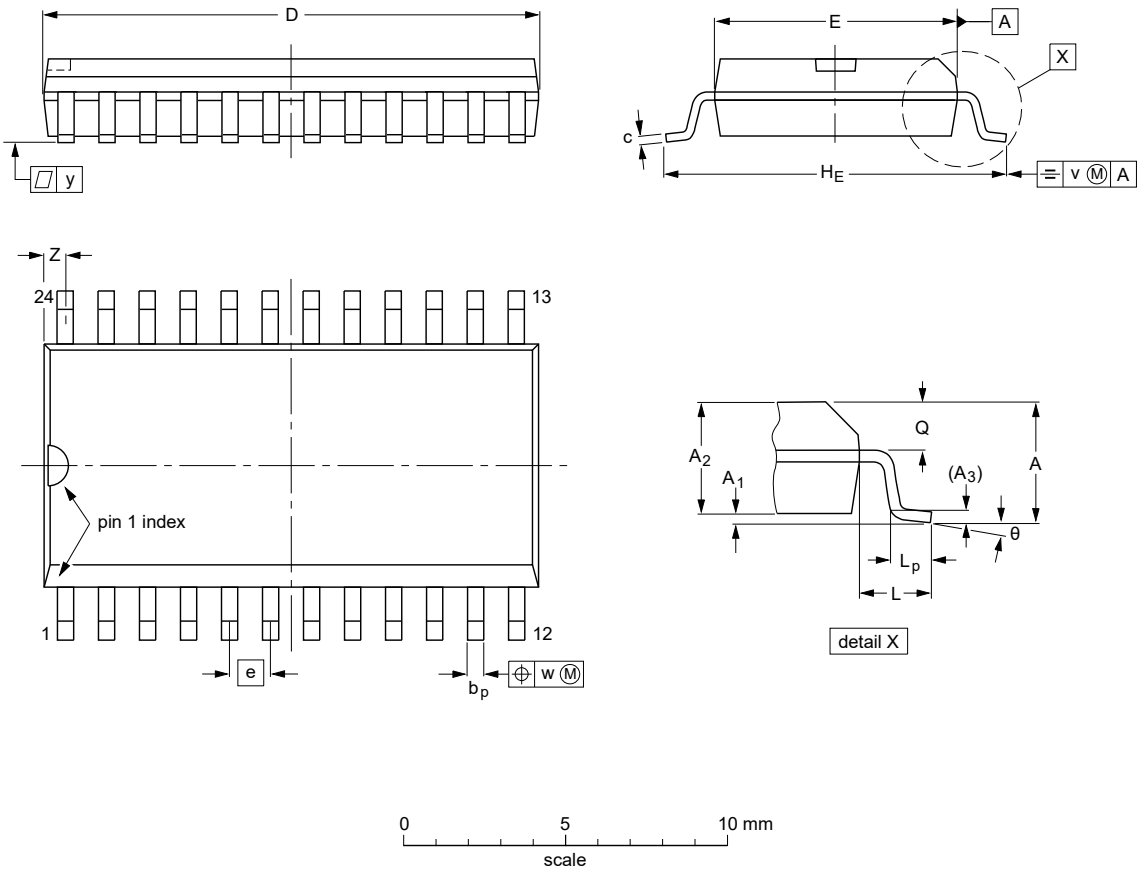
C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Figure 22. Test circuitry for switching times

13 Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

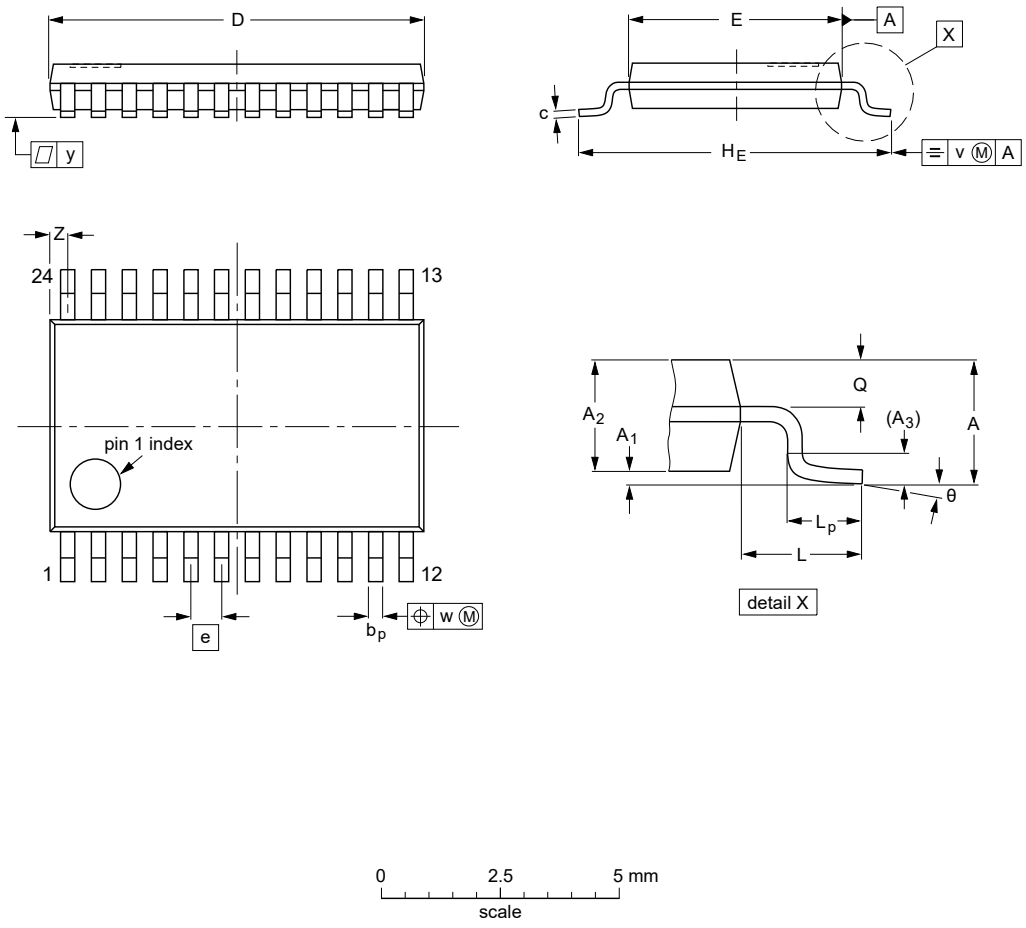
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Figure 23. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

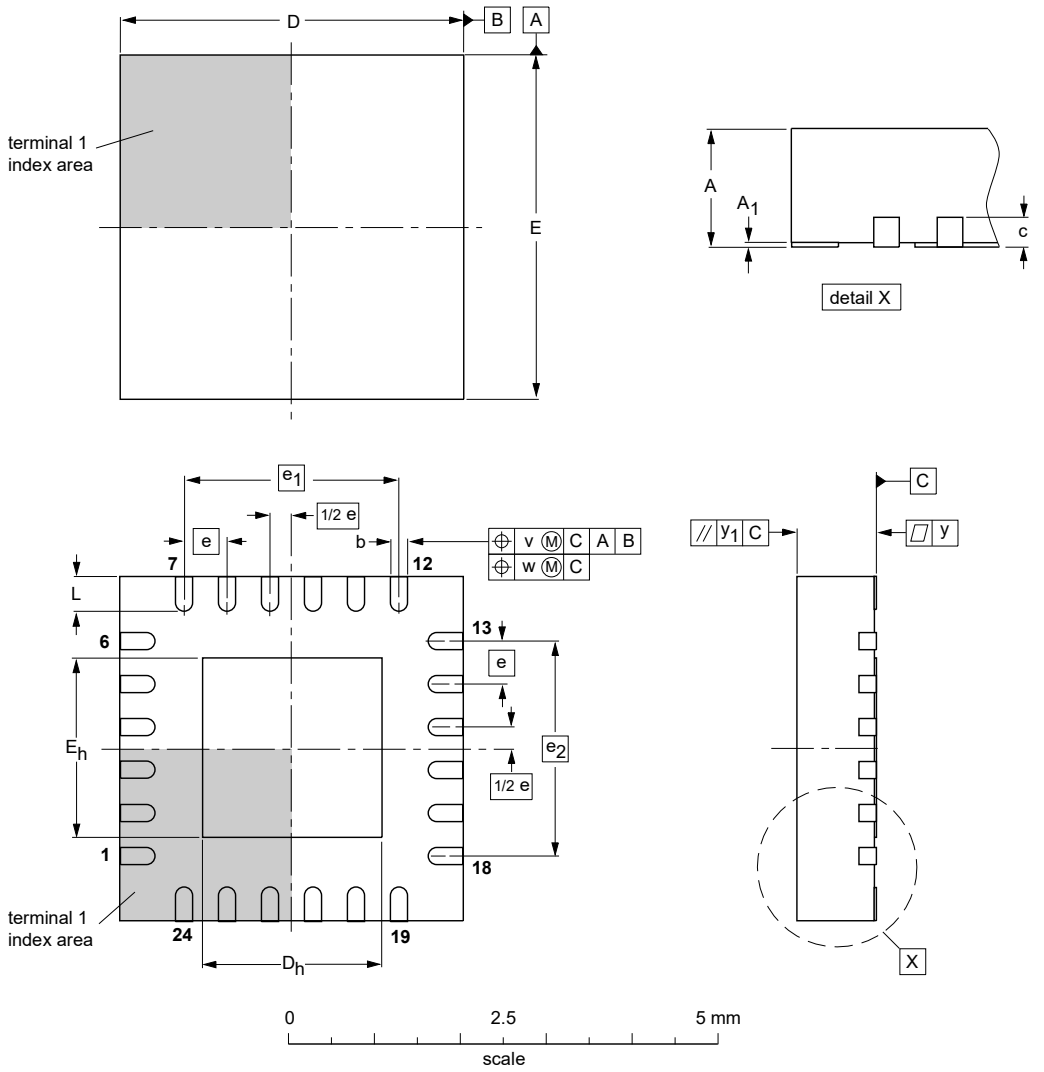
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Figure 24. Package outline SOT355-1 (TSSOP24)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Figure 25. Package outline SOT616-1 (HVQFN24)

14 Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

15 Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and Table 17

Table 16. SnPb eutectic process (from J-STD-020D)

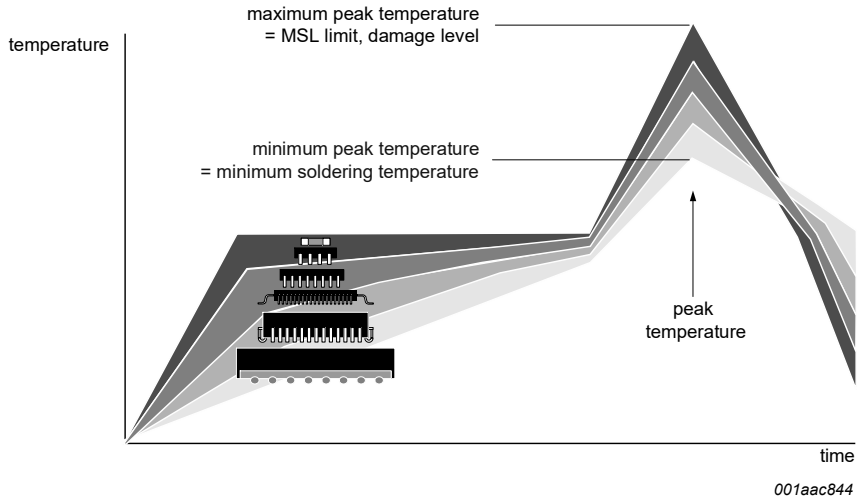
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



MSL: Moisture Sensitivity Level

Figure 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DSP	Digital Signal Processor
ESD	ElectroStatic Discharge
HBM	Human Body Model
GPIO	General Purpose Input/Output
IC	Integrated Circuit
I^2C-bus	Inter IC bus
LED	Light Emitting Diode
MCU	Microcontroller
MM	Machine Model
MPU	Microprocessor
POR	Power-On Reset
PWM	Pulse Width Modulation
SMBus	System Management Bus

17 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9552 v5.1	20230525	Product data sheet	-	PCA9552_5
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of NXP Semiconductors. • Replaced deprecated terms 'master' and 'slave' with 'controller' and 'target' respectively to comply with NXPs inclusive language policy			
PCA9552_5	20060309	Product data sheet	-	PCA9552_4
PCA9552_4	20041001	Product data sheet	-	PCA9552_3
PCA9552_3	20030502	Product data	853-2374 29857 of 2003 Apr 24	PCA9552_2
PCA9552_2	20030224	Product data	853-2374 29331 of 2002 Dec 20	PCA9552_1
PCA9552_1	20020927	Product data	853-2374 28878 of 2002 Sep 09	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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