



**THE DATASHEET OF  
PCA9539PWR**



# PCA9539 Remote 16-Bit I<sup>2</sup>C and SMBus Low-Power I/O Expander With Interrupt Output, Reset, and Configuration Registers

## 1 Features

- Low Standby-Current Consumption of 1  $\mu$ A Max
- I<sup>2</sup>C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Active-Low Reset Input
- 5-V Tolerant I/O Ports
- Compatible With Most Microcontrollers
- 400-kHz Fast I<sup>2</sup>C Bus
- Polarity Inversion Register
- Address by Two Hardware Address Pins for Use of up to Four Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Description

This 16-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.3-V to 5.5-V V<sub>CC</sub> operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

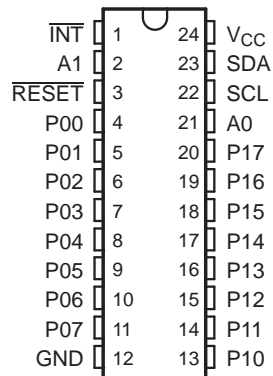
The PCA9539 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

### Device Information<sup>(1)</sup>

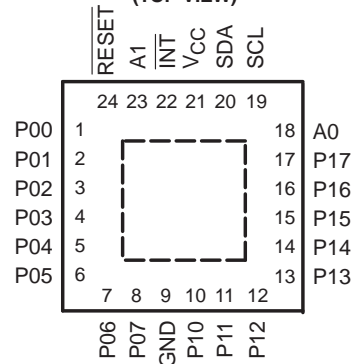
PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9539	SSOP (24)	8.20 mm x 5.30 mm
	TVSOP (24)	5.00 mm x 4.40 mm
	SOIC (24)	15.40 mm x 7.50 mm
	TSSOP (24)	7.80 mm x 4.40 mm
	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RGE PACKAGE  
(TOP VIEW)



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Description</b> ..... 1 <b>3 Revision History</b> ..... 2 <b>4 Description (Continued)</b> ..... 3 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 5 6.1 Absolute Maximum Ratings ..... 5 6.2 Handling Ratings..... 5 6.3 Recommended Operating Conditions..... 5 6.4 Electrical Characteristics..... 6 6.5 I <sup>2</sup> C Interface Timing Requirements..... 7 6.6 $\overline{\text{RESET}}$ Timing Requirements..... 7 6.7 Switching Characteristics ..... 7 6.8 Typical Characteristics..... 8 <b>7 Parameter Measurement Information</b> ..... 10	<b>8 Detailed Description</b> ..... 14 8.1 Functional Block Diagram ..... 14 8.2 Device Functional Modes..... 16 8.3 Programming..... 17 <b>9 Application And Implementation</b> ..... 24 9.1 Typical Application ..... 24 <b>10 Power Supply Recommendations</b> ..... 26 10.1 Power-On Reset Requirements ..... 26 10.2 Power-On Reset Errata..... 27 <b>11 Device and Documentation Support</b> ..... 28 11.1 Trademarks ..... 28 11.2 Electrostatic Discharge Caution..... 28 11.3 Glossary ..... 28 <b>12 Mechanical, Packaging, and Orderable Information</b> ..... 28
---	---

### 3 Revision History

Changes from Revision F (January 2011) to Revision G	Page
• Added $\overline{\text{RESET}}$ Errata section. ....	16
• Added Interrupt Errata section.....	17
• Power-On Reset Errata section.....	27

## 4 Description (Continued)

The system master can reset the PCA9539 in the event of a time-out or other improper operation by asserting a low in the  $\overline{\text{RESET}}$  input. The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine. Asserting  $\overline{\text{RESET}}$  causes the same reset/initialization to occur without de-powering the part.

The PCA9539 open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the PCA9539 can remain a simple slave device.

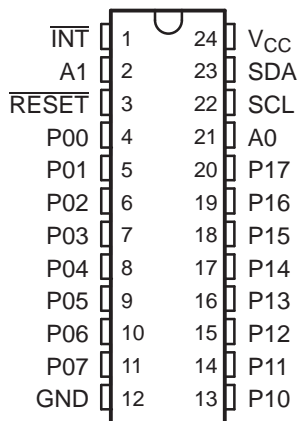
The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The PCA9539 is identical to the PCA9555, except for the removal of the internal I/O pullup resistor, which greatly reduces power consumption when the I/Os are held low, replacement of A2 with  $\overline{\text{RESET}}$ , and a different address range.

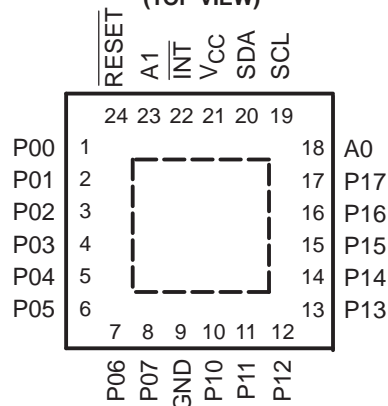
Two hardware pins (A0 and A1) are used to program and vary the fixed I<sup>2</sup>C address and allow up to four devices to share the same I<sup>2</sup>C bus or SMBus.

## 5 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RGE PACKAGE  
(TOP VIEW)



### Pin Functions

NAME	PIN		DESCRIPTION
	NO.		
	SOIC (DW), SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	QFN (RGE)	
$\overline{\text{INT}}$	1	22	Interrupt output. Connect to $V_{CC}$ through a pullup resistor.
A1	2	23	Address input. Connect directly to $V_{CC}$ or ground.
$\overline{\text{RESET}}$	3	24	Active-low reset input. Connect to $V_{CC}$ through a pullup resistor if no active connection is used.
P00	4	1	P-port input/output. Push-pull design structure.
P01	5	2	P-port input/output. Push-pull design structure.
P02	6	3	P-port input/output. Push-pull design structure.
P03	7	4	P-port input/output. Push-pull design structure.
P04	8	5	P-port input/output. Push-pull design structure.
P05	9	6	P-port input/output. Push-pull design structure.
P06	10	7	P-port input/output. Push-pull design structure.
P07	11	8	P-port input/output. Push-pull design structure.
GND	12	9	Ground
P10	13	10	P-port input/output. Push-pull design structure.
P11	14	11	P-port input/output. Push-pull design structure.
P12	15	12	P-port input/output. Push-pull design structure.
P13	16	13	P-port input/output. Push-pull design structure.
P14	17	14	P-port input/output. Push-pull design structure.
P15	18	15	P-port input/output. Push-pull design structure.
P16	19	16	P-port input/output. Push-pull design structure.
P17	20	17	P-port input/output. Push-pull design structure.
A0	21	18	Address input. Connect directly to $V_{CC}$ or ground.
SCL	22	19	Serial clock bus. Connect to $V_{CC}$ through a pullup resistor.
SDA	23	20	Serial data bus. Connect to $V_{CC}$ through a pullup resistor.
$V_{CC}$	24	21	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-20	mA
I <sub>I<sub>OK</sub></sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-50	mA
I <sub>CC</sub>	Continuous current through GND		-250	mA
	Continuous current through V <sub>CC</sub>		160	
θ <sub>JA</sub>	Package thermal impedance, junction to free air <sup>(3)</sup>	DB package	63	°C/W
		DBQ package	61	
		DGV package	86	
		DW package	46	
		PW package	88	
		RGE package	45	
θ <sub>JP</sub>	Package thermal impedance, junction to pad	RGE package	1.5	°C/W

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### 6.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	2.3	5.5	V	
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	5.5	V
		A0, A1, $\overline{\text{RESET}}$ , P07–P00, P17–P10	0.7 × V <sub>CC</sub>	5.5	
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>	V
		A0, A1, $\overline{\text{RESET}}$ , P07–P00, P17–P10	-0.5	0.3 × V <sub>CC</sub>	
I <sub>OH</sub>	High-level output current	P07–P00, P17–P10	-10	mA	
I <sub>OL</sub>	Low-level output current	P07–P00, P17–P00	25	mA	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.3 V to 5.5 V	-1.2			V
V <sub>POR</sub>	Power-on reset voltage	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	V <sub>POR</sub>		1.5	1.65	V
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = -8 mA	2.3 V		1.8		V
			3 V		2.6		
			4.75 V		4.1		
		I <sub>OH</sub> = -10 mA	2.3 V		1.7		
			3 V		2.5		
			4.75 V		4		
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	2.3 V to 5.5 V		3		mA
	P port <sup>(3)</sup>	V <sub>OL</sub> = 0.5 V			8	20	
		V <sub>OL</sub> = 0.7 V			10	24	
	$\overline{\text{INT}}$	V <sub>OL</sub> = 0.4 V			3		
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V			±1	μA
	A0, A1, $\overline{\text{RESET}}$					±1	
I <sub>IH</sub>	P port	V <sub>I</sub> = V <sub>CC</sub>	2.3 V to 5.5 V			1	μA
I <sub>IL</sub>	P port	V <sub>I</sub> = GND	2.3 V to 5.5 V			-1	μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz	5.5 V		100	200	μA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	V <sub>I</sub> = GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz	5.5 V		0.5	1	
			3.6 V		0.4	0.9	
			2.7 V		0.25	0.8	
ΔI <sub>CC</sub>	Additional current in standby mode	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.3 V to 5.5 V			200	μA
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		3	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		3	7	pF
	P port				3.7	9.5	

 (1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.

(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

## 6.5 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 13](#))

		MIN	MAX	UNIT	
$f_{scl}$	I <sup>2</sup> C clock frequency	0	400	kHz	
$t_{sch}$	I <sup>2</sup> C clock high time	0.6		μs	
$t_{scl}$	I <sup>2</sup> C clock low time	1.3		μs	
$t_{sp}$	I <sup>2</sup> C spike time		50	ns	
$t_{sds}$	I <sup>2</sup> C serial-data setup time	100		ns	
$t_{sdh}$	I <sup>2</sup> C serial-data hold time	0		ns	
$t_{icr}$	I <sup>2</sup> C input rise time	$20 + 0.1C_b^{(1)}$	300	ns	
$t_{icf}$	I <sup>2</sup> C input fall time	$20 + 0.1C_b^{(1)}$	300	ns	
$t_{ocf}$	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b^{(1)}$	300	ns
$t_{buf}$	I <sup>2</sup> C bus free time between Stop and Start	1.3		μs	
$t_{sts}$	I <sup>2</sup> C Start or repeated Start condition setup	0.6		μs	
$t_{sth}$	I <sup>2</sup> C Start or repeated Start condition hold	0.6		μs	
$t_{sps}$	I <sup>2</sup> C Stop condition setup	0.6		μs	
$t_{vd(data)}$	Valid-data time	SCL low to SDA output valid	50	ns	
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	μs
$C_b$	I <sup>2</sup> C bus capacitive load		400	pF	

(1)  $C_b$  = total capacitance of one bus line in pF

## 6.6 RESET Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 16](#))

		MIN	MAX	UNIT
$t_W$	Reset pulse duration	6		ns
$t_{REC}$	Reset recovery time	0		ns
$t_{RESET}$	Time to reset	400		ns

## 6.7 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 14](#) and [Figure 15](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{iv}$	P port	$\overline{INT}$		4	μs
$t_{ir}$	SCL	$\overline{INT}$		4	μs
$t_{pv}$	SCL	P port		200	ns
$t_{ps}$	P port	SCL	150		ns
$t_{ph}$	P port	SCL	1		μs

## 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

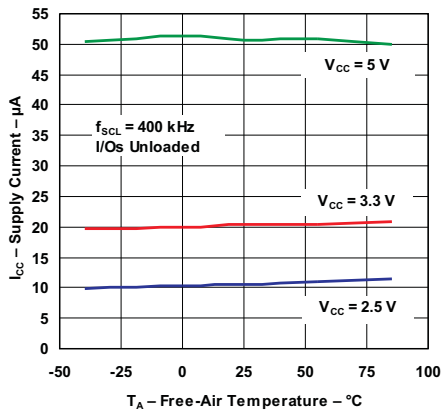


Figure 1. Supply Current vs Temperature

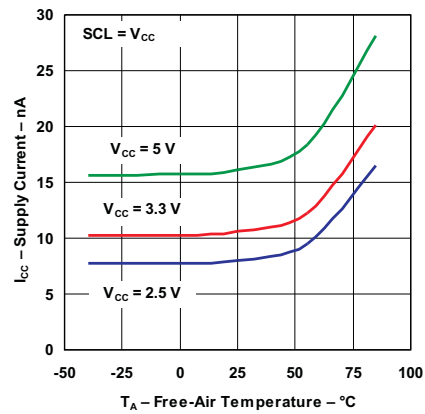


Figure 2. Standby Supply Current vs Temperature

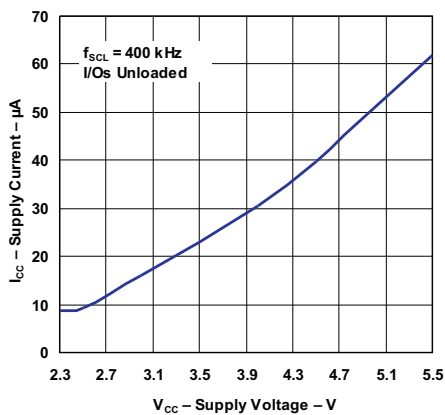


Figure 3. Supply Current vs Supply Voltage

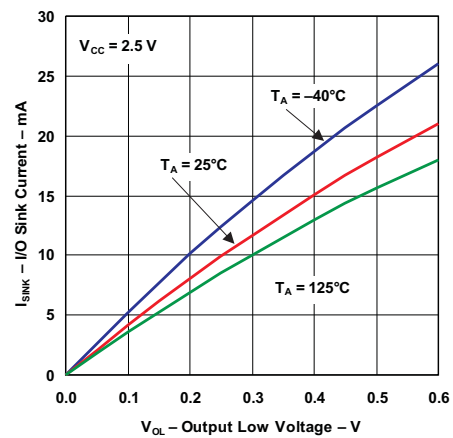


Figure 4. I/O Sink Current vs Output Low Voltage

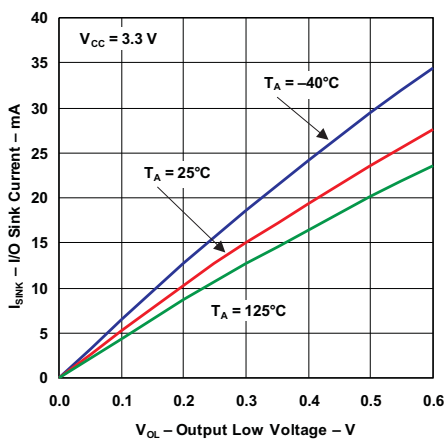


Figure 5. I/O Sink Current vs Output Low Voltage

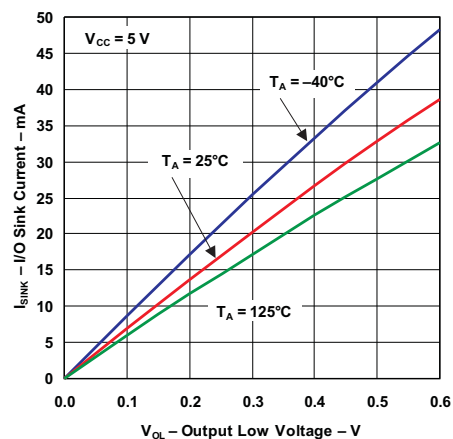


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise noted)

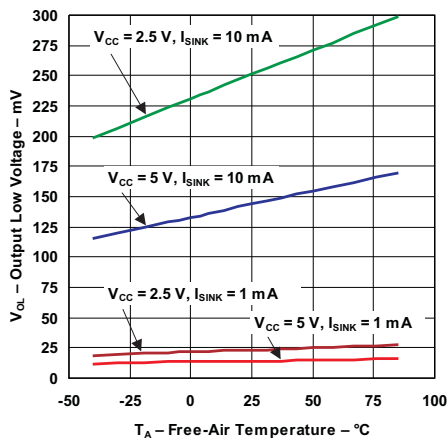


Figure 7. I/O Output Low Voltage vs Temperature

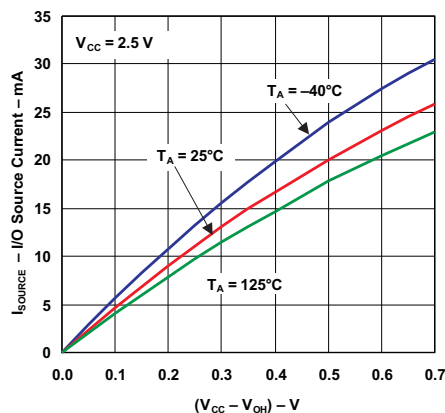


Figure 8. I/O Source Current vs Output High Voltage

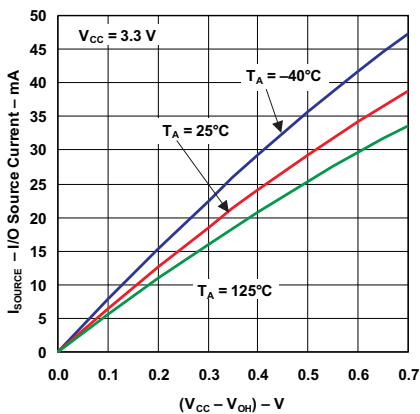


Figure 9. I/O Source Current vs Output High Voltage

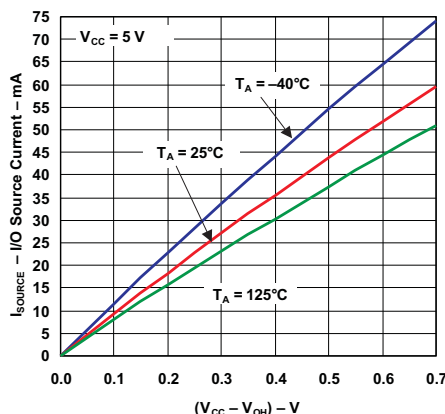


Figure 10. I/O Source Current vs Output High Voltage

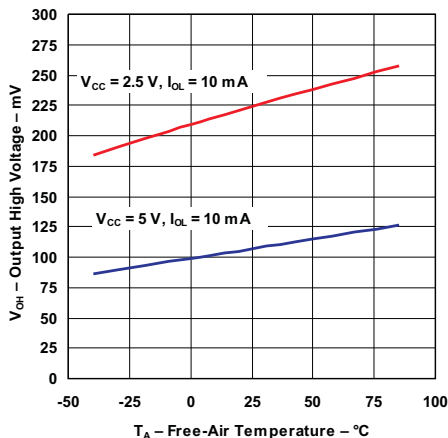


Figure 11. I/O High Voltage vs Temperature

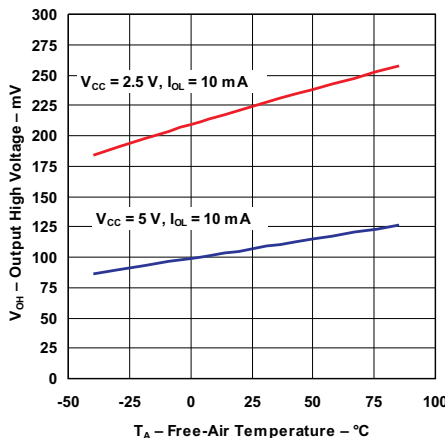
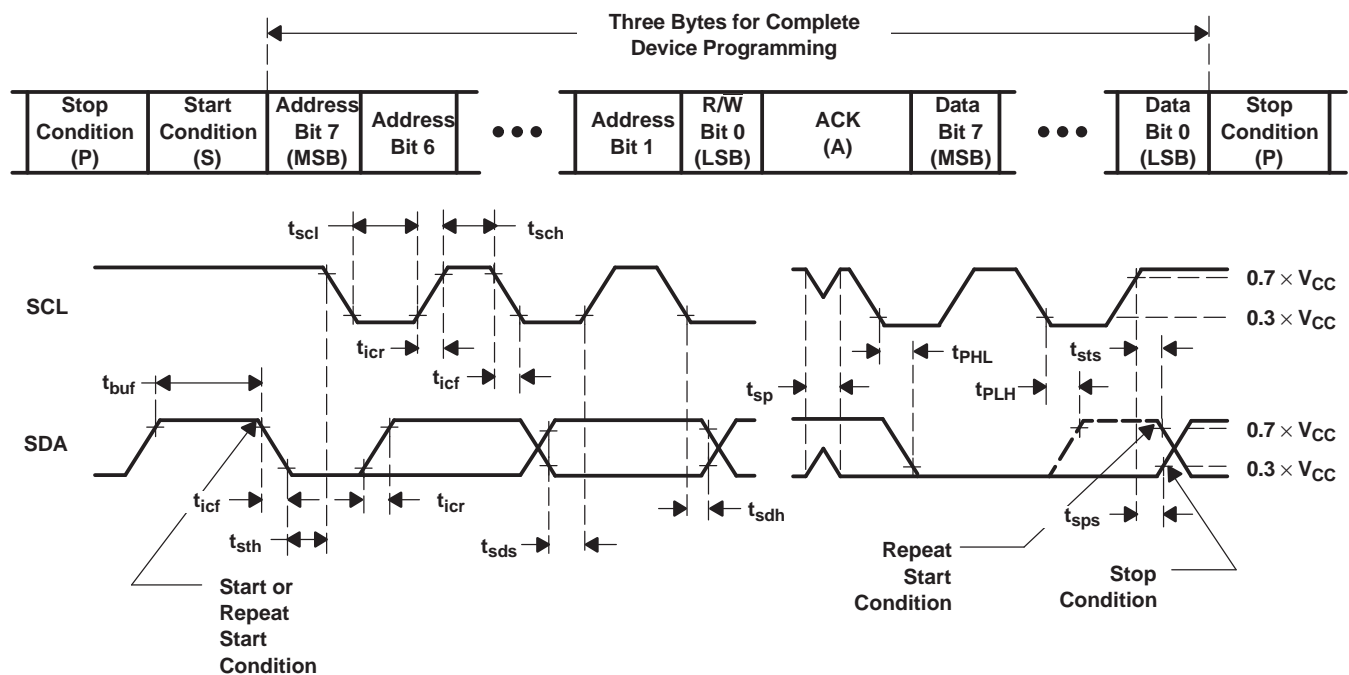


Figure 12. Output High Voltage vs Supply Voltage

## 7 Parameter Measurement Information



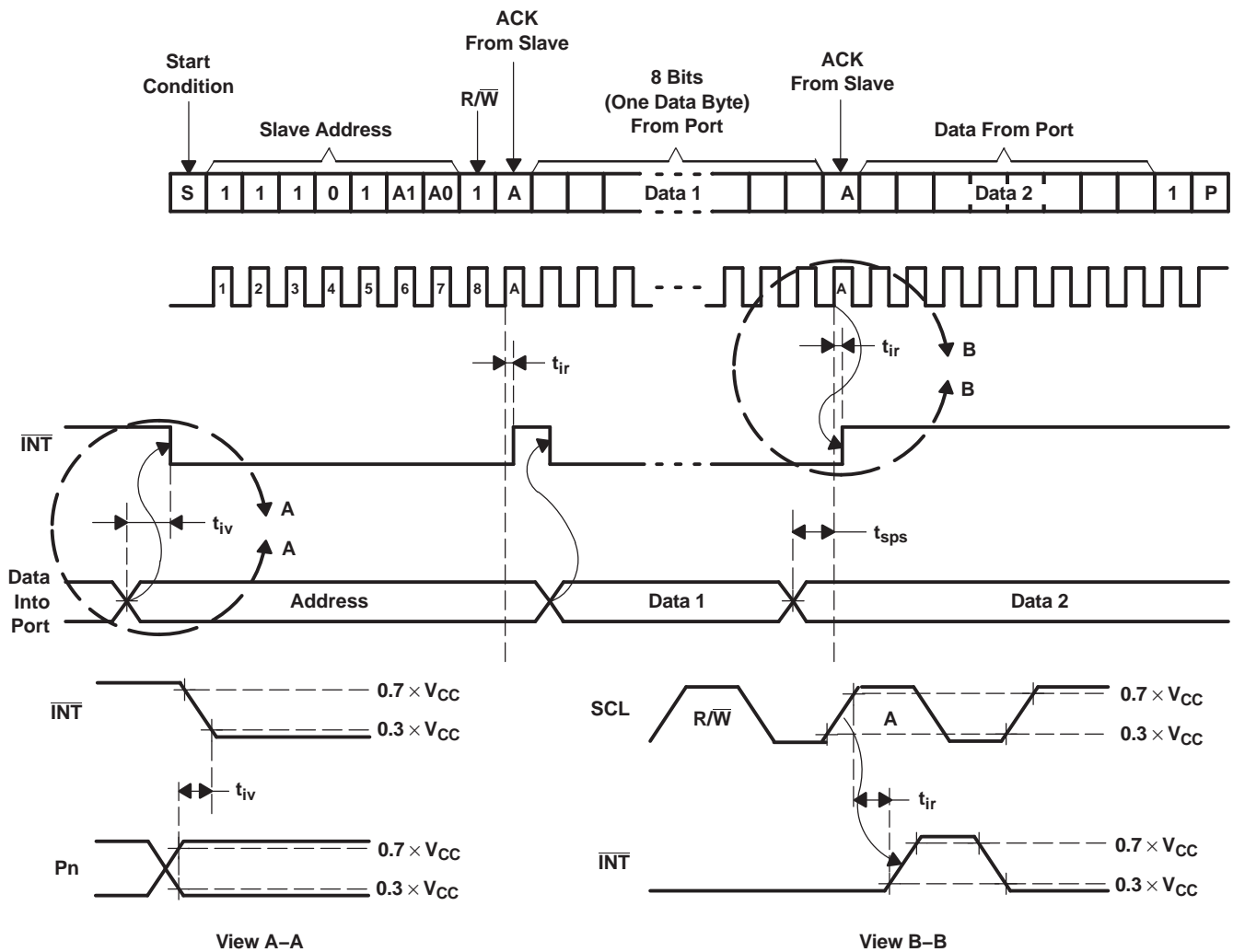
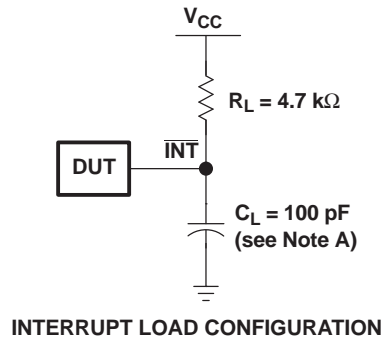
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

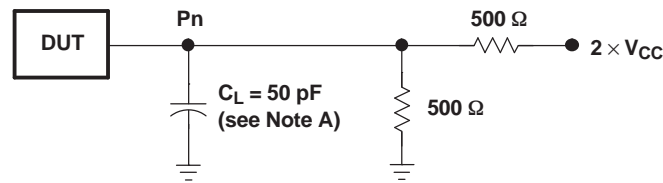
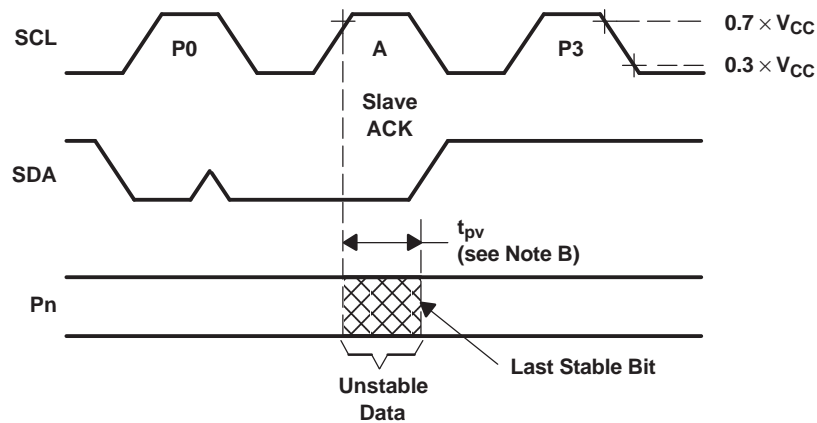
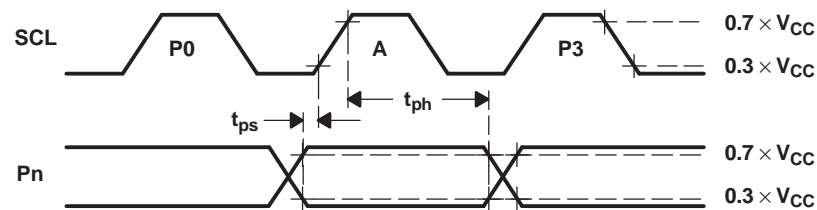
**Figure 13. I<sup>2</sup>C Interface Load Circuit And Voltage Waveforms**

Parameter Measurement Information (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

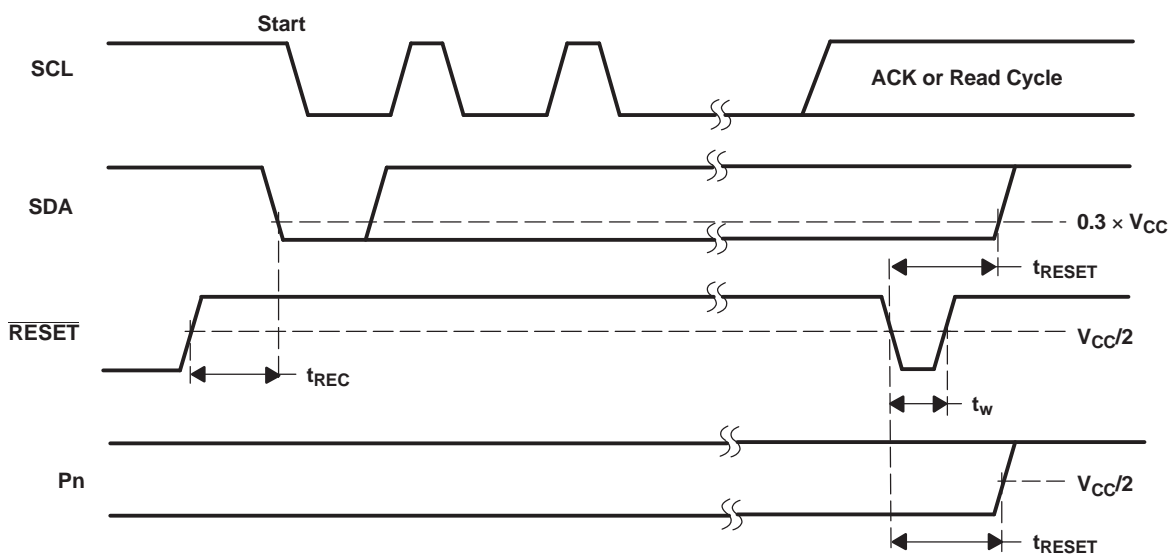
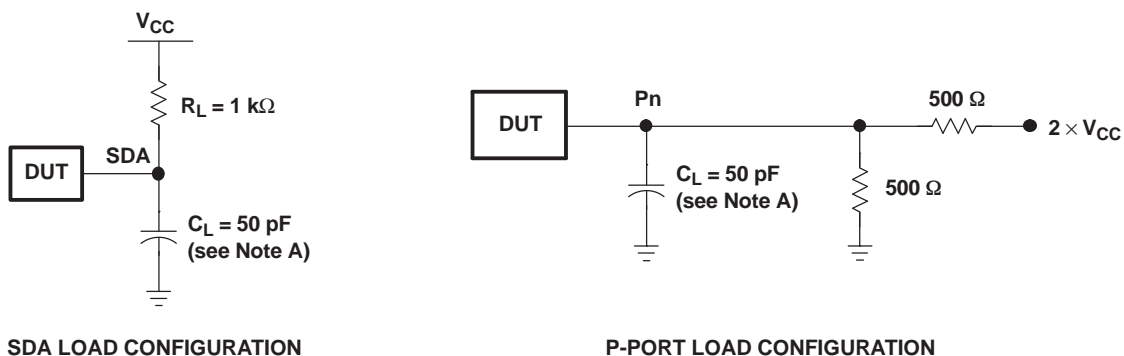
Figure 14. Interrupt Load Circuit And Voltage Waveforms

**Parameter Measurement Information (continued)**

**P-PORT LOAD CONFIGURATION**

**WRITE MODE ( $R/\bar{W} = 0$ )**

**READ MODE ( $R/\bar{W} = 1$ )**

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O (Pn) output.
- C. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 15. P-Port Load Circuit And Voltage Waveforms**

Parameter Measurement Information (continued)

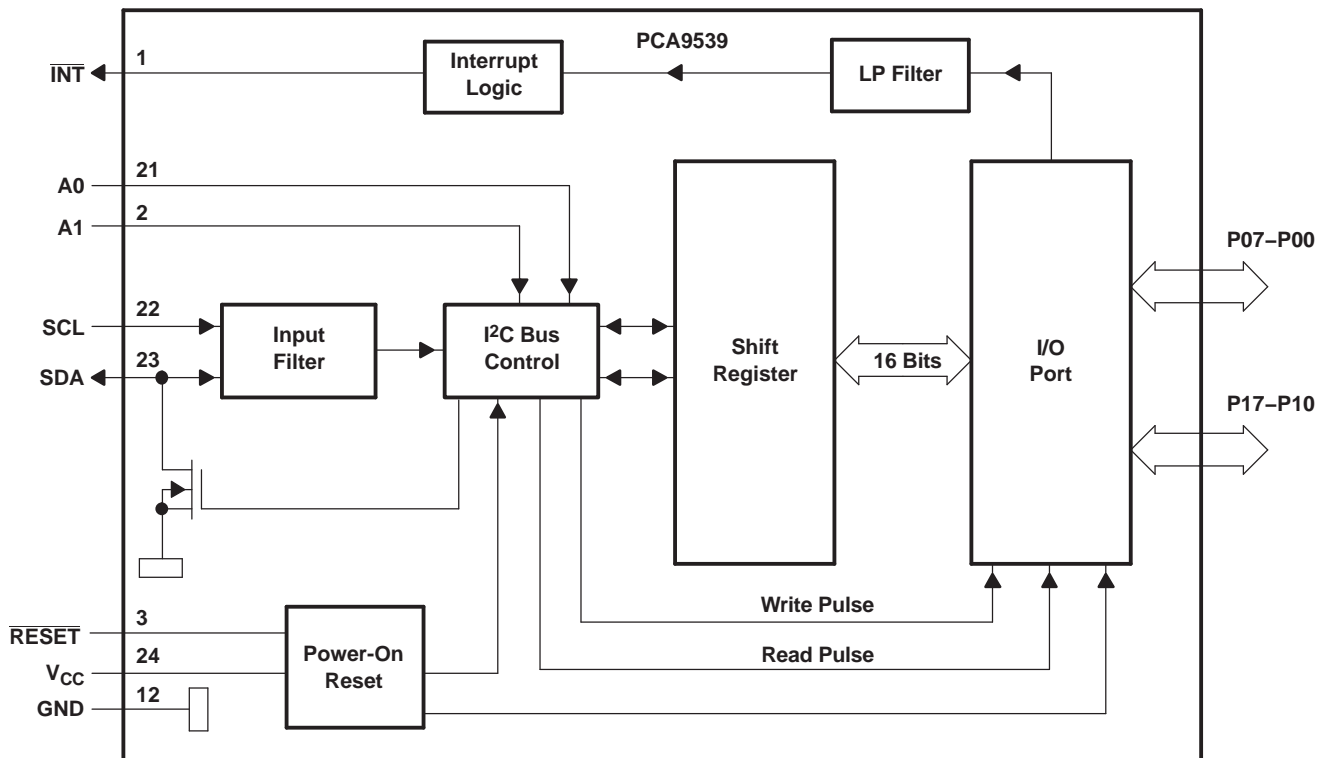


- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. I/Os are configured as inputs.
- E. All parameters and waveforms are not applicable to all devices.

Figure 16. Reset Load Circuits And Voltage Waveforms

## 8 Detailed Description

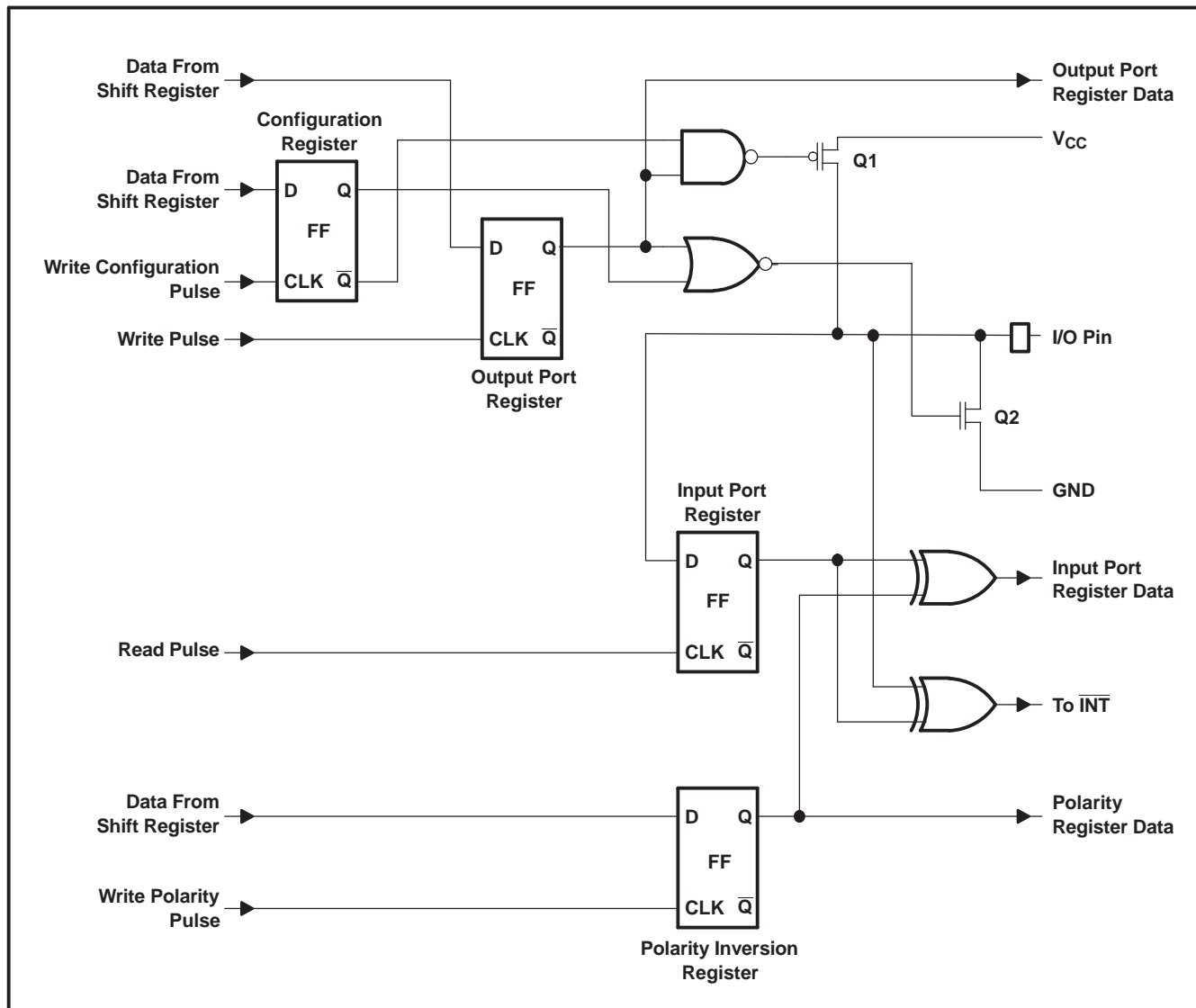
### 8.1 Functional Block Diagram



- A. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.
- B. All I/Os are set to inputs at reset.

Figure 17. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



(1) At power-on reset, all registers return to default values.

Figure 18. Simplified Schematic Of P-Port I/Os

## 8.2 Device Functional Modes

### 8.2.1 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin low for a minimum of  $t_{W}$ . The PCA9539 registers and I<sup>2</sup>C/SMBus state machine are held in their default states until  $\overline{\text{RESET}}$  is once again high. This input requires a pullup resistor to  $V_{CC}$ , if no active connection is used.

#### 8.2.1.1 $\overline{\text{RESET}}$ Errata

If  $\overline{\text{RESET}}$  voltage set higher than  $V_{CC}$ , current will flow from  $\overline{\text{RESET}}$  pin to  $V_{CC}$  pin.

#### System Impact

$V_{CC}$  will be pulled above its regular voltage level

#### System Workaround

Design such that  $\overline{\text{RESET}}$  voltage is same or lower than  $V_{CC}$

### 8.2.2 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the PCA9539 in a reset condition until  $V_{CC}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9539 registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{CC}$  must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the [Power-On Reset Errata](#) section.

### 8.2.3 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in [Figure 18](#)) are off, which creates a high-impedance input. The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

### 8.2.4 Interrupt ( $\overline{\text{INT}}$ ) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{IV}$ , the signal  $\overline{\text{INT}}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ . Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pullup resistor to  $V_{CC}$ .

## Device Functional Modes (continued)

### 8.2.4.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I<sup>2</sup>C command byte (register pointer) written to the device was 00h.

---

#### NOTE

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

---

2. Any other slave device on the I<sup>2</sup>C bus acknowledges an address byte with the R/W bit set high

### System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

### System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9539 device or before reading from another slave device.

---

#### NOTE

Software change will be compatible with other versions (competition and TI redesigns) of this device.

---

## 8.3 Programming

### 8.3.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 19](#)). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

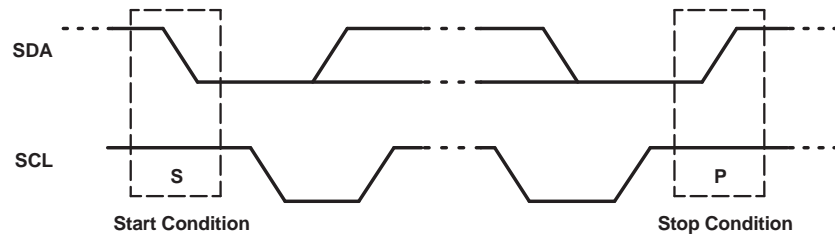
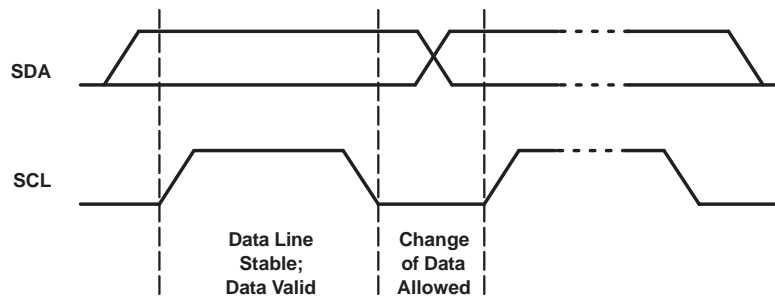
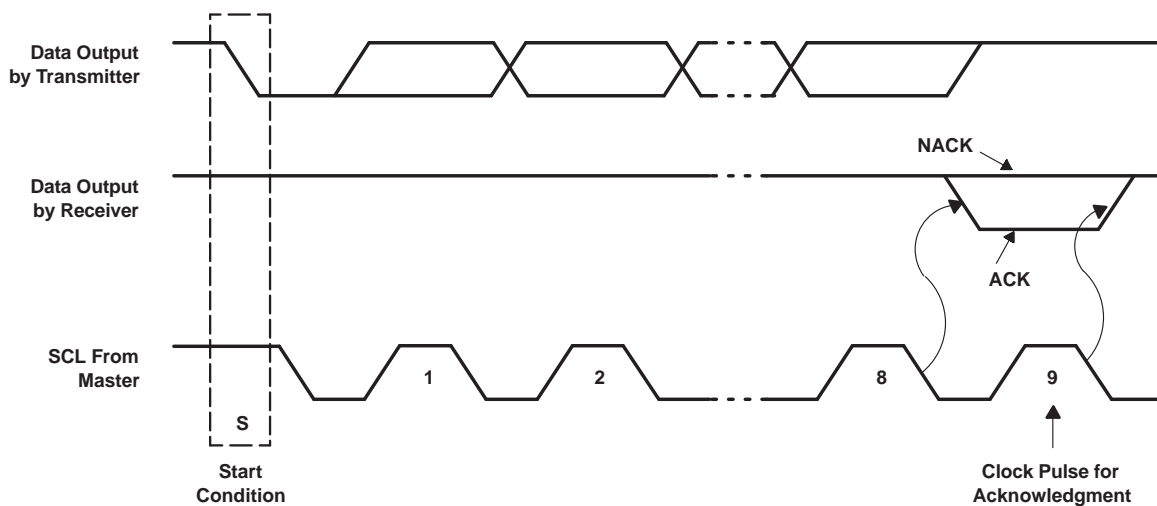
After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 and A1) of the slave device must not be changed between the Start and Stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see [Figure 20](#)).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 19](#)).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 21](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

**Programming (continued)**

**Figure 19. Definition Of Start And Stop Conditions**

**Figure 20. Bit Transfer**

**Figure 21. Acknowledgment On I<sup>2</sup>C Bus**
**8.3.2 Register Map**
**Table 1. Interface Definition**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	H	H	H	L	H	A1	A0	R/W
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.2.1 Device Address

Figure 22 shows the address byte of the PCA9539.

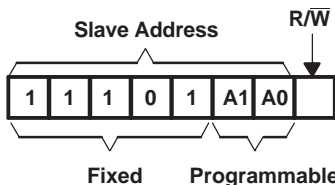


Figure 22. Pca9539 Address

Table 2. Address Reference

INPUTS		I <sup>2</sup> C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9539. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

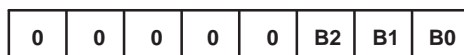


Figure 23. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

### 8.3.2.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port register will be accessed next.

**Table 4. Registers 0 And 1 (Input Port Registers)**

<b>Bit</b>	<b>I0.7</b>	<b>I0.6</b>	<b>I0.5</b>	<b>I0.4</b>	<b>I0.3</b>	<b>I0.2</b>	<b>I0.1</b>	<b>I0.0</b>
<b>Default</b>	X	X	X	X	X	X	X	X
<b>Bit</b>	<b>I1.7</b>	<b>I1.6</b>	<b>I1.5</b>	<b>I1.4</b>	<b>I1.3</b>	<b>I1.2</b>	<b>I1.1</b>	<b>I1.0</b>
<b>Default</b>	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 5. Registers 2 And 3 (Output Port Registers)**

<b>Bit</b>	<b>O0.7</b>	<b>O0.6</b>	<b>O0.5</b>	<b>O0.4</b>	<b>O0.3</b>	<b>O0.2</b>	<b>O0.1</b>	<b>O0.0</b>
<b>Default</b>	1	1	1	1	1	1	1	1
<b>Bit</b>	<b>O1.7</b>	<b>O1.6</b>	<b>O1.5</b>	<b>O1.4</b>	<b>O1.3</b>	<b>O1.2</b>	<b>O1.1</b>	<b>O1.0</b>
<b>Default</b>	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow Polarity Inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

**Table 6. Registers 4 And 5 (Polarity Inversion Registers)**

<b>Bit</b>	<b>N0.7</b>	<b>N0.6</b>	<b>N0.5</b>	<b>N0.4</b>	<b>N0.3</b>	<b>N0.2</b>	<b>N0.1</b>	<b>N0.0</b>
<b>Default</b>	0	0	0	0	0	0	0	0
<b>Bit</b>	<b>N1.7</b>	<b>N1.6</b>	<b>N1.5</b>	<b>N1.4</b>	<b>N1.3</b>	<b>N1.2</b>	<b>N1.1</b>	<b>N1.0</b>
<b>Default</b>	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7. Registers 6 And 7 (Configuration Registers)**

<b>Bit</b>	<b>C0.7</b>	<b>C0.6</b>	<b>C0.5</b>	<b>C0.4</b>	<b>C0.3</b>	<b>C0.2</b>	<b>C0.1</b>	<b>C0.0</b>
<b>Default</b>	1	1	1	1	1	1	1	1
<b>Bit</b>	<b>C1.7</b>	<b>C1.6</b>	<b>C1.5</b>	<b>C1.4</b>	<b>C1.3</b>	<b>C1.2</b>	<b>C1.1</b>	<b>C1.0</b>
<b>Default</b>	1	1	1	1	1	1	1	1

### 8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9539 through write and read commands.

#### 8.3.2.4.1 Writes

Data is transmitted to the PCA9539 by sending the device address and setting the least-significant bit to a logic 0 (see [Figure 22](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9539 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion ports, and Configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 24 and Figure 25). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

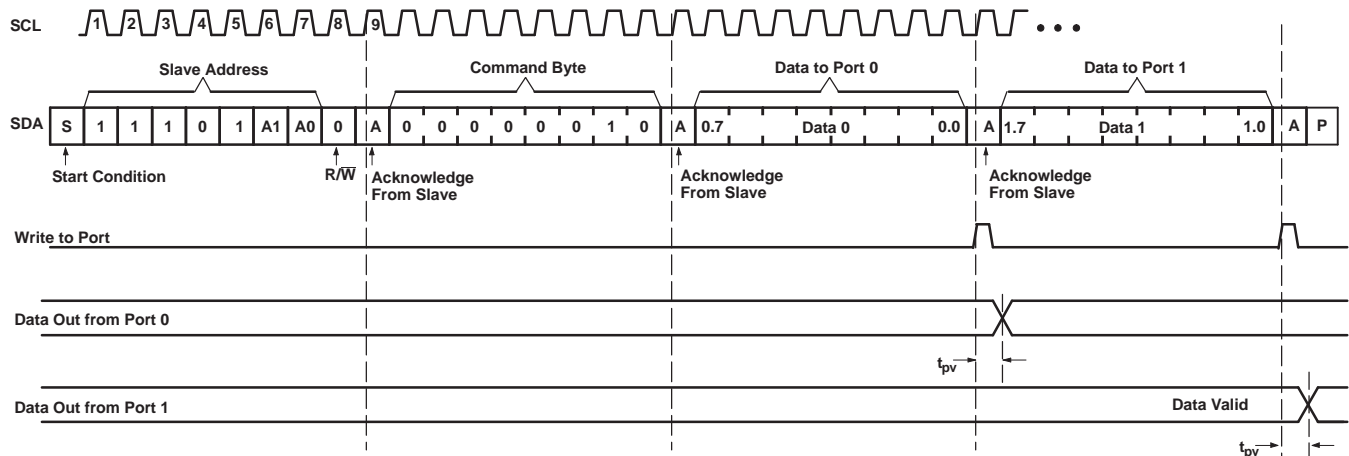


Figure 24. Write To Output Port Registers

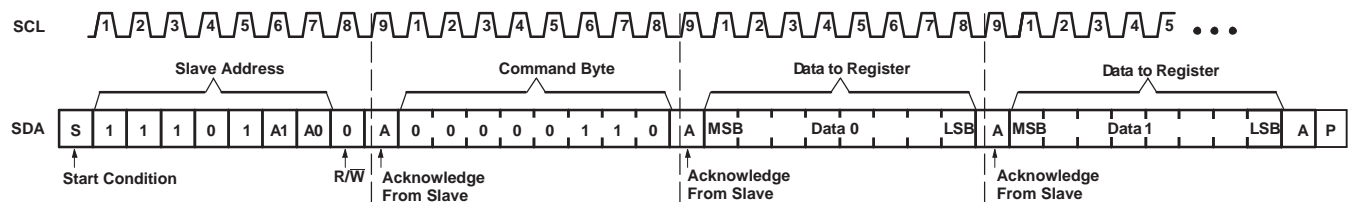


Figure 25. Write To Configuration Registers

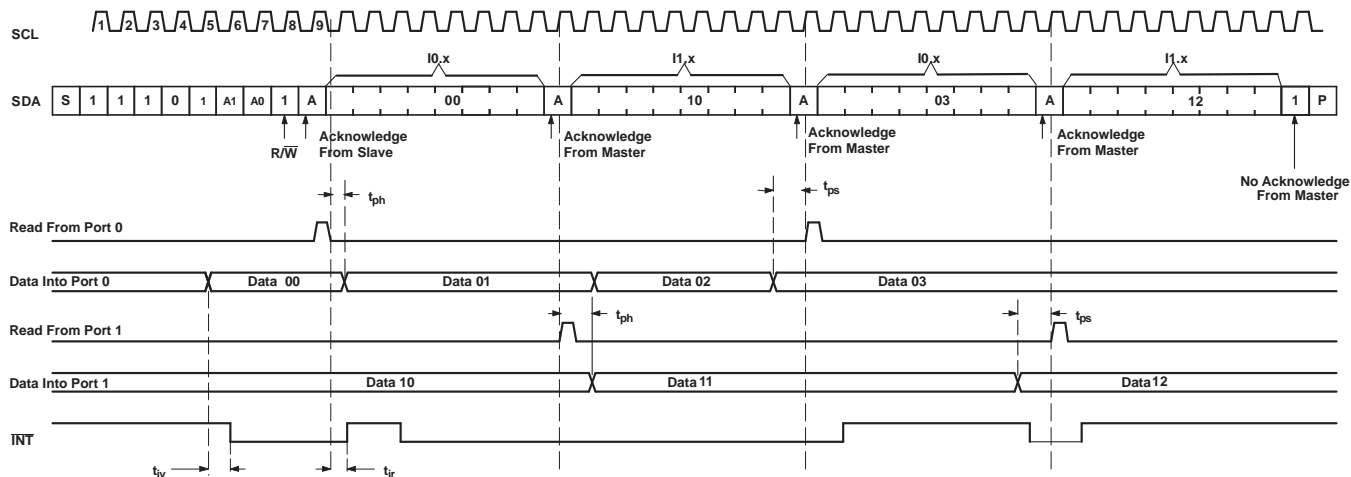
### 8.3.2.4.2 Reads

The bus master first must send the PCA9539 address with the least-significant bit set to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9539 (see Figure 26 through Figure 28).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.





- A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).
- B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see [Figure 26](#) for these details).

**Figure 28. Read Input Port Register, Scenario 2**



## Typical Application (continued)

### 9.1.1 Detailed Design Procedure

#### 9.1.1.1 Minimizing $I_{CC}$ When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to  $V_{CC}$  through a resistor (see Figure 29). Because the LED acts as a diode, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in Electrical Characteristics shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to  $V_{CC}$ , when the LED is off, to minimize current consumption.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{CC}$  at or above  $V_{CC}$  and prevent additional supply-current consumption when the LED is off.

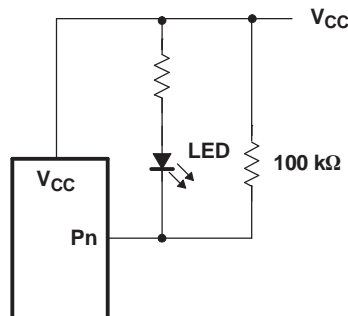


Figure 30. High-Value Resistor In Parallel With Led

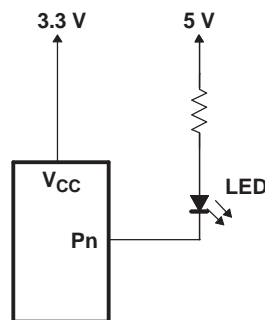


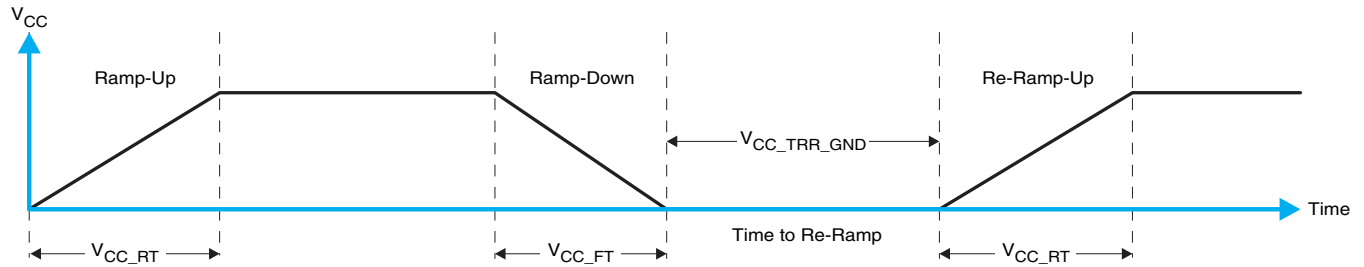
Figure 31. Device Supplied By Lower Voltage

## 10 Power Supply Recommendations

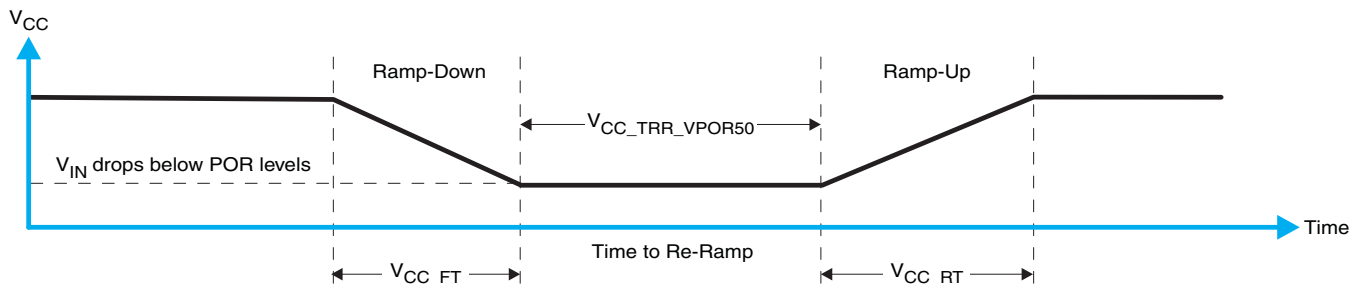
### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9539 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 32](#) and [Figure 33](#).



**Figure 32.  $V_{CC}$  Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To  $V_{CC}$**



**Figure 33.  $V_{CC}$  Is Lowered Below The Por Threshold, Then Ramped Back Up To  $V_{CC}$**

[Table 8](#) specifies the performance of the power-on reset feature for PCA9539 for both types of power-on reset.

**Table 8. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 32</a>	1		100	ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 32</a>	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See <a href="#">Figure 32</a>	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See <a href="#">Figure 33</a>	0.001			ms
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See <a href="#">Figure 34</a>			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See <a href="#">Figure 34</a>				$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.767		1.144	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$		1.033		1.428	V

(1)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 34 and Table 8 provide more information on how to measure these specifications.

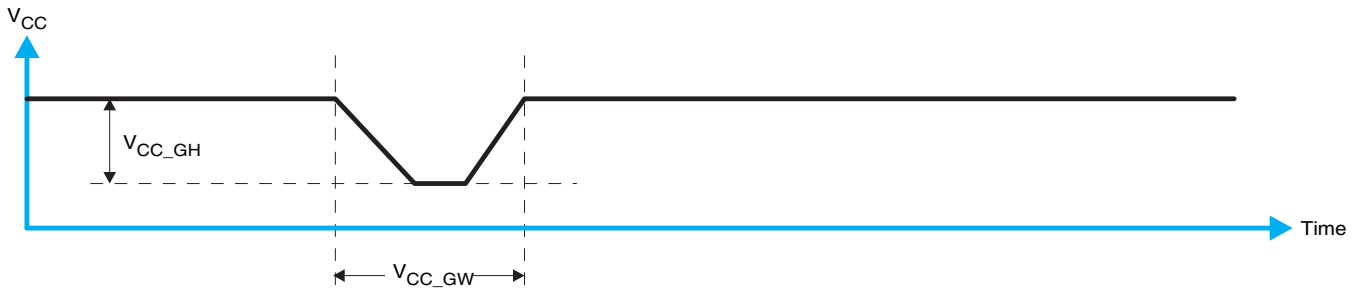


Figure 34. Glitch Width And Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 35 and Table 8 provide more details on this specification.

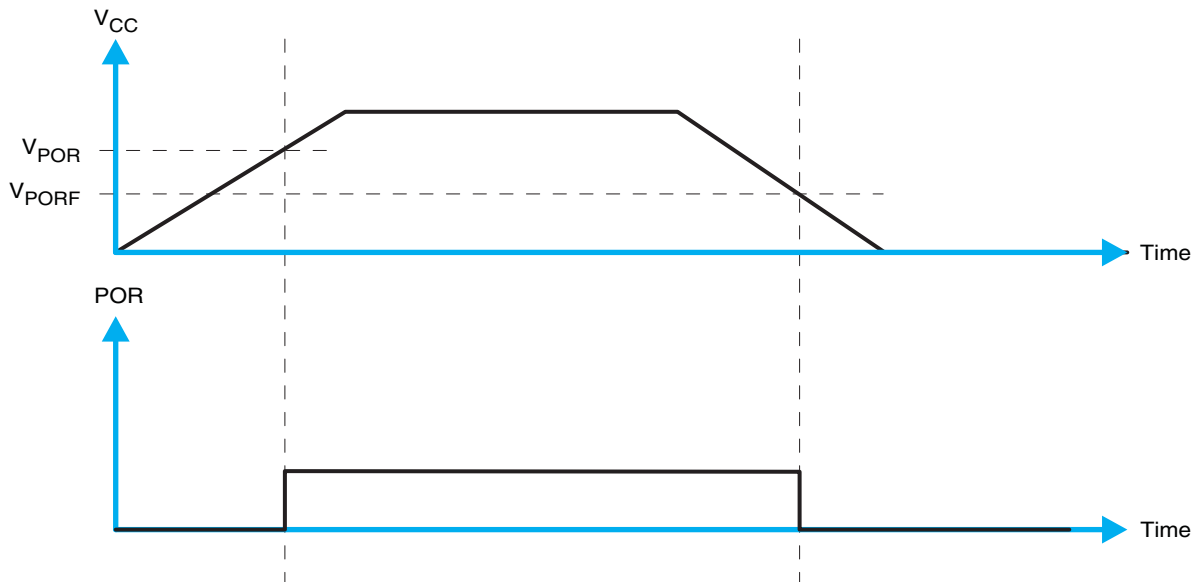


Figure 35.  $V_{POR}$

## 10.2 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed above.

### System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9539DB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	<a href="#">Samples</a>
PCA9539DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9539	<a href="#">Samples</a>
PCA9539DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	<a href="#">Samples</a>
PCA9539DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	<a href="#">Samples</a>
PCA9539DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539	<a href="#">Samples</a>
PCA9539DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539	<a href="#">Samples</a>
PCA9539PW	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	
PCA9539PWE4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	
PCA9539PWG4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	
PCA9539PWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	
PCA9539PWRG4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539	
PCA9539RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD9539	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

---

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9539DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9539DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9539DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9539DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9539PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9539RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



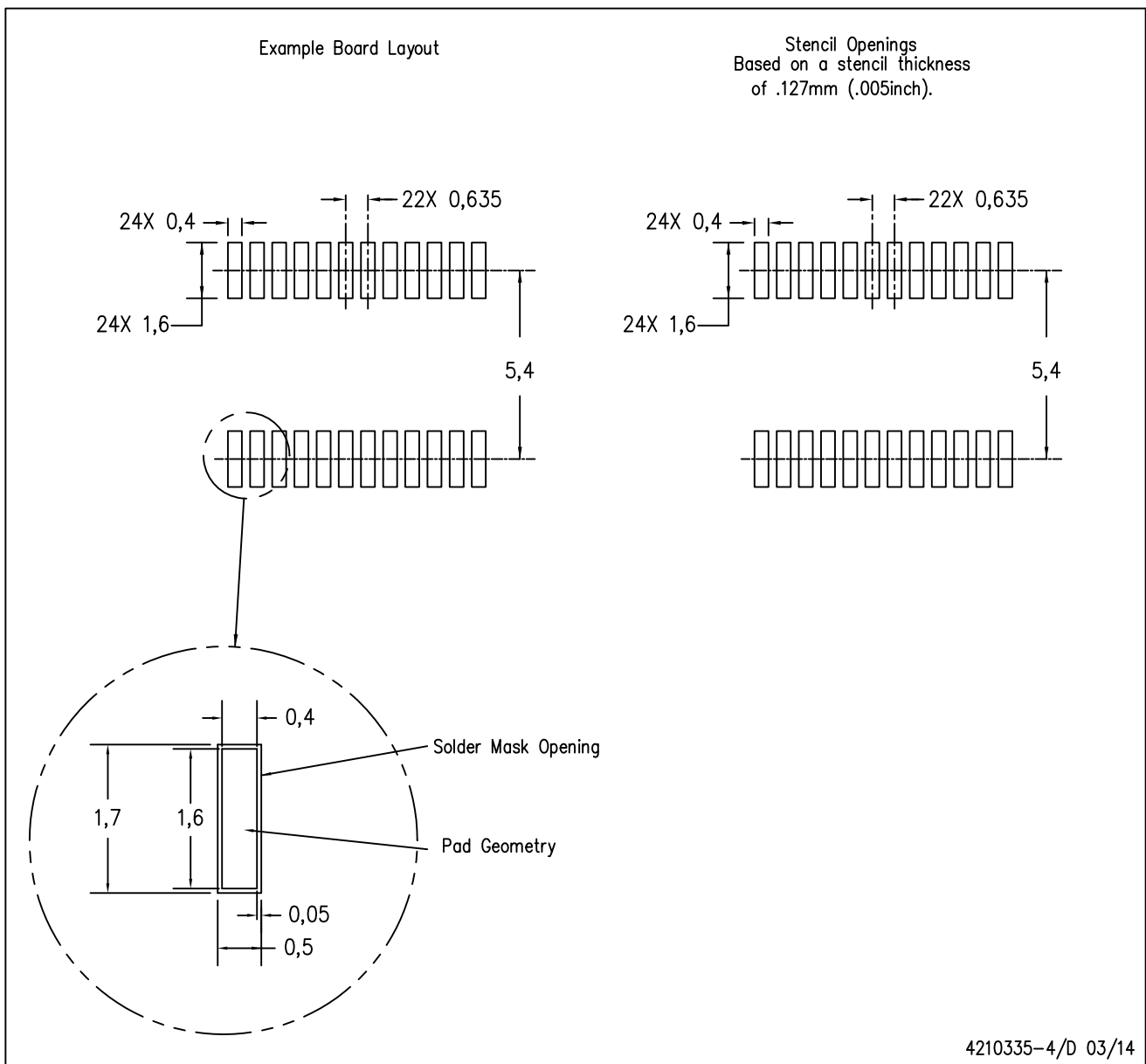
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9539DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
PCA9539DBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCA9539DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCA9539DWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCA9539PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCA9539RGER	VQFN	RGE	24	3000	367.0	367.0	35.0



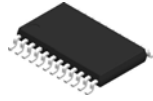
DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

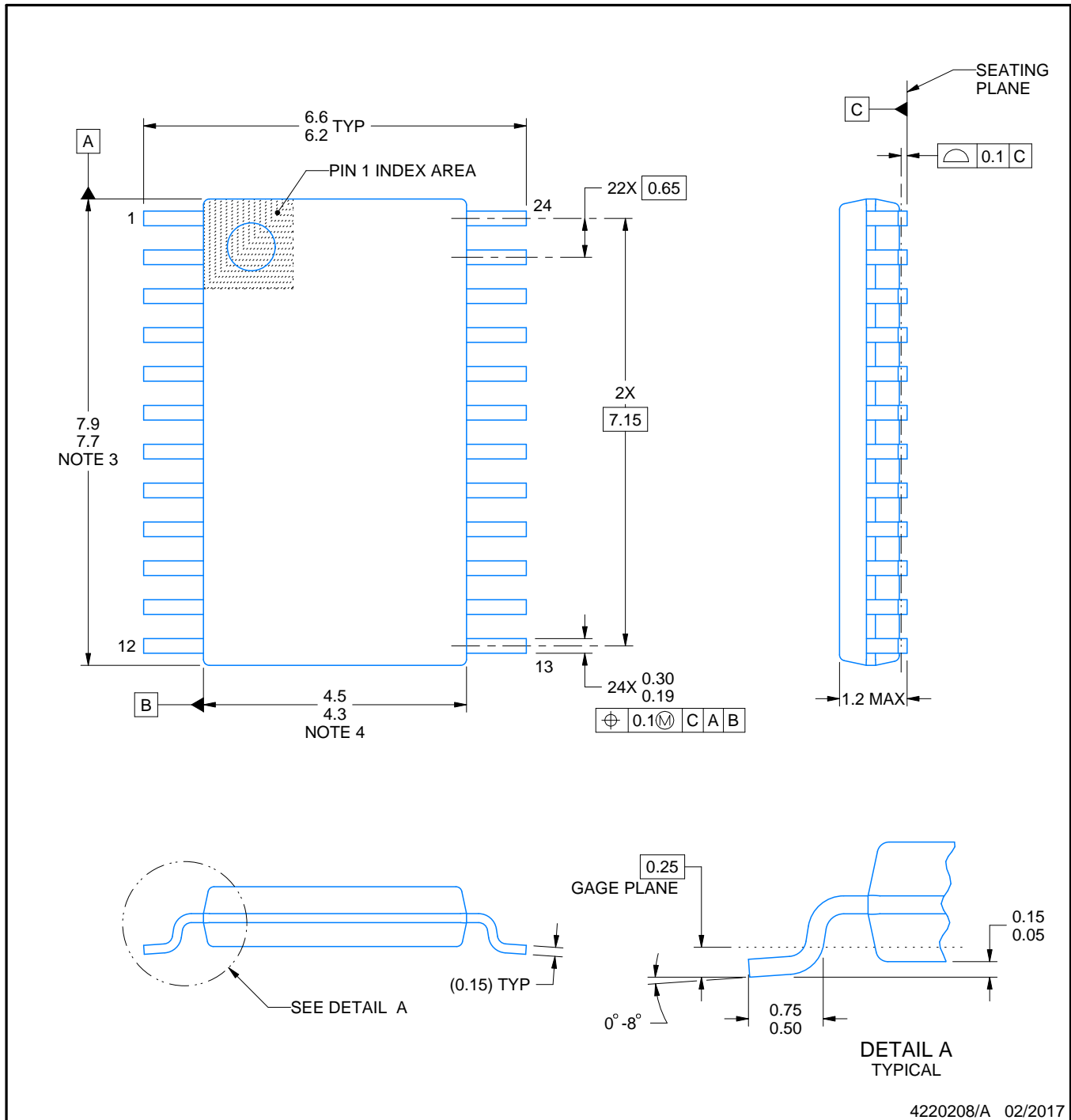
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

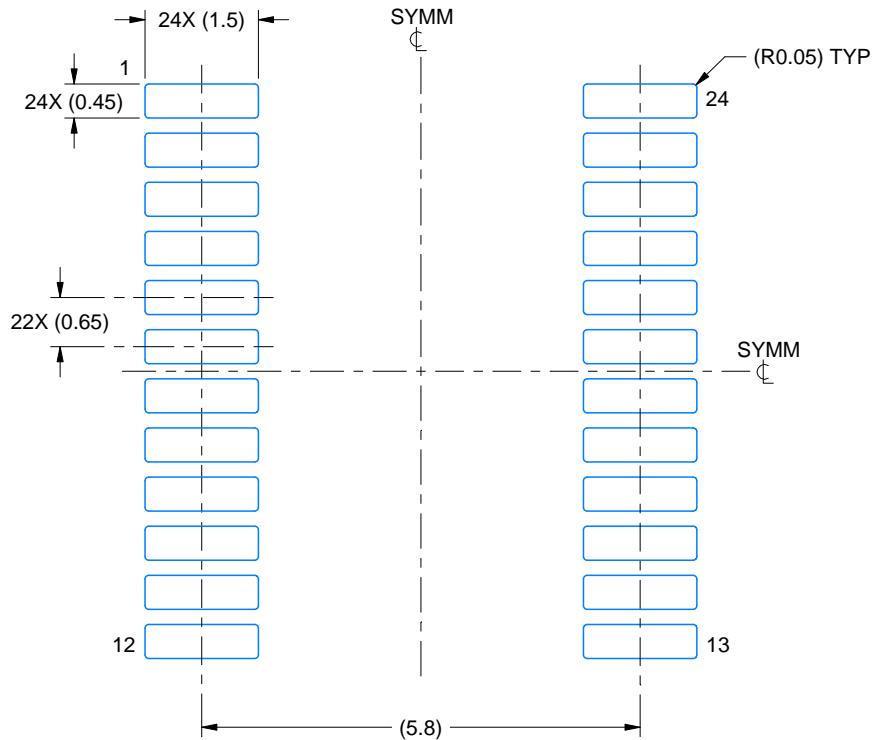
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

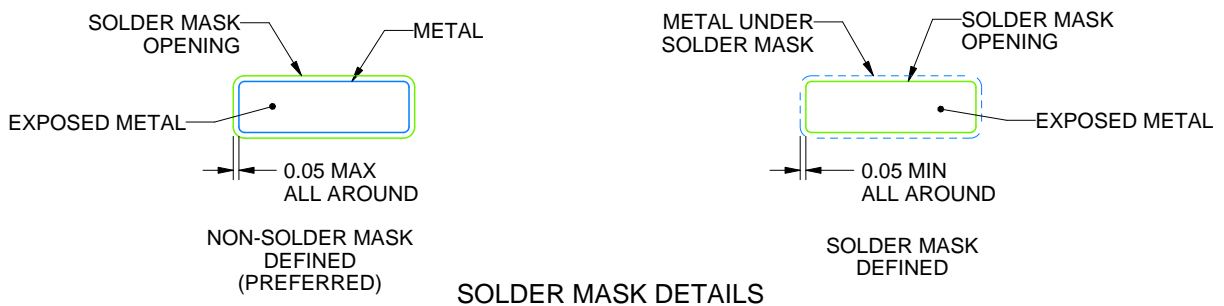
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

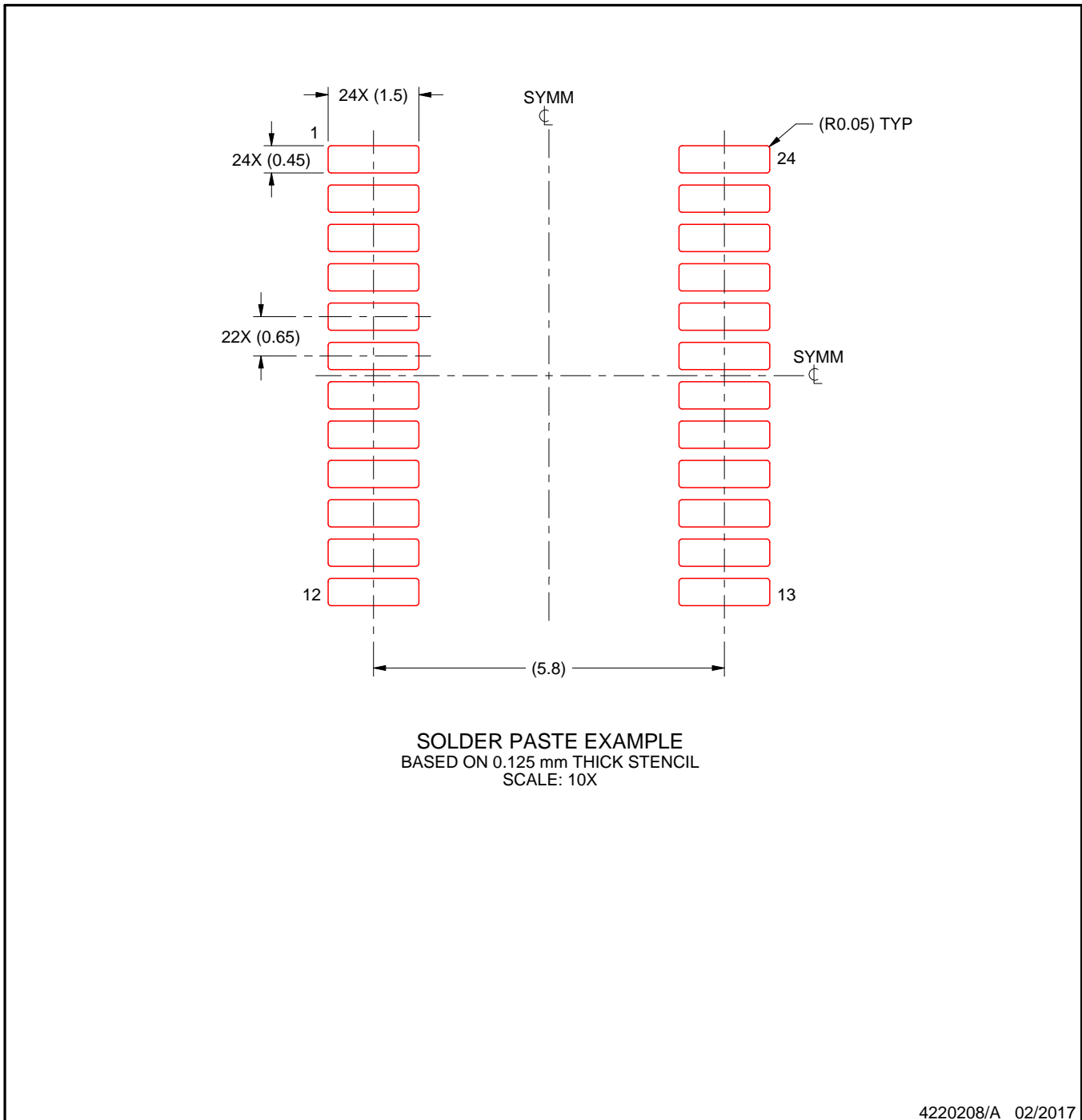
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



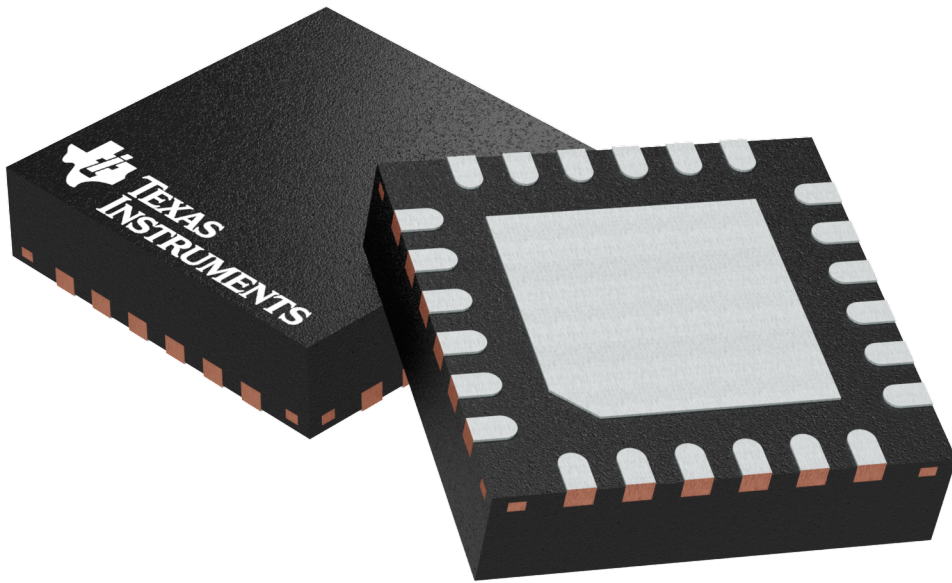


## GENERIC PACKAGE VIEW

RGE 24

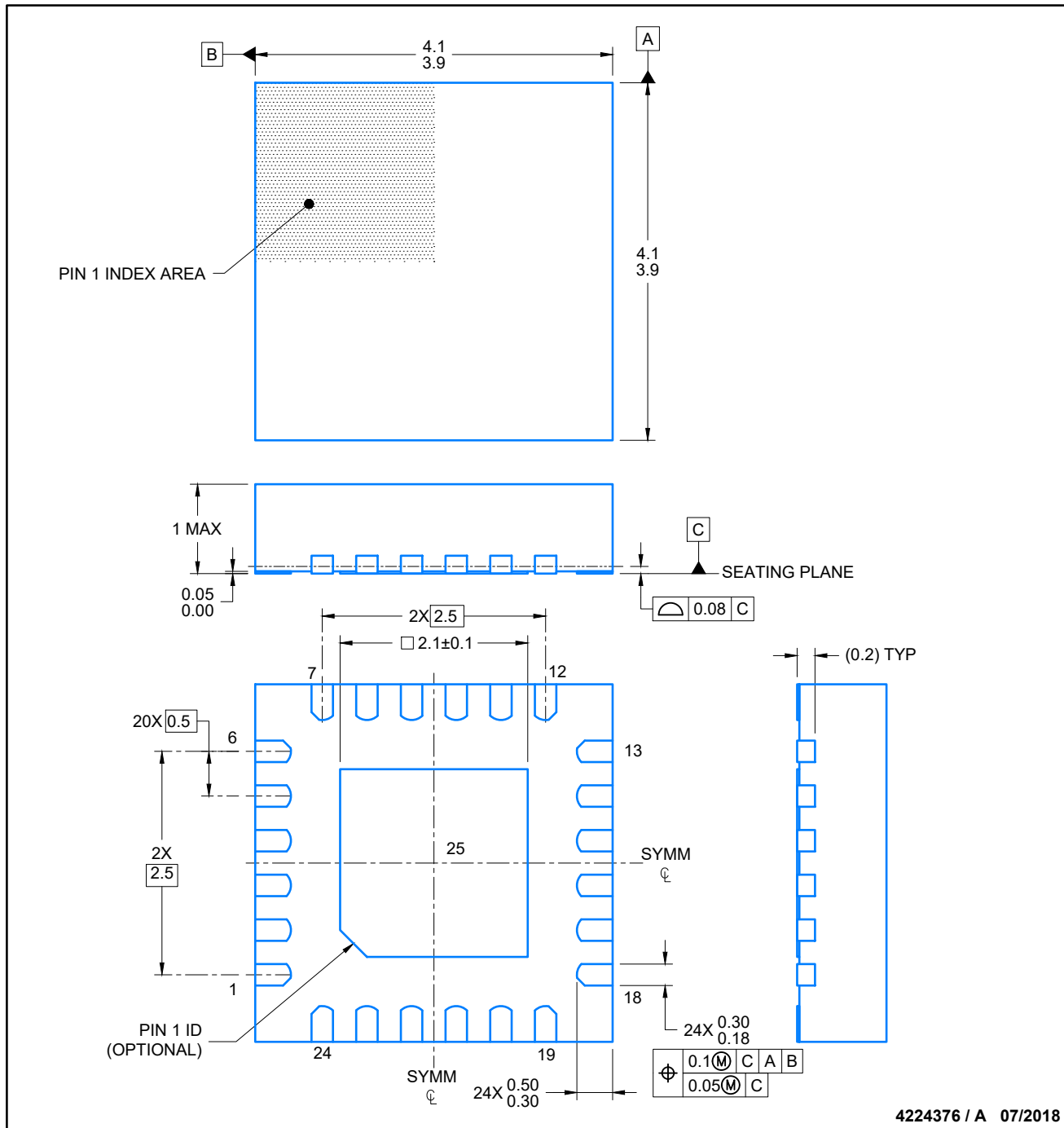
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



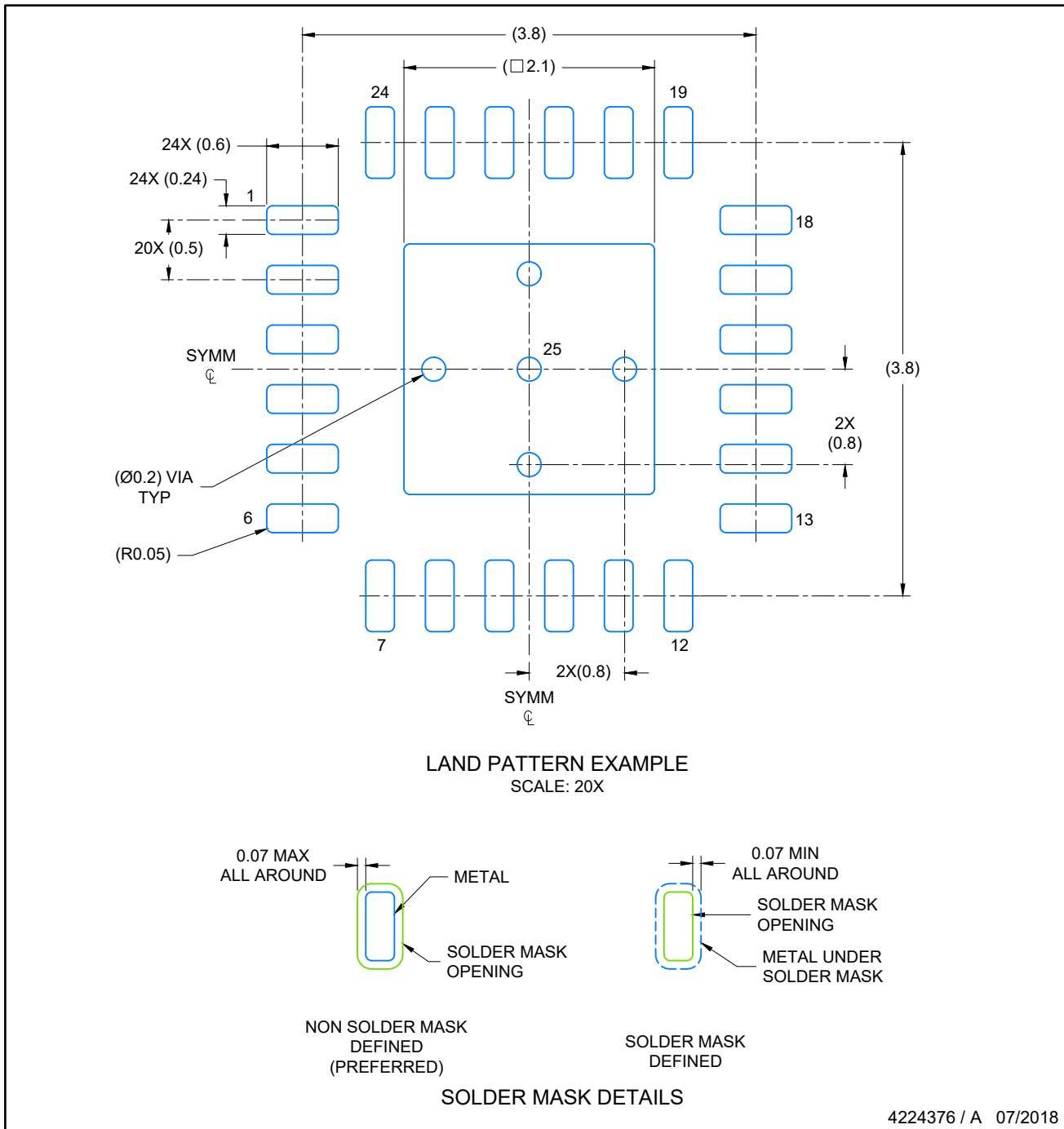
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



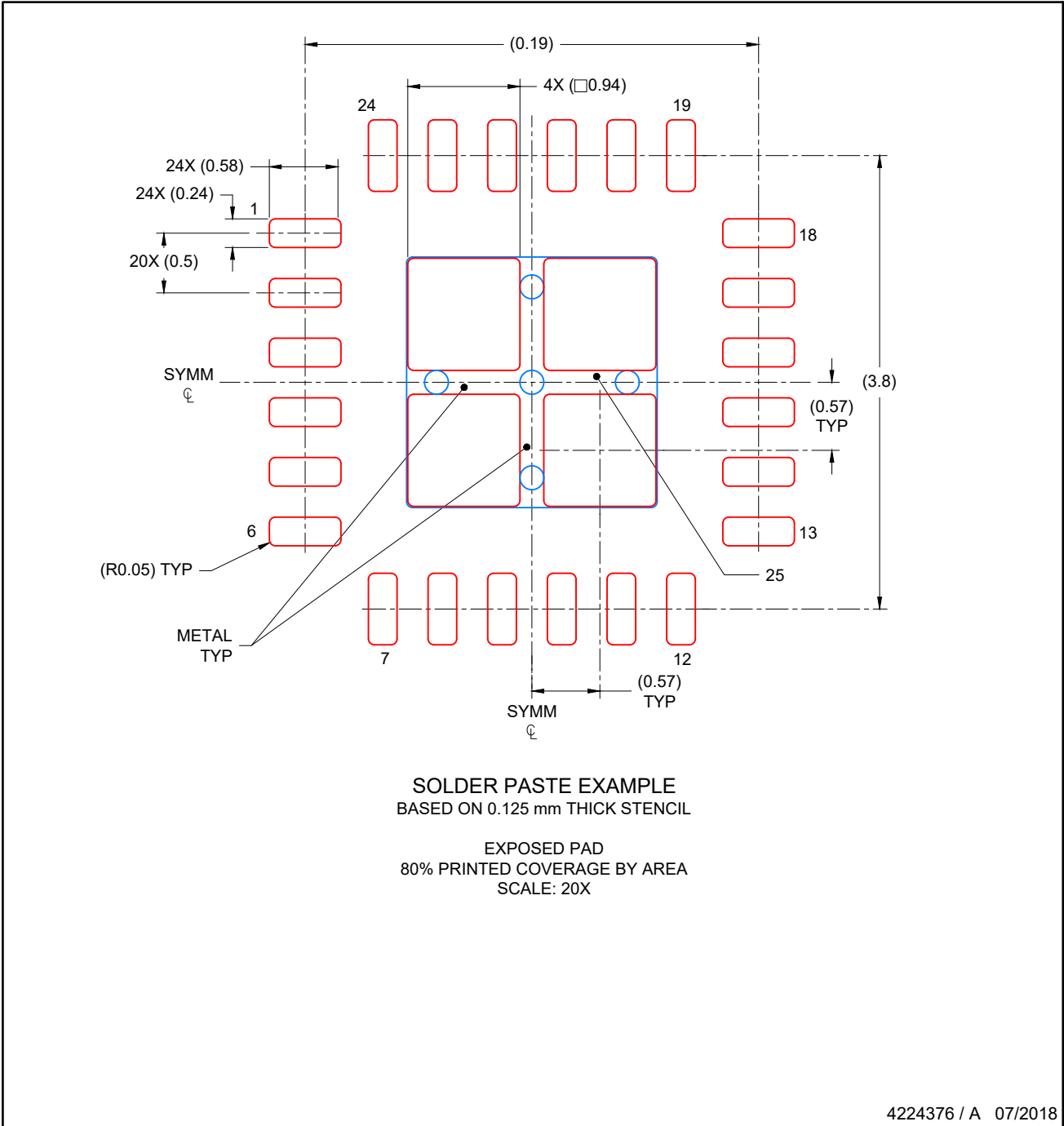
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View PCA9539PWR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management