P89LPC912/913/914

8-bit microcontrollers with two-clock 80C51 core, 1 kB 3 V flash with 128-byte RAM

Rev. 05 — 28 September 2007 Product data sheet

1. General description

The P89LPC912/913/914 are single-chip microcontrollers in low-cost 14-pin packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC912/913/914 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 1 kB byte-erasable flash code memory organized into 256 B sectors and 16 B pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 128 B RAM data memory.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow or to become a PWM output.
- 23-bit system timer that can also be used as a RTC.
- Two analog comparators with selectable inputs and reference source.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities (P89LPC913, P89LPC914).
- SPI communication port.
- Internal RC oscillator (factory calibrated to ±1 %) option allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- Up to 12 I/O pins when using internal oscillator and reset options.

2.2 Additional features

- 14-pin TSSOP packages.
- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz (167 ns to 333 ns at 12 MHz). This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.

- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz (P89LPC912, P89LPC913).
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open-drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC912/913/914 when internal reset option is selected.
- Four interrupt priority levels.
- Four keypad interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison

Table 1 highlights the differences between these three devices. For a complete list of device features, please see Section 2 “Features” on page 1.

Table 1. Product comparison

Type number	External crystal pins	X2 CLKOUT	T0 PWM output	SPI with $\overline{SS}$ pin	SPI without $\overline{SS}$ pin	UART		Max f_{osc} (MHz)
						TXD	RXD	
P89LPC912	X	X	X	X	-	-	-	18
P89LPC913	X	X	-	-	X	X	X	18
P89LPC914	-	-	X	X	-	X	X	12

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC912FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC912HDH			
P89LPC913FDH			
P89LPC914FDH			

4.1 Ordering options

Table 3. Ordering options

Type number	Temperature range	Frequency
P89LPC912FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC912HDH	–40 °C to +125 °C	0 MHz to 18 MHz
P89LPC913FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC914FDH	–40 °C to +85 °C	0 MHz to 12 MHz

5. Block diagram

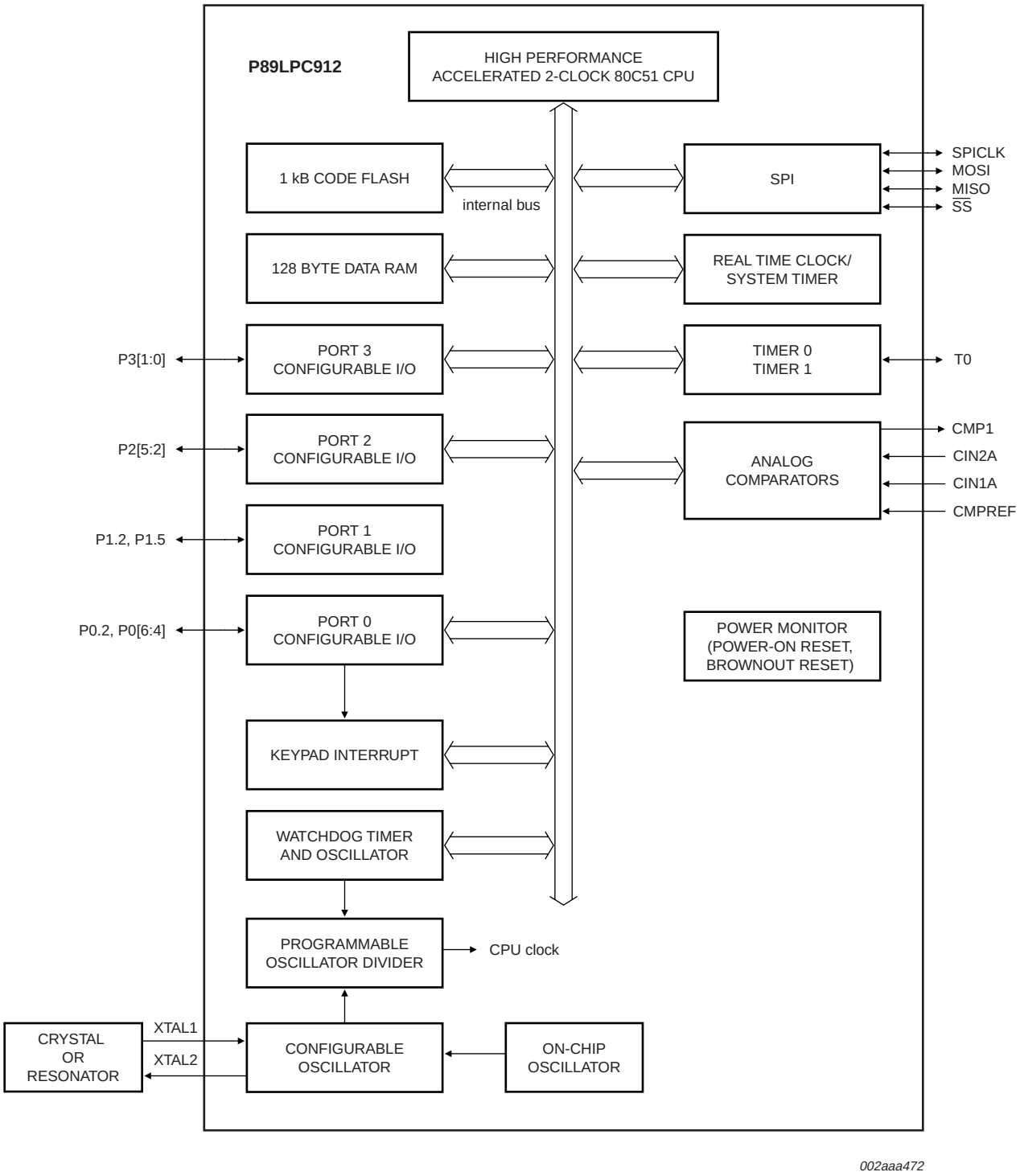


Fig 1. P89LPC912 block diagram

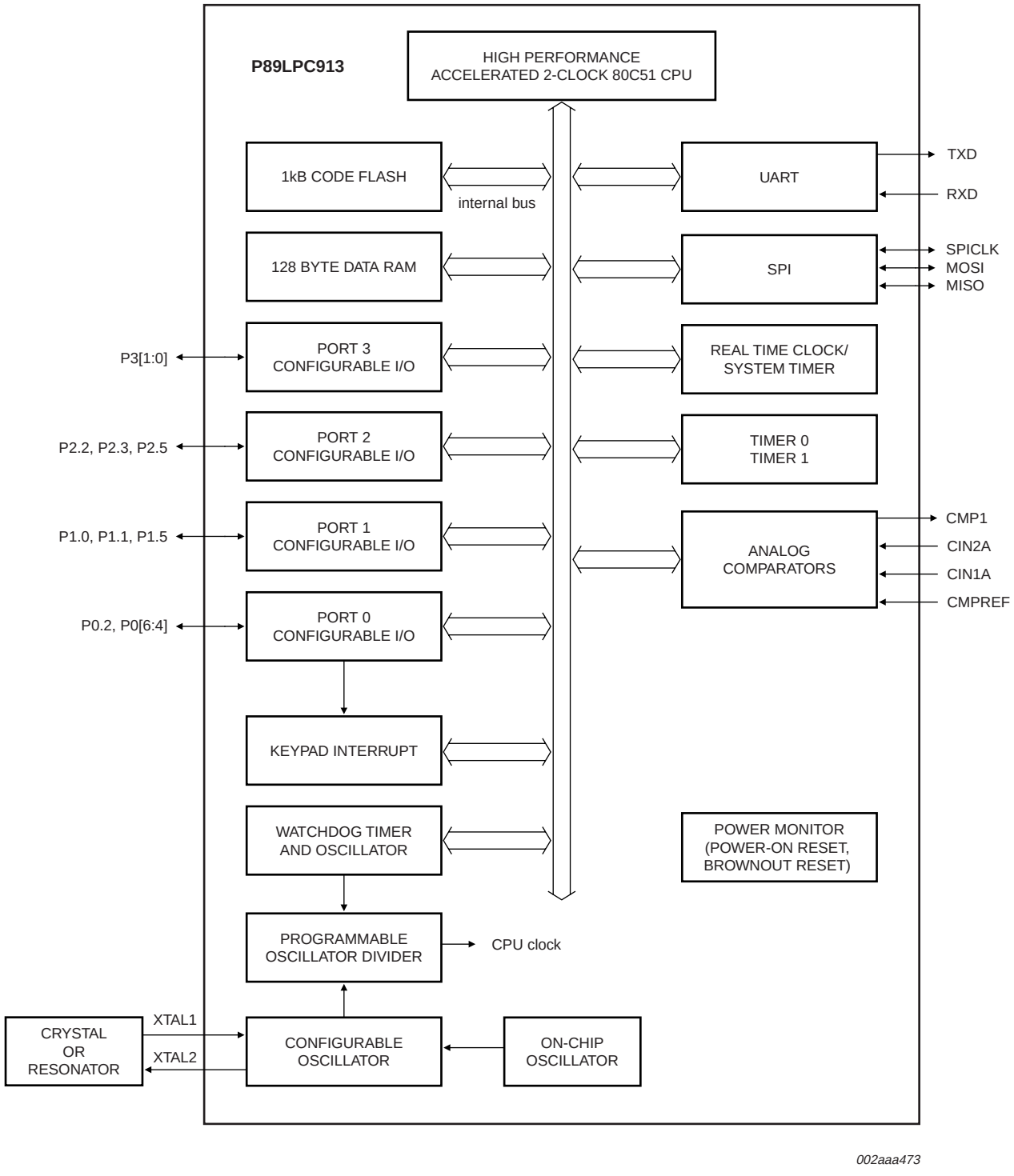


Fig 2. P89LPC913 block diagram

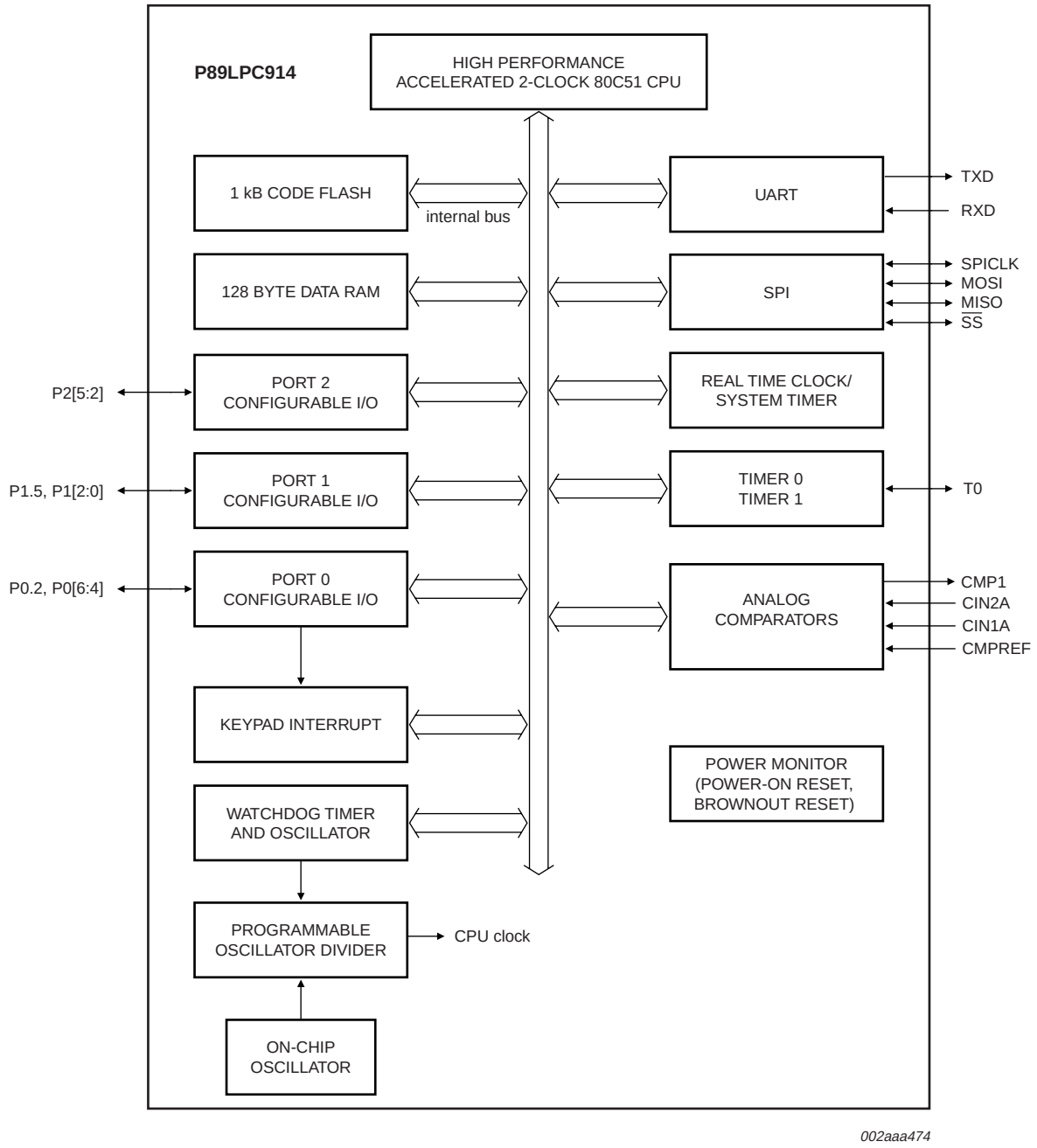


Fig 3. P89LPC914 block diagram

6. Functional diagram

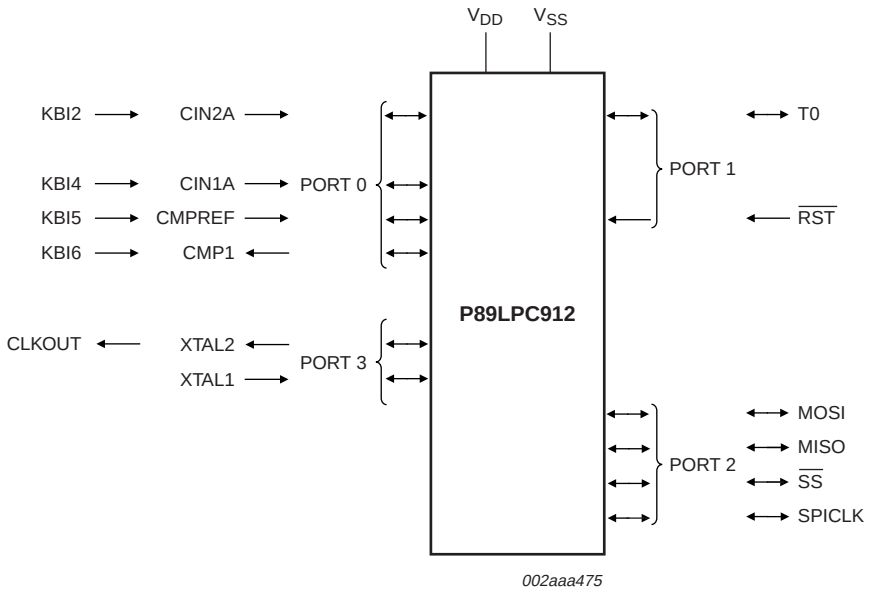


Fig 4. P89LPC912 functional diagram

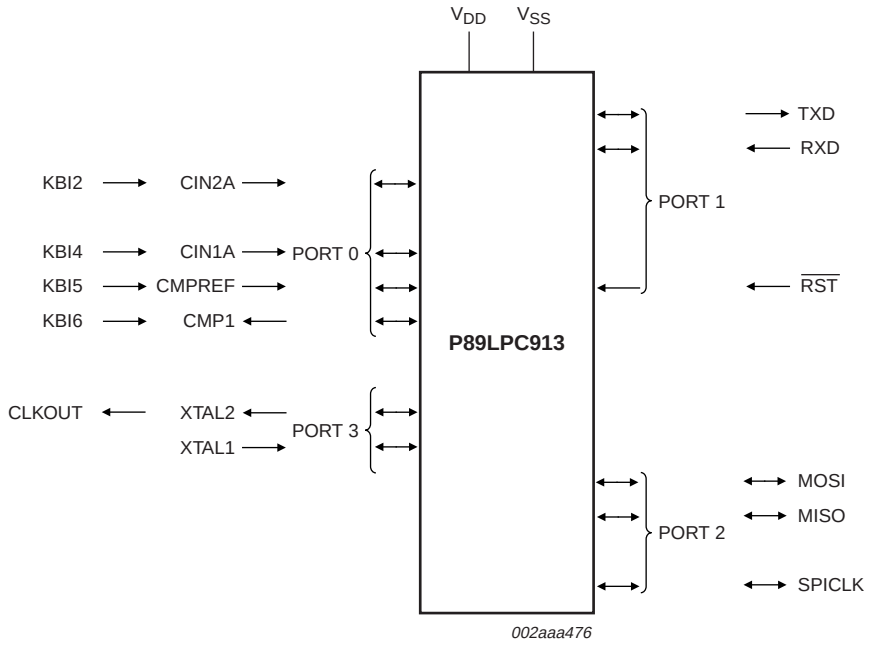


Fig 5. P89LPC913 functional diagram

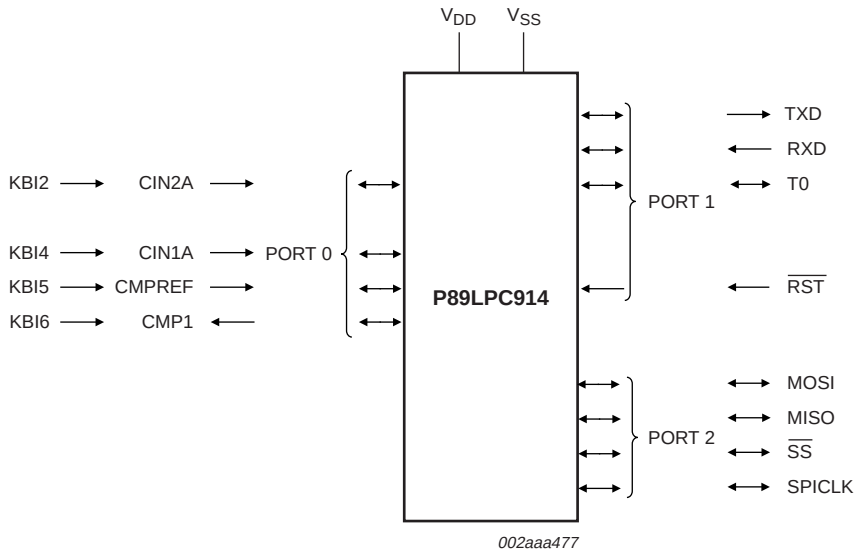


Fig 6. P89LPC914 functional diagram

7. Pinning information

7.1 Pinning

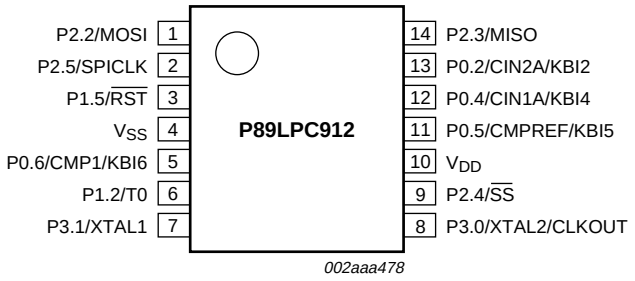


Fig 7. P89LPC912 TSSOP14 pin configuration

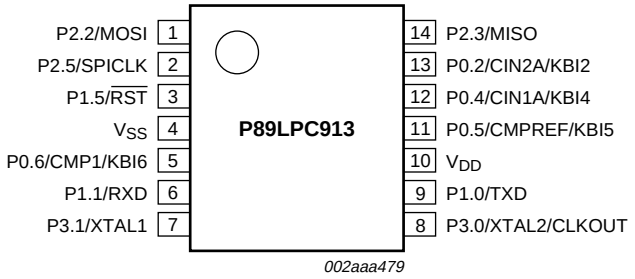


Fig 8. P89LPC913 TSSOP14 pin configuration

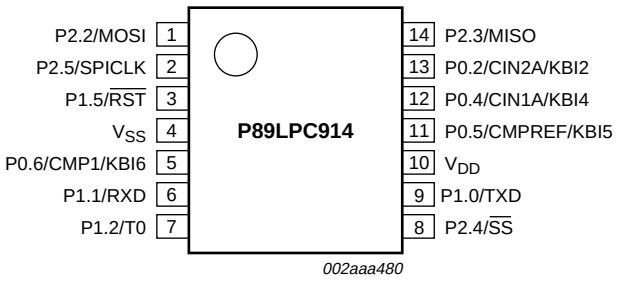


Fig 9. P89LPC914 TSSOP14 pin configuration

7.2 Pin description

Table 4. P89LPC912 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P1.2, P1.5		I/O (P1.2); I (P1.5)	**Port 1:** Port 1 is a 2-bit I/O port with P1.2 having a user-configurable output type as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the P1.2 input and outputs depends upon the port configuration selected. Refer to Section 8.12.1 “Port configurations” and Table 13 “Static characteristics” for details. P1.2 is an open drain when used as an output. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.2/T0	6	I/O	**P1.2 —** Port 1 bit 2. (Open drain when used as an output.)
		I/O	**T0 —** Timer/counter 0 external count input or overflow output. (Open drain when used as outputs.).
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5. (Input only.)
		I	**$\overline{\text{RST}}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 4. P89LPC912 pin description *...continued*

Symbol	Pin	Type	Description
P2.2 to P2.5		I/O	**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	9	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 5. P89LPC913 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P1.0, P1.1, P1.5		I/O (P1.0, P1.1); I (P1.5)	**Port 1:** Port 1 is a 3-bit I/O port with a user-configurable output type, except for P1.5 noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 5. P89LPC913 pin description *...continued*

Symbol	Pin	Type	Description
P2.2, P2.3, P2.5		I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 6. P89LPC914 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF / KBI5	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P1.0 to P1.2, P1.5		I/O (P1.0 to P1.2); I (P1.5)	**Port 1:** Port 1 is a 4-bit I/O port with a user-configurable output type, except for three pins noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.2 is an open drain when used as an output. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
P1.2/T0	7	I/O	**P1.2 —** Port 1 bit 2. (Open drain when used as an output.)
		I/O	**T0 —** Timer/counter 0 external count input or overflow output. (Open drain when used as outputs.)
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.

Table 6. P89LPC914 pin description *…continued*

Symbol	Pin	Type	Description
P2.2 to P2.5		I/O	**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	8	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

8. Functional description

Remark: Please refer to the P89LPC912/913/914 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 7. P89LPC912 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**
ACC*	Accumulator	E0H							
AUXR1	Auxiliary function register	A2H	CLKLP	-	-	ENT0	SRST	0	-
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**
B*	B register	F0H							
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H	-	-	-	-	-	-	
FMADRL	Program flash address low	E6H							
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1
FMDATA	Program flash data	E5H							
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	-	ET1	-	ET0
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	-	-	-	-	ESPI	EC	EKBI
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	-	-	-	-	PSPI	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	-	-	-	-	PSPIH	PCH	PKBIH

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H							
KBPATN	Keypad pattern register	93H							
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H			$\overline{\text{RST}}$			T0	
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**
P2*	Port 2	A0H			SPICLK	$\overline{\text{SS}}$	MISO	MOSI	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**
P3*	Port 3	B0H							XTAL1
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)	
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)	
P1M1	Port 1 output mode 1	91H						(P1M1.2)	
P1M2	Port 1 output mode 2	92H						(P1M2.2)	
P2M1	Port 2 output mode 1	A4H			(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	
P2M2	Port 2 output mode 2	A5H			(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	
P3M1	Port 3 output mode 1	B1H							(P3M1.1)
P3M2	Port 3 output mode 2	B2H							(P3M2.1)
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	-
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
RTCL	Real-time clock register low	D3H							
SP	Stack pointer	81H							
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-
SPDAT	SPI data register	E3H							
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF
WDL	Watchdog load	C1H							
WFEED1	Watchdog feed 1	C2H							
WFEED2	Watchdog feed 2	C3H							

[1] All ports are in input only (high impedance) state after power-up.

[2] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and I xx11 0000.

[3] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset Other resets will not affect WDTOF.

[4] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[5] The only reset source that affects these SFRs is power-on reset.

Table 8. P89LPC913 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**
ACC*	Accumulator	E0H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	-	SRST	0	-
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**
B*	B register	F0H							
BRGR0[2]	Baud rate generator rate low	BEH							
BRGR1[2]	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	-
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H	-	-	-	-	-	-	
FMADRL	Program flash address low	E6H							
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1
FMDATA	Program flash data	E5H							
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
		Bit address	FF	FE	FD	FC	FB	FA	F9
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H							
KBPATN	Keypad pattern register	93H							
		Bit address	87	86	85	84	83	82	81
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2	
		Bit address	97	96	95	94	93	92	91
P1*	Port 1	90H			$\overline{\text{RST}}$				RXD
		Bit address	A7	A6	A5	A4	A3	A2	A1
P2*	Port 2	A0H			SPICLK		MISO	MOSI	
		Bit address	B7	B6	B5	B4	B3	B2	B1
P3*	Port 3	B0H							XTAL1
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)	
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)	
P1M1	Port 1 output mode 1	91H							(P1M1.1)
P1M2	Port 1 output mode 2	92H							(P1M2.1)
P2M1	Port 2 output mode 1	A4H			(P2M1.5)		(P2M1.3)	(P2M1.2)	
P2M2	Port 2 output mode 2	A5H			(P2M2.5)		(P2M2.3)	(P2M2.2)	
P3M1	Port 3 output mode 1	B1H							(P3M1.1)
P3M2	Port 3 output mode 2	B2H							(P3M2.1)
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial port data buffer register	99H							
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**
SCON	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-
SPDAT	SPI data register	E3H							
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses
			MSB
WDL	Watchdog load	C1H	
WFEED1	Watchdog feed 1	C2H	
WFEED2	Watchdog feed 2	C3H	

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any of them is written if BRGEN = 1, result is unpredictable

[3] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and I xx11 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[6] The only reset source that affects these SFRs is power-on reset.

Table 9. P89LPC914 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
AUXR1	Auxiliary function register	A2H	-	EBRR	-	ENT0	SRST	0	-
	Bit address		F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
BRGR0[2]	Baud rate generator rate low	BEH							
BRGR1[2]	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H	-	-	-	-	-	-	
FMADRL	Program flash address low	E6H							
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1
FMDATA	Program flash data	E5H							
	Bit address		AF	AE	AD	AC	AB	AA	A9
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0
	Bit address		EF	EE	ED	EC	EB	EA	E9
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI

Table 9. P89LPC914 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H							
KBPATN	Keypad pattern register	93H							
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H		CMP1/KB6	CMPREF/KB5	CIN1A/KB4		CIN2A/KB2	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H			$\overline{\text{RST}}$			T0	RXD
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**
P2*	Port 2	A0H			SPICLK	$\overline{\text{SS}}$	MISO	MOSI	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)	
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)	
P1M1	Port 1 output mode 1	91H						(P1M1.2)	(P1M1.1)
P1M2	Port 1 output mode 2	92H						(P1M2.2)	(P1M2.1)
P2M1	Port 2 output mode 1	A4H			(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	
P2M2	Port 2 output mode 2	A5H			(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD

Table 9. P89LPC914 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		D7	D6	D5	D4	D3	D2	D1
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial port data buffer register	99H							
	Bit address		9F	9E	9D	9C	9B	9A	99
SCON	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-
SPDAT	SPI data register	E3H							
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-
	Bit address		8F	8E	8D	8C	8B	8A	89
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1
TRIM	Internal oscillator trim register	96H	-	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF

Table 9. P89LPC914 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses
			MSB
WDL	Watchdog load	C1H	
WFEED1	Watchdog feed 1	C2H	
WFEED2	Watchdog feed 2	C3H	

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any of them is written if BRGEN = 1, result is unpredictable

[3] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and I xx11 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[6] The only reset source that affects these SFRs is power-on reset.

8.2 Enhanced CPU

The P89LPC912/913/914 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.3 Clocks

8.3.1 Clock definitions

The P89LPC912/913/914 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 10, 11, and 12) and can also be optionally divided to a slower frequency (see Section 8.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.3.2 CPU clock (OSCCLK)

The P89LPC912/913/914 provide user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator and an on-chip RC oscillator.

In addition, both the P89LPC912 and P89LPC913 provide an oscillator using an external crystal or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.3.3 Low-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.3.4 Medium-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.3.5 High-speed oscillator option (P89LPC912, P89LPC913)

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

8.3.6 Clock output (P89LPC912, P89LPC913)

The P89LPC912 supports a user selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC912. This output is enabled by the ENCLK bit in the TRIM register. The frequency of this clock output is ½ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.4 On-chip RC oscillator option

The P89LPC912/913/914 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz, ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

8.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.6 External clock input option (P89LPC912, P89LPC913)

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 12 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed, V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

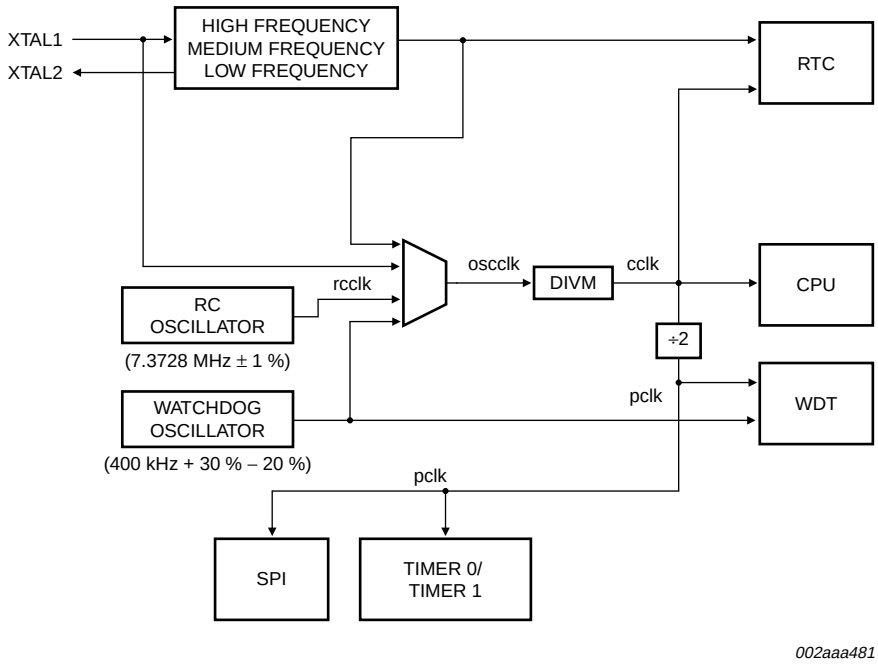


Fig 10. Block diagram of oscillator control (P89LPC912)

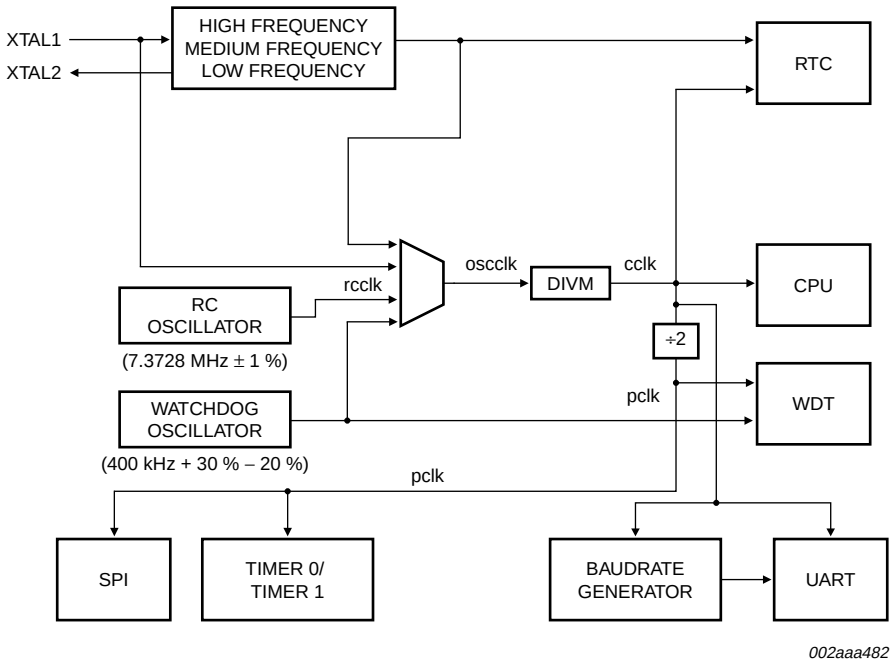


Fig 11. Block diagram of oscillator control (P89LPC913)

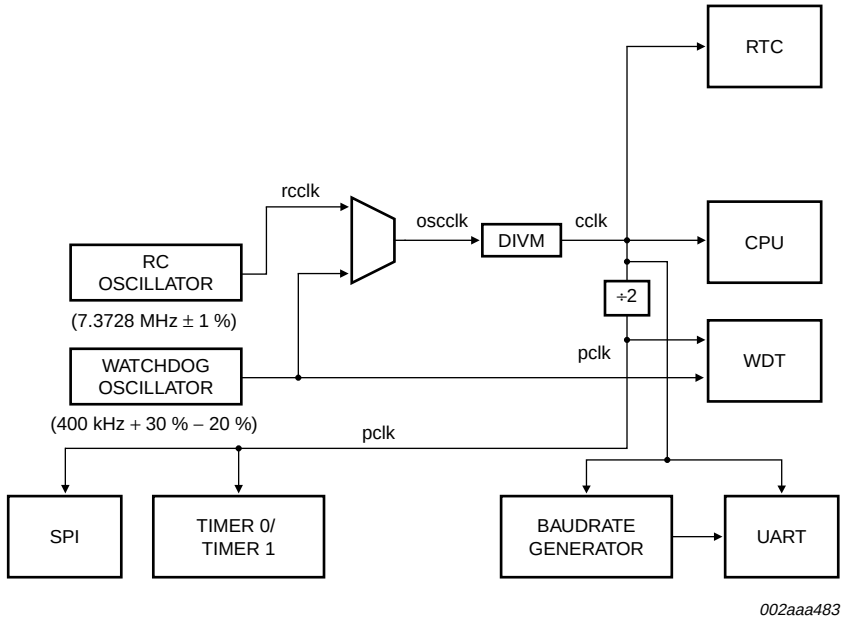


Fig 12. Block diagram of oscillator control (P89LPC914)

8.7 CCLK wake-up delay

The P89LPC912/913/914 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (P89LPC912, P89LPC913) the delay is 992 OSCCLK cycles plus 60 µs to 100 µs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 µs to 100 µs.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.9 Low power select

The P89LPC912 and P89LPC913 are designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.10 Memory organization

The various P89LPC912/913/914 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC912/913/914 has 1 kB of on-chip Code memory.

8.11 Interrupts

The P89LPC912/913/914 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources.

The P89LPC912 supports 7 interrupt sources: timers 0 and 1, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

The P89LPC913 and P89LPC914 devices support 10 interrupt sources: timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, Watchdog/Real-Time clock, keyboard, comparators 1 and 2, and SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC912/913/914 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC912/913/914 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

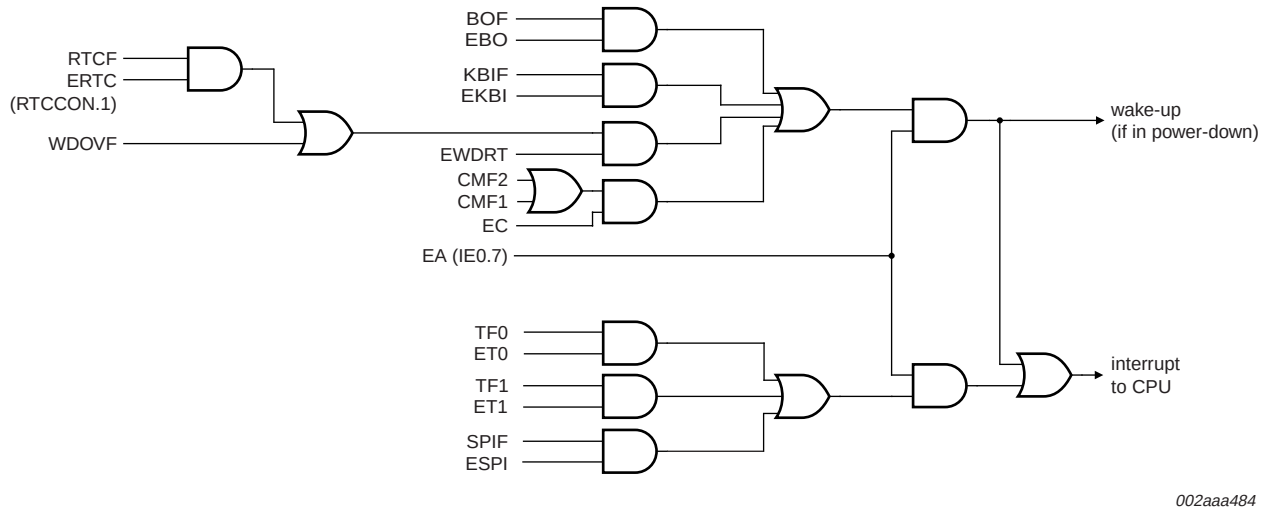


Fig 13. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC912)

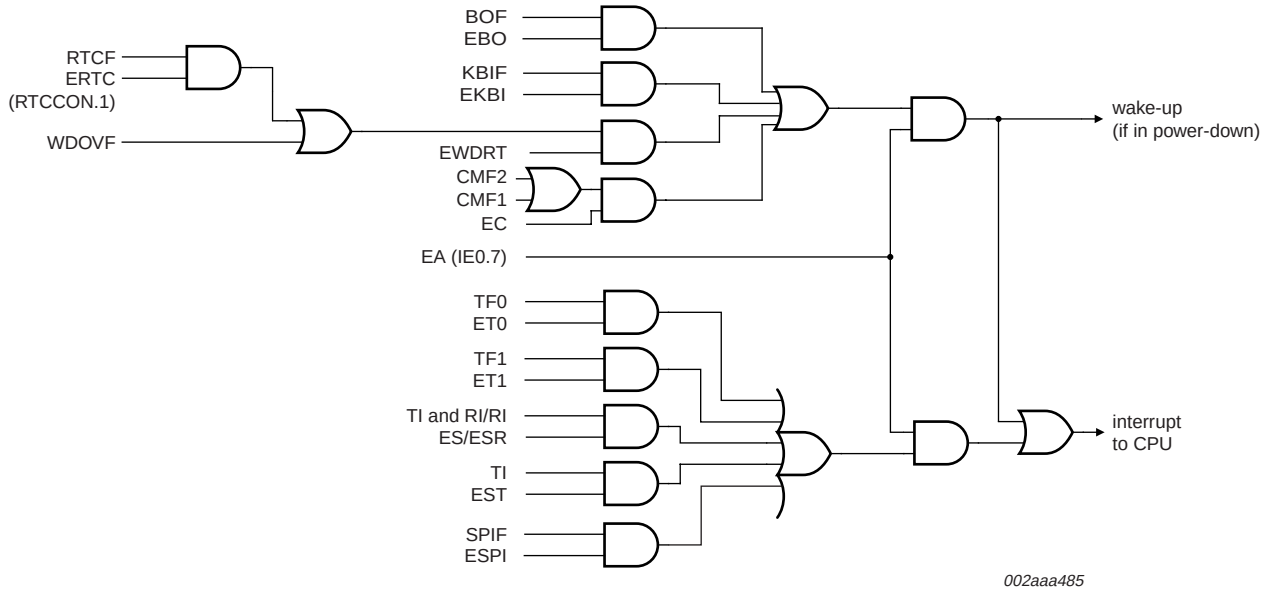


Fig 14. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC913, P89LPC914)

8.12 I/O ports

The P89LPC912 and P89LPC913 devices have 4 I/O ports: Port 0, Port 1, Port 2 and Port 3. The exact number of I/O pins available depends on the clock and reset options chosen, as shown in Table 10.

Table 10. Number of I/O pins available (P89LPC912, P89LPC913)

Clock source	Reset option	Number of I/O pins (14-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	12
	External $\overline{RST}$ pin supported	11
External clock input	No external reset (except during power-up)	11
	External $\overline{RST}$ pin supported	10
Low/medium/high-speed oscillator (external crystal or resonator)	No external reset (except during power-up)	10
	External $\overline{RST}$ pin supported[1]	9

[1] Required for operation above 12 MHz.

The P89LPC914 has three I/O ports: Port 0, Port 1, and Port 2. The exact number of I/O pins available depends upon the reset option chosen, as shown in Table 11.

Table 11. Number of I/O pins available (P89LPC914)

Reset option	Number of I/O pins (14-pin package)
No external reset (except during power-up)	12
External $\overline{RST}$ pin supported[1]	11

[1] Required for operation above 12 MHz.

8.12.1 Port configurations

Except as listed below, every I/O pin on the P89LPC912/913/914 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5/$\overline{RST}$ can only be an input and cannot be configured.

P1.2/T0 may only be configured to be either input-only or open drain (P89LPC912, P89LPC914).

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC912/913/914 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.6 Port 0 analog functions

The P89LPC912/913/914 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-only (high-impedance) mode as described in Section 8.12.4 “Input-only configuration”.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to logic 0s to enable digital functions.

8.12.7 Additional port features

After power-up, all pins are in Input-Only mode. After power-up all I/O pins except P1.5, may be configured by software.

- Pin P1.5 is input only.
- P1.2/T0 is configurable for either input-only or open-drain (P89LPC912, P89LPC914).

Every output on the P89LPC912/913/914 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 13 “Static characteristics” for detailed specifications.

All port pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC912/913/914 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

8.13.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however, it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 13 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC912/913/914 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 13 “Static characteristics” for specifications.

8.13.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC912/913/914 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and Total Power-down mode.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC912/913/914 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM data retention voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered-down separately), and RTC/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1. This option must be used for an oscillator frequency above 12 MHz.)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset (P89LPC913, P89LPC914).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16 Timers/counters 0 and 1

The P89LPC912/913/914 devices have two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. An option to automatically toggle the T0 pin upon timer overflow has been added (P89LPC912, P89LPC914). In the ‘Timer’ function, the register is incremented every machine cycle. In the ‘Counter’ function, the register of Timer 0 is incremented in response to a 1-to-0 transition at its external input pin, T0. This external input is sampled once very machine cycle.

Timer 0 has four operating modes (modes 0, 1, 2, and 3) on the P89LPC913).

Timer 0 has five operating modes (modes 0, 1, 2, 3, and 6 on the P89LPC912 and P89LPC914.

Timer 1 has four operating modes (modes 0, 1, 2, and 3) on all devices. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC912, P89LPC914)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output (P89LPC912, P89LPC914)

Timers 0 can be configured to automatically toggle the T0 output whenever a timer overflow occurs. The same device pins that are used for the T0 count input is also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 RTC/system timer

The P89LPC912/913/914 devices have a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set.

On the P89LPC914 the clock source for this counter is the CPU clock (CCLK). On the P89LPC912 and P89LPC913 devices, the clock source for this counter can either be the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source.

Only power-on reset will reset the RTC and its associated SFRs to the default state.

8.18 UART (P89LPC913, P89LPC914)

The P89LPC913 and P89LPC914 devices have an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC913 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CCLK/32 or CCLK/16.

8.18.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 "Baud rate generator and selection").

8.18.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CCLK frequency, as determined by the SMOD1 bit in PCON.

8.18.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in section Section 8.18.5 "Baud rate generator and selection").

8.18.5 Baud rate generator and selection

The P89LPC913 and P89LPC914 devices have an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 15). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses CCLK.

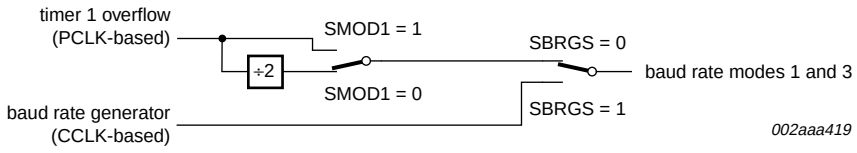


Fig 15. Baud rate sources for UART (Modes 1, 3)

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7, respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON[7:6]) are set up when SMOD0 is logic 0.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.18.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TX interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TX interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.19 Serial Peripheral Interface (SPI)

P89LPC912/913/914 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 4.5 Mbit/s can be supported in Master mode or 3 Mbit/s in Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

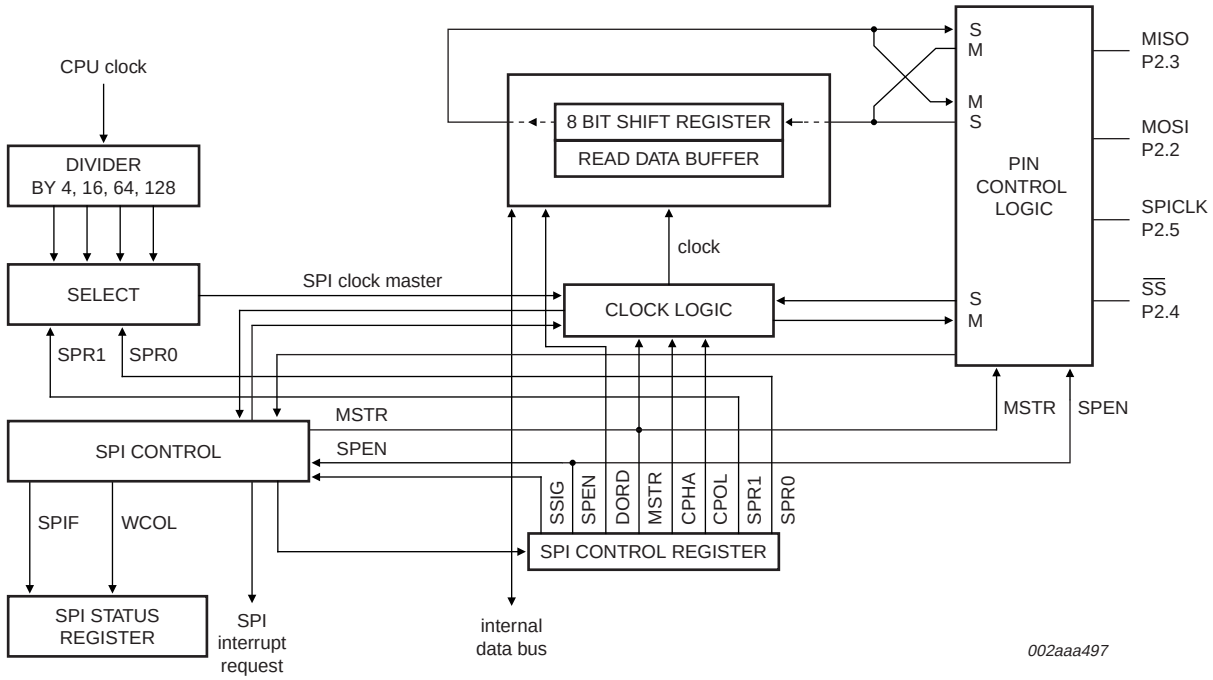


Fig 16. SPI block diagram (P89LPC912, P89LPC914)

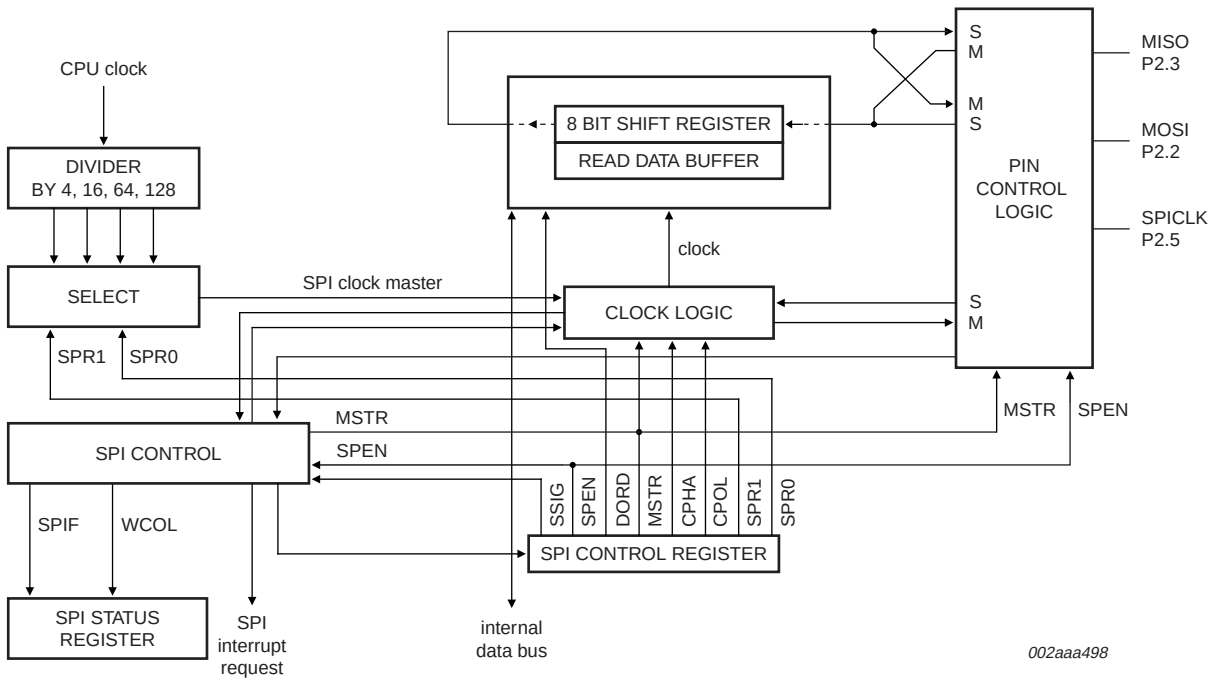


Fig 17. SPI block diagram (P89LPC913)

The SPI interface has four pins: SPICLK, MOSI, MISO, and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e. SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 18, 19, and 20.

- The P89LPC913 does not have the slave select pin, $\overline{SS}$. The SPI interface is set to Master mode and an I/O pin may be used to implement the $\overline{SS}$ function. Typical connections are shown in Figure 18 and Figure 19.

8.19.1 Typical SPI configurations

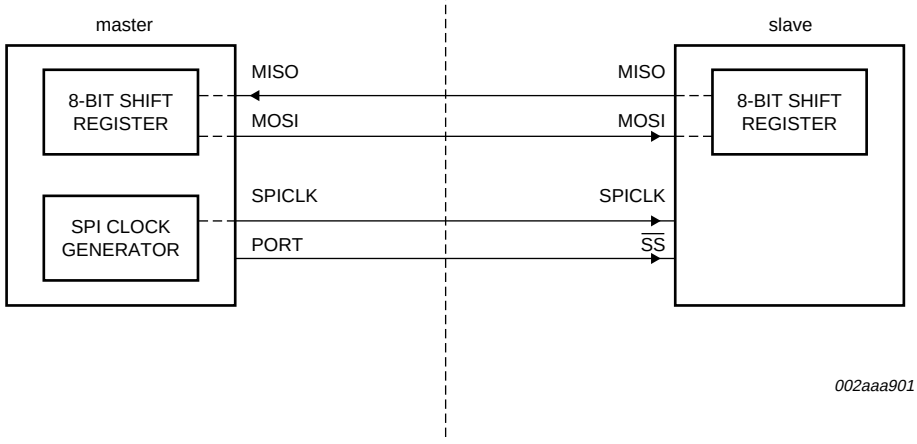


Fig 18. SPI single master single slave configuration

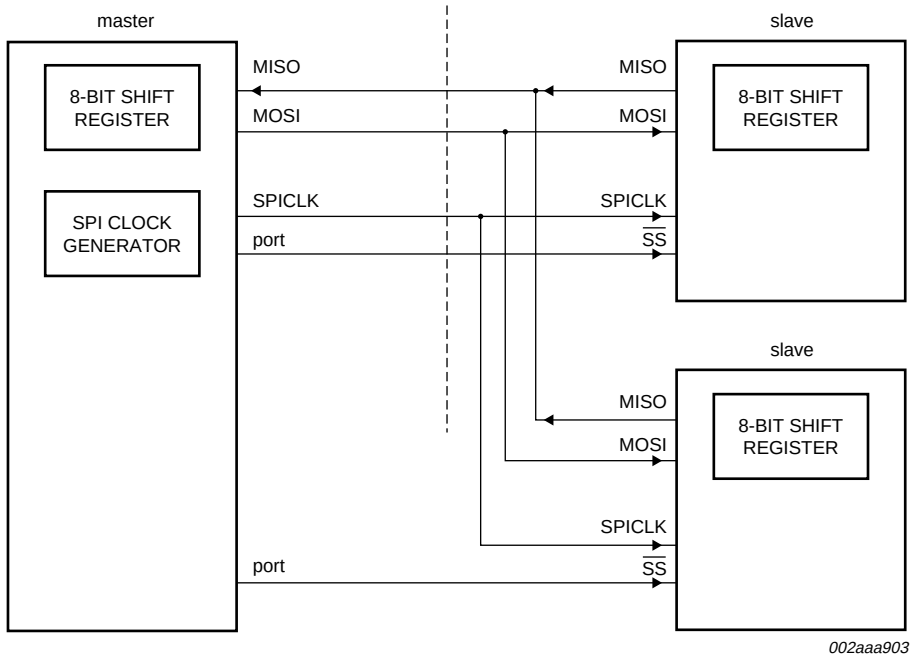


Fig 19. SPI single master multiple slaves configuration

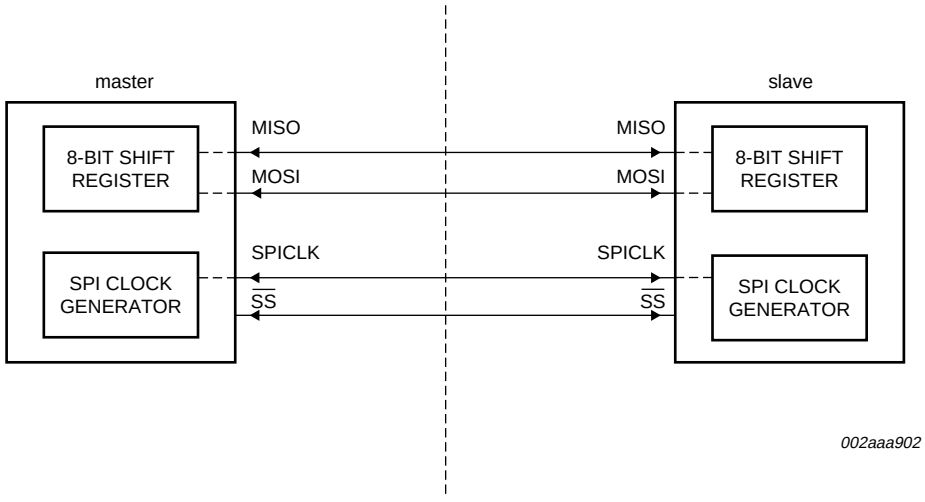


Fig 20. SPI dual device configuration, where either can be a master or a slave

8.20 Analog comparators

Two analog comparators are provided on the P89LPC912/913/914. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes. Comparator 1 may be output to a port pin.

The overall connections to both comparators are shown in Figure 21. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

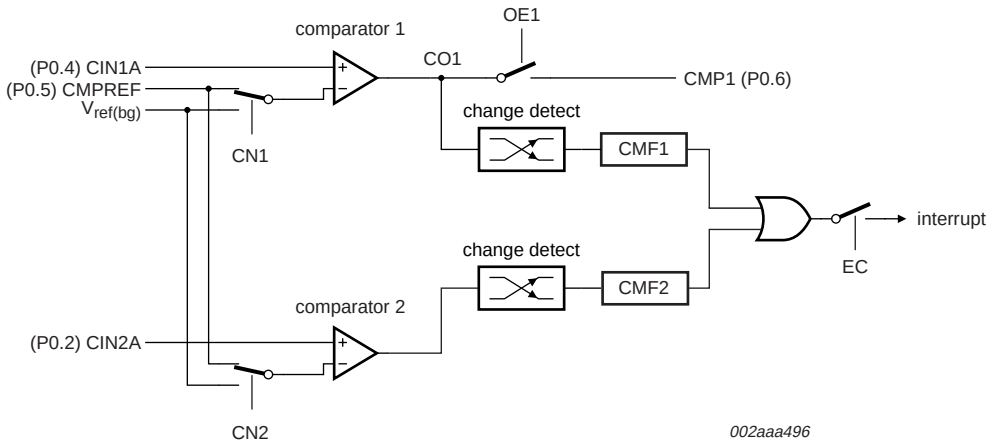


Fig 21. Comparator input and output connections

8.21 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 3 %.

8.22 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

Possible comparator configurations are shown in Figure 22.

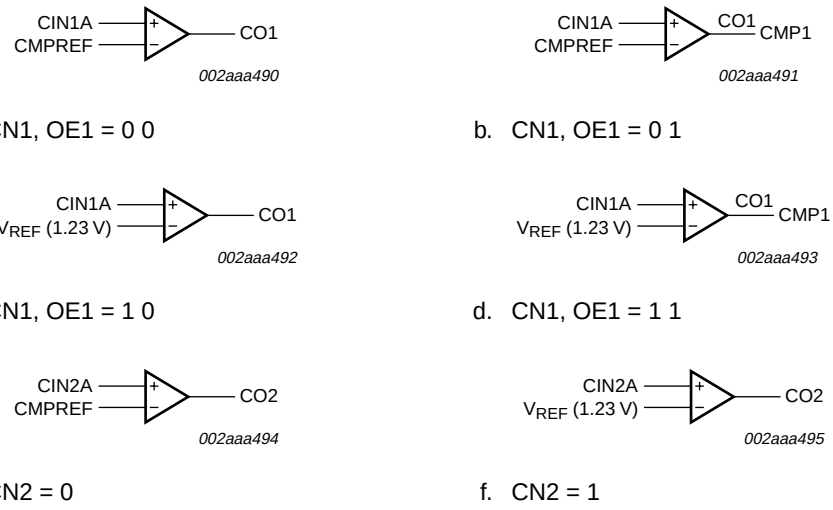


Fig 22. Comparator configurations

8.23 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.24 Keypad interrupt

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

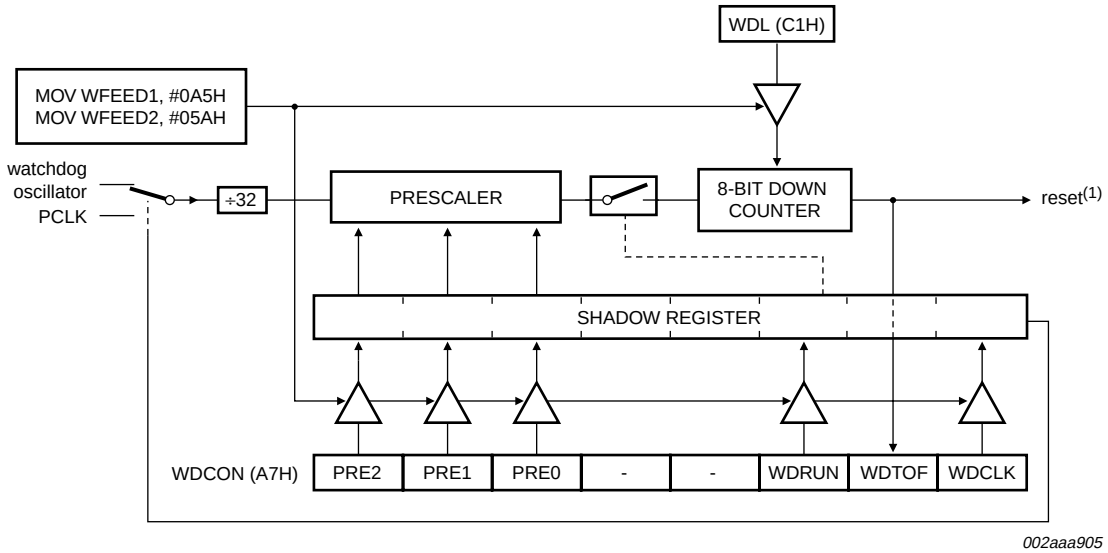
The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

8.25 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 23 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the P89LPC912/913/914 *User manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 23. Watchdog timer in Watchdog mode (WDTE = '1')

8.26 Additional features

8.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

8.27 Flash program memory

8.27.1 General description

The P89LPC912/913/914 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (256 B) or page (16 B). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC912/913/914 flash reliably stores memory contents even after 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC912/913/914 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.27.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 400000 typical erase/program cycles for each byte.
- 20 year minimum data retention.

8.27.3 Flash organization

The P89LPC912/913/914 program memory consists of four 256 byte sectors. Each sector can be further divided into 16 B pages. In addition to sector erase, page erase, and byte erase, a 16 B page register is included which allows from 1 B to 16 B of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable configuration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.27.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

8.27.5 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC912/913/914 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector (with V_{DD}, V_{SS}, $\overline{RST}$, clock, and data signals) needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP-Lite facility consists of internal hardware resources to facilitate programming and erasing. The NXP In-Application Programming Lite has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC912/913/914 *User manual*.

8.27.7 Using flash as data storage

The flash code memory array of this device supports **individual** byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.27.8 User configuration bytes

Some user-configurable features of the P89LPC912/913/914 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC912/913/914 *User manual* for additional details.

8.27.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the P89LPC912/913/914 *User manual* for additional details.

9. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 12 “Limiting values”:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 13. Static characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current						
	P89LPC912, P89LPC913	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	7	13	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	11	16	mA
	P89LPC914	V_{DD} = 3.6 V; f_{osc} = 7.373 MHz	[3]	-	4	8	mA
$I_{DD(idle)}$	Idle mode supply current						
	P89LPC912, P89LPC913	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	1.5	5.6	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	4	6	mA
	P89LPC914	V_{DD} = 3.6 V; f_{osc} = 7.373 MHz	[3]	-	1	3	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V	[2][3]	-	-	70	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V	[2][3]	-	0.5	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; all ports		-	0.6	1.0	V
		I_{OL} = 10 mA; all ports		-	0.3	0.5	V
		I_{OL} = 3.2 mA; all ports		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; all ports, push-pull mode		V_{DD} − 1.0	-	-	V
		I_{OH} = −3.2 mA; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 µA; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
C_{iss}	input capacitance		[4]	-	-	15	pF
I_{IL}	LOW-state input current	V_I = 0.4 V; all ports	[5]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$ or V_{IH}; all ports	[6]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	V_I = 2.0 V at V_{DD} = 3.6 V; all ports	[7][8]	−30	-	−450	µA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ

Table 13. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC912, P89LPC913).

[3] The $I_{DD(oper)}$, $I_{DD(idle)}$ and $I_{DD(pd)}$ specifications are measured with the following functions disabled: comparators, brownout detect, and watchdog timer (P89LPC914).

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

11. Dynamic characteristics

Table 14. Dynamic characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz	320	520	320	520	kHz
Crystal oscillator (P89LPC912, P89LPC913)							
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 25	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock (P89LPC912, P89LPC913)							
t_{CHCX}	clock HIGH time	see Figure 25	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 25	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 25	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 25	-	8	-	8	ns
Shift register (UART mode 0 - P89LPC913, P89LPC914)							
T_{XLXL}	serial port clock cycle time	see Figure 24	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 24	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 24	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 24	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge	see Figure 24	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	2.0 MHz (slave)		0	$^{CCLK}/_{6}$	0	2.0	MHz
	3.0 MHz (master)		-	$^{CCLK}/_{4}$	-	3.0	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 27, 28, 29					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns

Table 14. Dynamic characteristics *...continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 28, 29					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 28, 29					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 27, 28, 29					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 27, 28, 29					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 27, 28, 29	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 27, 28, 29	100	-	100	-	ns
t_{SPIA}	SPI access time						
	slave	see Figure 28, 29	0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 28, 29					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 27, 28, 29					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 27, 28, 29	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 27, 28, 29					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 27, 28, 29					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 15. Dynamic characteristics (P89LPC912, P89LPC913)

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Variable clock		f_{osc} = 18 MHz		Unit
				Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz		320	520	320	520	kHz
Crystal oscillator								
f_{osc}	oscillator frequency		[2]	0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 25		55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency			0	8	-	-	MHz
Glitch filter								
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin		-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin		125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock								
t_{CHCX}	clock HIGH time	see Figure 25		22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 25		22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 25		-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 25		-	5	-	5	ns
SPI interface								
f_{SPI}	SPI operating frequency							
	3.0 MHz (slave)			0	$^{CCLK}/_{6}$	0	3	MHz
	4.5 MHz (master)			-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 27, 28, 29						
	slave			$^{6}/_{CCLK}$	-	333	-	ns
	master			$^{4}/_{CCLK}$	-	222	-	ns

Table 15. Dynamic characteristics (P89LPC912, P89LPC913) *…continued*

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 28, 29					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 28, 29					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 27, 28, 29					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 27, 28, 29					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 27, 28, 29	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 27, 28, 29	100	-	100	-	ns
t_{SPIA}	SPI access time						
	slave	see Figure 28, 29	0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 28, 29					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 27, 28, 29					
	slave		0	160	-	160	ns
	master		0	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 27, 28, 29	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 27, 28, 29					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

Table 15. Dynamic characteristics (P89LPC912, P89LPC913) *…continued*

V_{DD} = 3.0 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
t_{SPIF}	SPI fall time	see Figure 26, 27, 28, 29					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

11.1 Waveforms

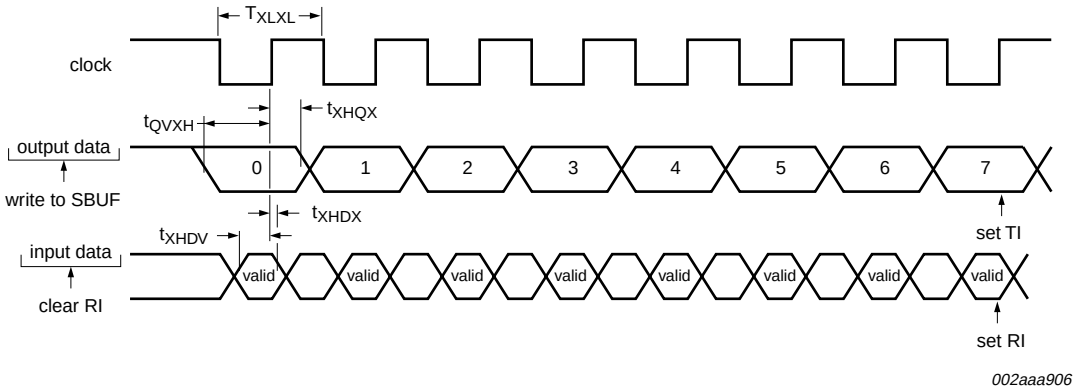


Fig 24. Shift register mode timing

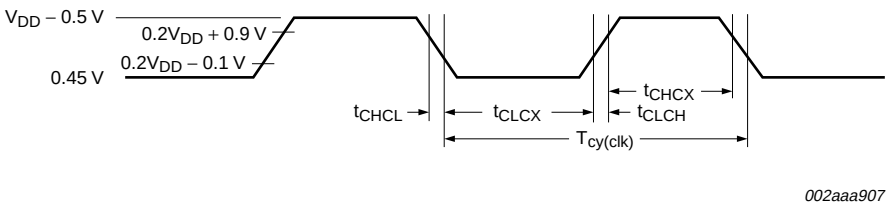


Fig 25. External clock timing

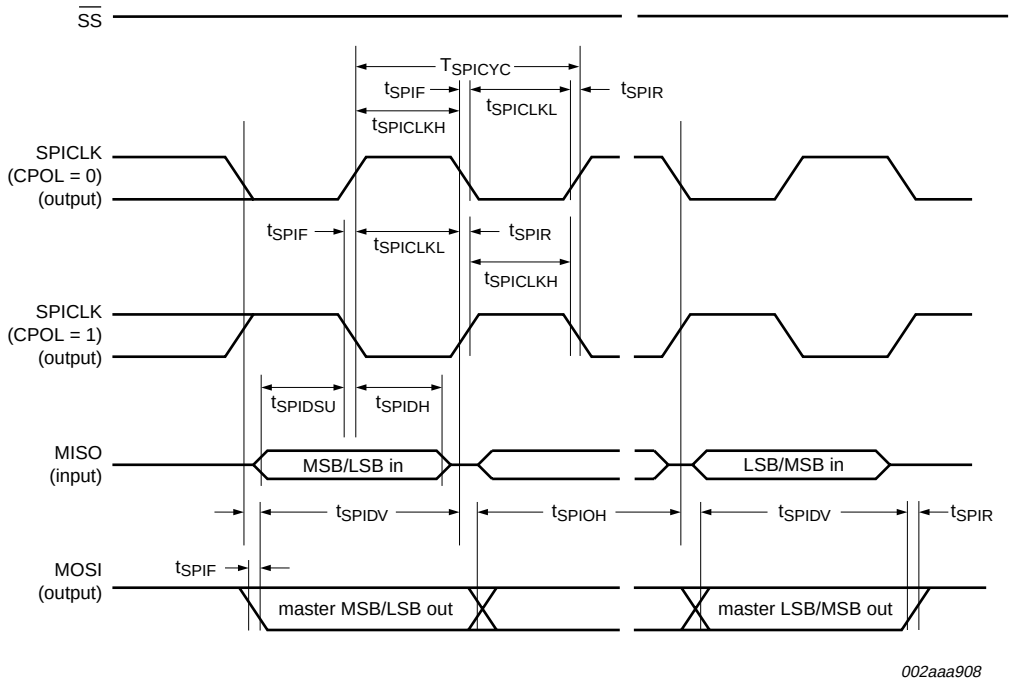


Fig 26. SPI master timing (CPHA = 0)

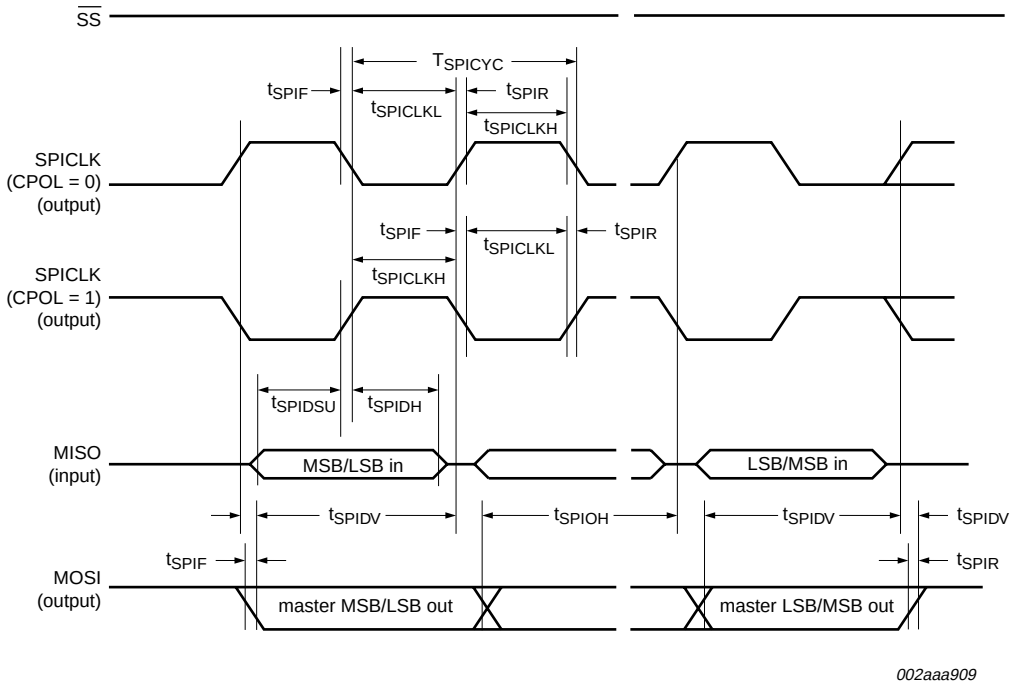


Fig 27. SPI master timing (CPHA = 1)

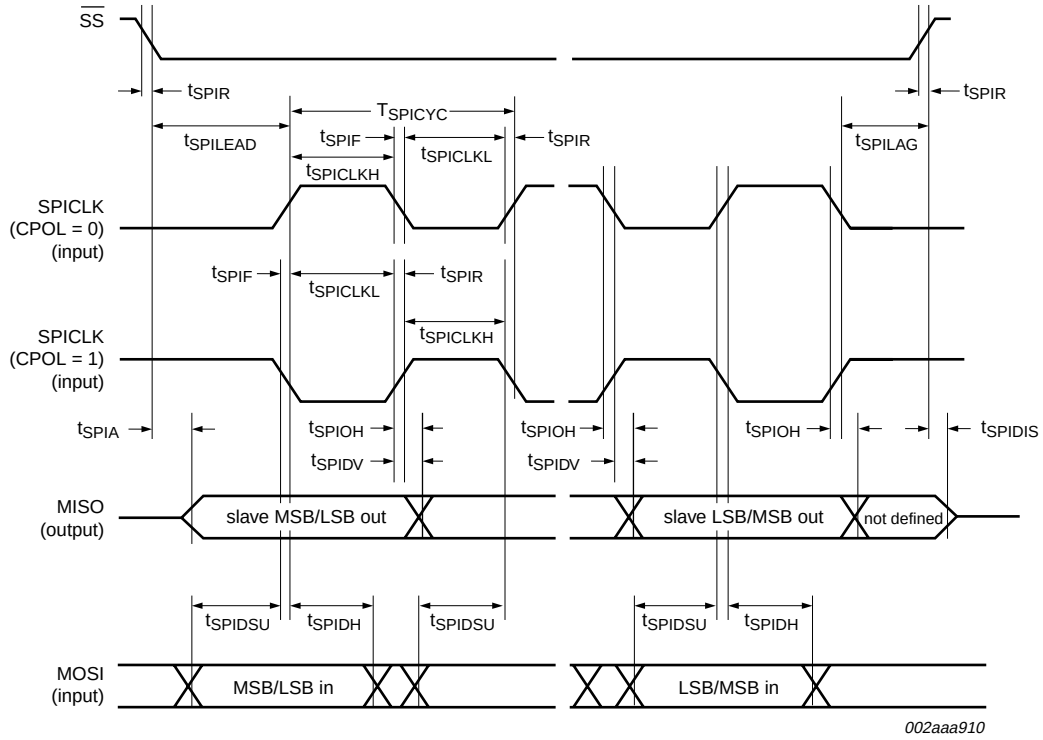


Fig 28. SPI slave timing (CPHA = 0)

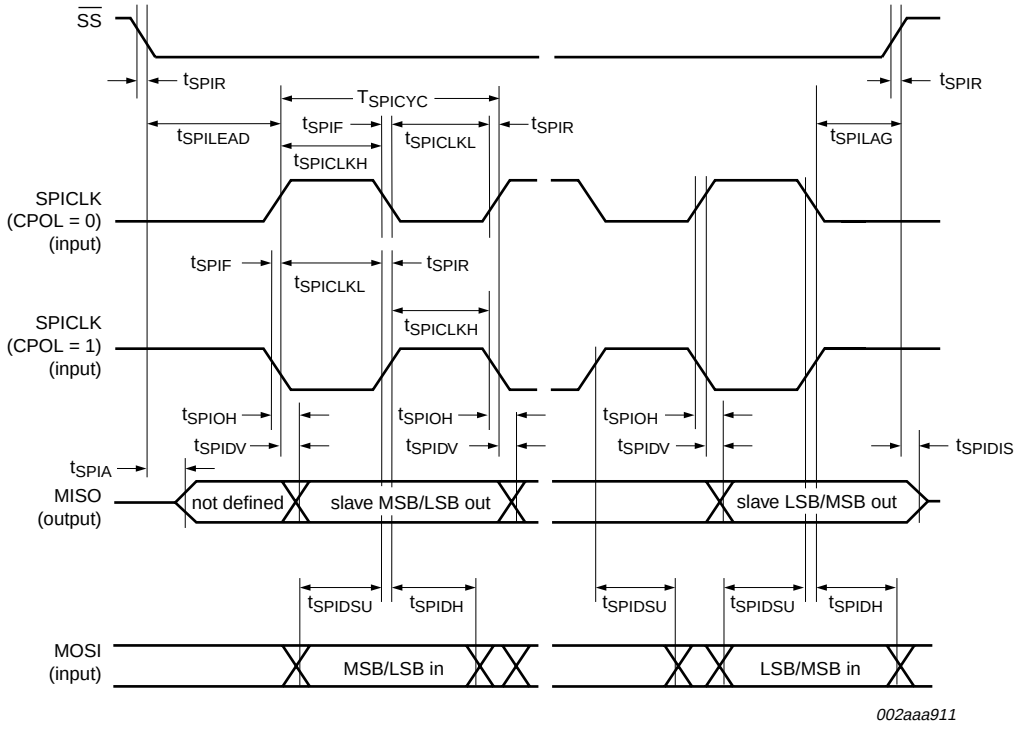


Fig 29. SPI slave timing (CPHA = 1)

12. Other characteristics

12.1 Comparator electrical characteristics

Table 16. Comparator electrical characteristics

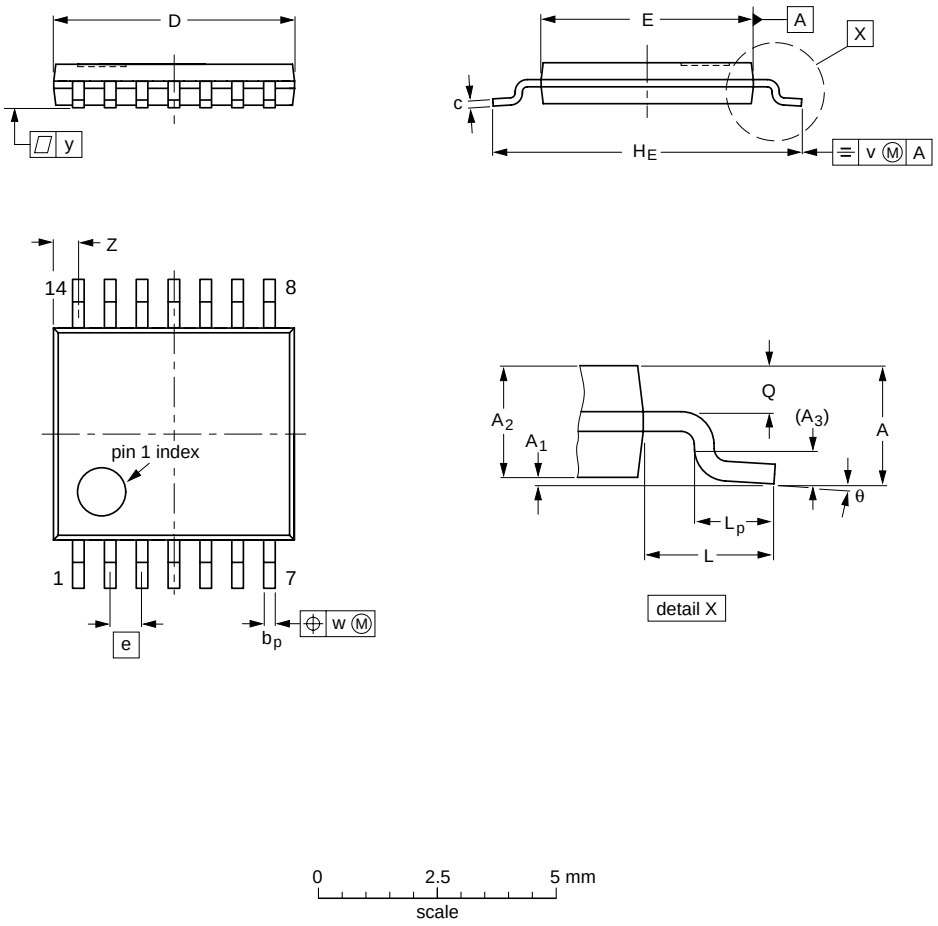
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±1	µA

[1] This parameter is characterized, but not tested in production.

13. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 30. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 17. Acronym list

Acronym	Description
CRC	Cyclic Redundancy Check
EPROM	Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
ISP	In-System Programming
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
RTC	Real-Time Clock
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC912_913_914_5	20070928	Product data sheet	-	P89LPC912_913_914_4
Modifications:	• Figure 10, 11 and 12: changed incorrect character font			
P89LPC912_913_914_4	20070830	Product data sheet	-	P89LPC912_913_914-03
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added P89LPC912HDH			
P89LPC912_913_914-03	20041217	Product data	-	P89LPC912_913_914-02
P89LPC912_913_914-02	20031212	Product data	01-A14930	P89LPC912_913_914-01
P89LPC912_913_914-01	20030711	Objective data	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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