# THE DATASHEET OF

# P87C51MC2BA/02,529

# P87C51MB2/P87C51MC2

80C51 8-bit microcontroller family with extended memory; 64 kB/96 kB OTP with 2 kB/3 kB RAM

**Rev. 03 — 13 November 2003** **Product data**

## 1. General description

The P87C51Mx2 represents the first microcontroller based on Philips Semiconductors' new 51MX core. The P87C51MC2 features 96 kbytes of OTP program memory and 3 kbytes of data SRAM, while the P87C51MB2 has 64 kbytes of OTP and 2 kbytes of RAM. In addition, both devices are equipped with a Programmable Counter Array (PCA), a watchdog timer that can be configured to different time ranges through SFR bits, as well as two enhanced UARTs and Serial Peripheral Interface (SPI).

Philips Semiconductors' 51MX (Memory eXtension) core is an accelerated 80C51 architecture that executes instructions at twice the rate of standard 80C51 devices. The linear address range of the 51MX has been expanded to support up to 8 Mbytes of program memory and 8 Mbytes of data memory. It retains full program code compatibility to enable design engineers to re-use 80C51 development tools, eliminating the need to move to a new, unfamiliar architecture. The 51MX core also retains 80C51 bus compatibility to allow for the continued use of 80C51-interfaced peripherals and Application Specific Integrated Circuits (ASICs).

The P87C51Mx2 provides greater functionality, increased performance and overall lower system cost. By offering an embedded memory solution combined with the enhancements to manage the memory extension, the P87C51Mx2 eliminates the need for software work-around. The increased program memory enables design engineers to develop more complex programs in a high-level language like C, for example, without struggling to contain the program within the traditional 64 kbytes of program memory. These enhancements also greatly improve C Language efficiency for code size below 64 kbytes.

The 51MX core is described in more detail in the *51MX Architecture Reference*.

## 2. Features

### 2.1 Key features

- Extended features of the 51MX Core:
  - 23-bit program memory space and 23-bit data memory space
  - Linear program and data address range expanded to support up to 8 Mbytes each
  - Program counter expanded to 23 bits
  - Stack pointer extended to 16 bits enabling stack space beyond the 80C51 limitation

PHILIPS

- New 23-bit extended data pointer and two 24-bit universal pointers greatly improve C compiler code efficiency in using pointers to access variables in different spaces

- 100% binary compatibility with the classic 80C51 so that existing code is completely reusable
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 kbytes (MC2) or 64 kbytes (MB2) of on-chip OTP
- 3 kbytes (MC2) or 2 kbytes (MB2) of on-chip RAM
- Programmable Counter Array (PCA)
- Two full-duplex enhanced UARTs and Serial Peripheral Interface (SPI) communication modules

## 2.2 Key benefits

- Increases program/data address range to 8 Mbytes each
- Enhances performance and efficiency for C programs
- Fully 80C51-compatible microcontroller
- Provides seamless and compelling upgrade path from classic 80C51
- Preserves 80C51 code base, investment/knowledge, and peripherals & ASICs
- Supported by wide range of 80C51 development systems and programming tools vendors
- The P87C51Mx2 makes it possible to develop applications at lower cost and with a reduced time-to-market

## 2.3 Complete features

- Fully static
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 kbytes or 64 kbytes of on-chip OTP
- 3 kbytes or 2 kbytes of on-chip RAM
- 23-bit program memory space and 23-bit data memory space
- Four-level interrupt priority
- 34 I/O lines (5 ports)
- Three Timers: Timer0, Timer1 and Timer2
- Two full-duplex enhanced UARTs with baud rate generator
- Framing error detection
- Automatic address recognition
- Supports industry-standard Serial Peripheral Interface (SPI) with a baud rate up to 6 Mbits/s
- Power control modes
- Clock can be stopped and resumed
- Idle mode
- Power down mode with advanced clock control
- Second DPTR register
- Asynchronous port reset
- Programmable Counter Array (PCA) (compatible with 8xC51Rx+) with five Capture/Compare modules

- Low EMI (inhibit ALE)
- Watchdog timer with programmable prescaler for different time ranges (compatible with 8xC66x with added prescaler)

## 3. Differences between P87C51MX2/02 part and previous revisions of P87C51MX2

The P87C51MX2/02 offers several advantages over the previous generation of P87C51MX2 parts. Right now, SPI module is available, two more general purpose digital pins on P4 are present and additional power control features are implemented (advanced peripheral clock control). New memory interface mode and code size optimization options are available with the use of MXCON register.

No changes are necessary when porting and loading code written for existing P87C51MX2 to the new P87C51MX2/02.

## 4. Ordering information

**Table 1: Ordering information**

| Type number | Memory | | Temp Range (°C) | $V_{DD}$ voltage range | Frequency | | Package | | |
|---|---|---|---|---|---|---|---|---|---|
| | OTP | RAM | | | $V_{DD}$ = 2.7 to 5.5 V | $V_{DD}$ = 4.5 to 5.5 V | Name | Description | Version |
| P87C51MB2BA/02 | 64 kB | 2048 B | 0 to +70 | 2.7 to 5.5 V | 0 to 12 MHz | 0 to 24 MHz | PLCC44 | plastic leaded chip carrier; 44 leads | SOT187-2 |
| P87C51MC2BA/02 | 96 kB | 3072 B | 0 to +70 | 2.7 to 5.5 V | 0 to 12 MHz | 0 to 24 MHz | PLCC44 | plastic leaded chip carrier; 44 leads | SOT187-2 |

## 5. Block diagram

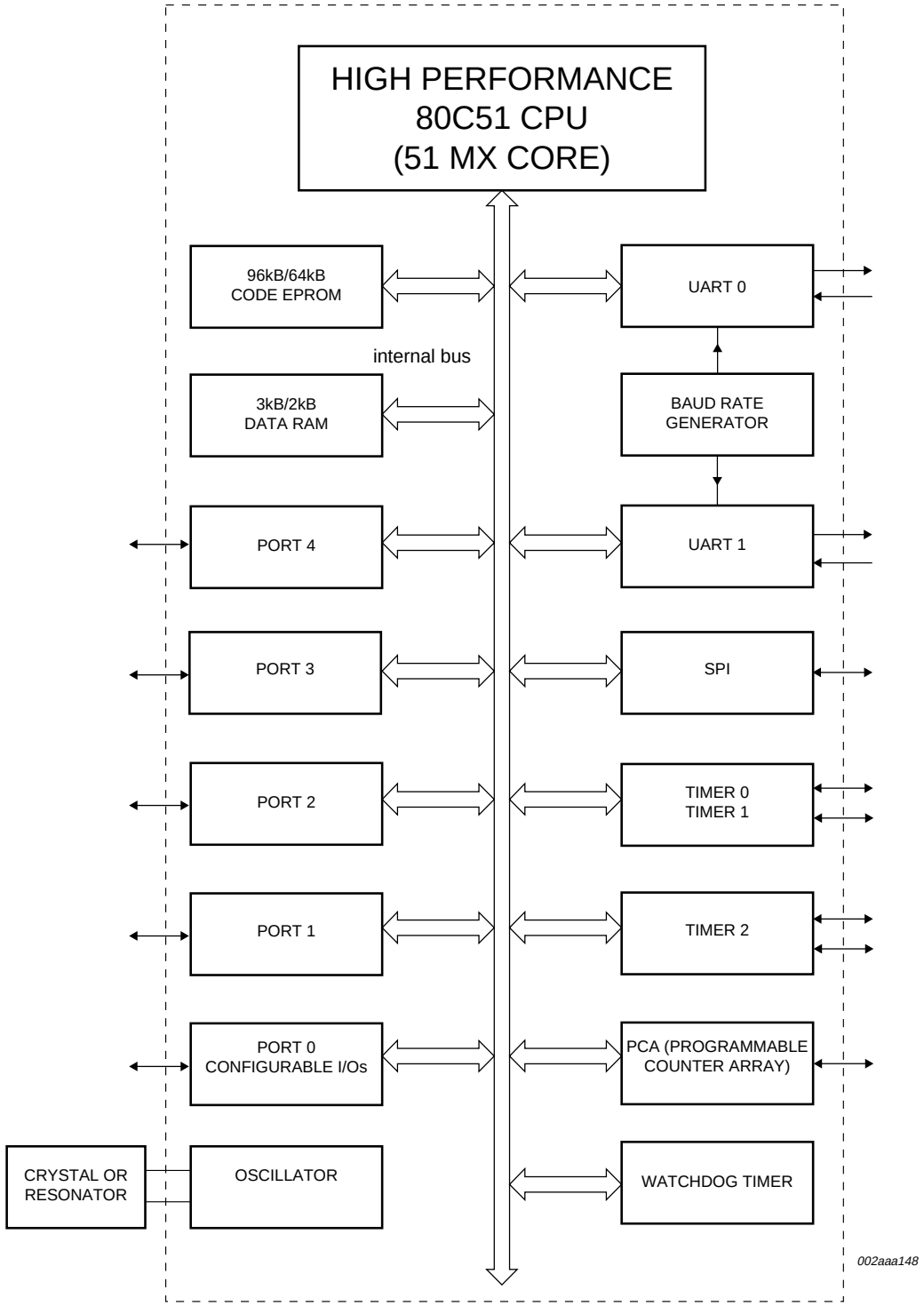



**Fig 1. Block diagram.**

## 6. Functional diagram

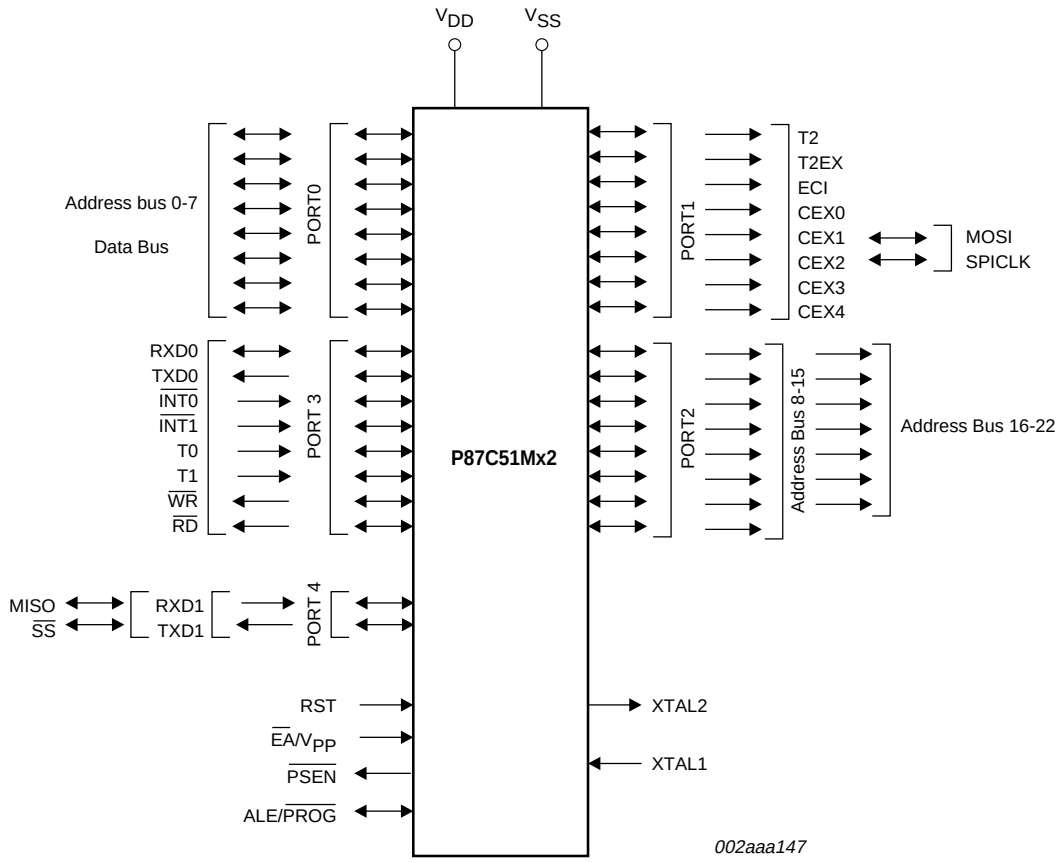



**Fig 2. Functional diagram.**

# 7. Pinning information

## 7.1 Pinning

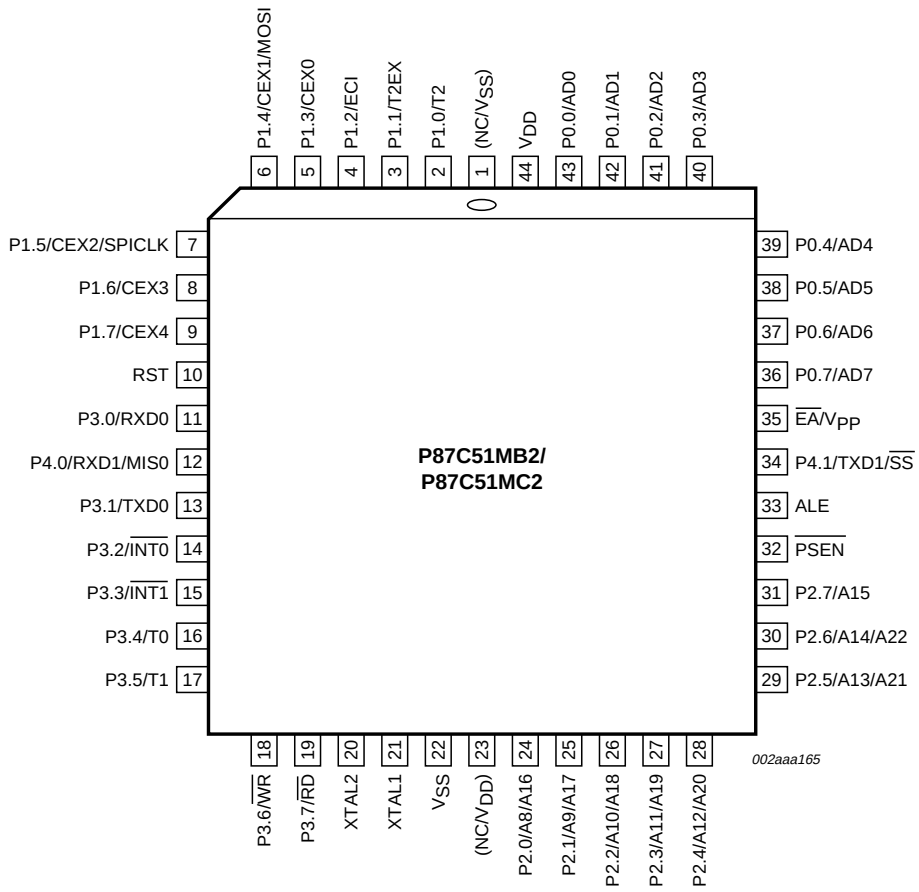



**Fig 3. Pinning.**

## 7.2 Pin description

**Table 2: Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0.0 - P0.7 | 43 - 36 | I/O | **Port 0:** Port 0 is an open drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. |
| P1.0 - P1.7 | 2 - 9 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled LOW will source current because of the internal pull-ups. |
| | 2 | I/O | • **P1.0, T2**<br>– Timer/Counter 2 external count input/Clock out |
| | 3 | I | • **P1.1, T2EX**<br>– Timer/Counter 2 Reload/Capture/Direction Control |
| | 4 | I | • **P1.2, ECI**<br>– External Clock Input to the PCA |
| | 5 | I/O | • **P1.3, CEX0**<br>– Capture/Compare External I/O for PCA module 0 |
| | 6 | I/O | • **P1.4, CEX1**<br>– Capture/Compare External I/O for PCA module 1 (with pull-up on pin) |
| | | I/O | • **MOSI**<br>– SPI Master Out/Slave In (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled) |
| | 7 | I/O | • **P1.5, CEX2**<br>– Capture/Compare External I/O for PCA module 2 (with pull-up on pin) |
| | | I/O | • **SPICLK**<br>– SPI Clock (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled) |
| | 8 | I/O | • **P1.6, CEX3**<br>– Capture/Compare External I/O for PCA module 3 |
| | 9 | I/O | • **P1.7, CEX4**<br>– Capture/Compare External I/O for PCA module |

**Table 2: Pin description**...*continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P2.0 - P2.7 | 24 - 31 | I/O | **Port 2:** Port 2 is a 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 2 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled LOW will source current because of the internal pull-ups. (See Section 10 "Static characteristics", $I_{IL}$). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR) or 23-bit addresses (MOVX @EPTR, EMOV). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @ Ri), port 2 emits the contents of the P2 Special Function Register.<br>Note that when 23-bit address is used, address bits A16-A22 will be outputted to P2.0-P2.6 when ALE is HIGH, and address bits A8-A14 are outputted to P2.0-P2.6 when ALE is LOW. Address bit A15 is outputted on P2.7 regardless of ALE. |
| P3.0 - P3.7 | 11,13 -19 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled LOW will source current because of the internal pull-ups. |
| | 11 | I | • **P3.0, RXD0**<br>– Serial input port 0 |
| | 13 | O | • **P3.1, TXD0**<br>– Serial output port 0 |
| | 14 | I | • **P3.2, INT0**<br>– External interrupt 0 |
| | 15 | I | • **P3.3, INT1**<br>– External interrupt 1 |
| | 16 | I | • **P3.4, T0**<br>– Timer0 external input |
| | 17 | I | • **P3.5, T1**<br>– Timer1 external input |
| | 18 | O | • **P3.6, $\overline{WR}$**<br>– External data memory write strobe |
| | 19 | O | • **P3.7, $\overline{RD}$**<br>– External data memory read strobe |
| P4.0 - P4.1 | 12,34 | I/O | **Port 4:** Port 4 is an 2-bit bidirectional I/O port with internal pull-ups on all pins. Port 4 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. (Note: When SPEN, i.e.,SPCTL.6, is '1', the pull-ups at these port pins are disabled.) |
| | 12 | I | • **P4.0, RXD1**<br>– Serial input port 1 (with pull-up on pin) |
| | | I/O | • **MISO**<br>– SPI Master In/Slave Out (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled) |

**Table 2: Pin description**...*continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| | 34 | O | • **P4.1, TXD1**<br>– Serial output port 1 (with pull-up on pin) |
| | | I/O | • **$\overline{SS}$**<br>– SPI Slave Select (Selected when SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled) |
| RST | 10 | I | **Reset:** A HIGH on this pin for two machine cycles, while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{DD}$. |
| ALE | 33 | O | **Address Latch Enable:** Output pulse for latching the LOW byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR AUXR.0. With this bit is set, ALE will be active only during a MOVX/EMOV/MOVC instruction. |
| $\overline{PSEN}$ | 32 | O | **Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. |
| $\overline{EA}/V_{PP}$ | 35 | I | **External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations. If $\overline{EA}$ is held HIGH, the device executes from internal program memory. The value on the $\overline{EA}$ pin is latched when RST is released and any subsequent changes have no effect. |
| XTAL1 | 21 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 20 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |
| $V_{SS}$ | 22 | I | **Ground:** 0 V reference. |
| $V_{DD}$ | 44 | I | **Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power Down modes. |
| ($NC/V_{SS}$) | 1 | I | **No Connect/Ground:** This pin is internally connected to $V_{SS}$ on the P87C51MB2/MC2. If connected externally, this pin must only be connected to the same $V_{SS}$ as at pin 22. (Note: Connecting the second pair of $V_{SS}$ and $V_{DD}$ pins is not required. However, they may be connected in addition to the primary $V_{SS}$ and $V_{DD}$ pins to improve power distribution, reduce noise in output signals, and improve system-level EMI characteristics.) |
| ($NC/V_{DD}$) | 23 | I | **No Connect/Power Supply:** This pin is internally connected to $V_{DD}$ on the P87C51MB2/MC2. If connected externally, this pin must only be connected to the same $V_{DD}$ as at pin 44. (Note: Connecting the second pair of $V_{SS}$ and $V_{DD}$ pins is not required. However, they may be connected in addition to the primary $V_{SS}$ and $V_{DD}$ pins to improve power distribution, reduce noise in output signals, and improve system-level EMI characteristics.) |

# 8. Functional description

## 8.1 Memory arrangement

P87C51MB2 has 64 kbytes of OTP (MX universal map range: 80:0000-80:FFFF), while P87C51MC2 has 96 kbytes of OTP (MX universal map range: 80:0000-81:7FFF).

The P87C51MB2 and P87C51MC2 have 2 kbytes and 3 kbytes of on-chip RAM respectively:

**Table 3: Memory arrangement**

| Data memory | | Size (bytes) and MX universal memory map range | |
|---|---|---|---|
| **Type** | **Description** | **P87C51MB2** | **P87C51MC2** |
| DATA | memory that can be addressed both directly and indirectly; can be used as stack | 128 (7F:0000-7F:007F) | 128 (7F:0000-7F:001F) |
| IDATA | superset of DATA; memory that can be addressed indirectly (where direct address for upper half is for SFR only); can be used as stack | 256 (7F:0000-7F:00FF) | 256 (7F:0000-7F:00FF) |
| EDATA | superset of DATA/IDATA; memory that can be addressed indirectly using Universal Pointers (PR0,1); can be used as stack | 512 (7F:0000-7F:01FF) | 512 (7F:0000-7F:01FF) |
| XDATA | memory (on-chip 'External Data') that is accessed via the MOVX/EMOV instructions using DPTR/EPTR | 1536 (00:0000-00:05FF) | 2560 (00:0000-00:09FF) |

For more detailed information, please refer to the *P87C51Mx2 User Manual* or the *51MX Architecture Specification*.

## 8.2 Special Function Registers

Special Function Register (SFR) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0', or '1' can **only** be written and read as follows:
  - '-' MUST be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' MUST be written with '0', and will return a '0' when read.
  - '1' MUST be written with '1', and will return a '1' when read.

9397 750 12302

**Table 4: Special Function Registers**

| Name | Description | SFR Addr. | Bit functions and addresses | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | |
| | | Bit address | E7 | E6 | E5 | E4 | E3 | E2 | E1 |
| ACC [1] | Accumulator | E0H | | | | | | | |
| AUXR [2] | Auxiliary Function Register | 8EH | - | - | - | - | - | - | EX |
| AUXR1 [2] | Auxiliary Function Register 1 | A2H | - | - | - | LPEP | GF2 | 0 | - |
| | | Bit address | F7 | F6 | F5 | F4 | F3 | F2 | F1 |
| B [1] | B Register | F0H | | | | | | | |
| BRGCON [2] | Baud Rate Generator Control | 85H [3] | - | - | - | - | - | - | SC |
| BRGR0 [2][5] | Baud Rate Generator Rate LOW | 86H [3] | | | | | | | |
| BRGR1 [2][5] | Baud Rate Generator Rate HIGH | 87H [3] | | | | | | | |
| CCAP0H [2] | Module 0 Capture HIGH | FAH | | | | | | | |
| CCAP1H [2] | Module 1 Capture HIGH | FBH | | | | | | | |
| CCAP2H [2] | Module 2 Capture HIGH | FCH | | | | | | | |
| CCAP3H [2] | Module 3 Capture HIGH | FDH | | | | | | | |
| CCAP4H [2] | Module 4 Capture HIGH | FEH | | | | | | | |
| CCAP0L [2] | Module 0 Capture LOW | EAH | | | | | | | |
| CCAP1L [2] | Module 1 Capture LOW | EBH | | | | | | | |
| CCAP2L [2] | Module 2 Capture LOW | ECH | | | | | | | |
| CCAP3L [2] | Module 3 Capture LOW | EDH | | | | | | | |
| CCAP4L [2] | Module 4 Capture LOW | EEH | | | | | | | |
| CCAPM0 [2] | Module 0 Mode | DAH | - | ECOM_0 | CAPP_0 | CAPN_0 | MAT_0 | TOG_0 | PW |
| CCAPM1 [2] | Module 1 Mode | DBH | - | ECOM_1 | CAPP_1 | CAPN_1 | MAT_1 | TOG_1 | PW |
| CCAPM2 [2] | Module 2 Mode | DCH | - | ECOM_2 | CAPP_2 | CAPN_2 | MAT_2 | TOG_2 | PW |
| CCAPM3 [2] | Module 3 Mode | DDH | - | ECOM_3 | CAPP_3 | CAPN_3 | MAT_3 | TOG_3 | PW |
| CCAPM4 [2] | Module 4 Mode | DEH | - | ECOM_4 | CAPP_4 | CAPN_4 | MAT_4 | TOG_4 | PW |
| | | Bit address | DF | DE | DD | DC | DB | DA | D9 |
| CCON [1] [2] | PCA Counter Control | D8H | CF | CR | - | CCF4 | CCF3 | CCF2 | CC |
| CH [2] | PCA Counter HIGH | F9H | | | | | | | |
| CL [2] | PCA Counter LOW | E9H | | | | | | | |
| CMOD [2] | PCA Counter Mode | D9H | CIDL | WDTE | - | - | - | CPS1 | CI |

9397 750 12302

**Table 4: Special Function Registers** *...continued*

| Name | Description | SFR Addr. | Bit functions and addresses | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | |
| DPTR | Data Pointer (2 bytes) | | | | | | | | |
| DPH | Data Pointer HIGH | 83H | | | | | | | |
| DPL | Data Pointer LOW | 82H | | | | | | | |
| EPTR | Extended Data Pointer (3 bytes) | | | | | | | | |
| EPL [2] | Extended Data Pointer LOW | FCH[3] | | | | | | | |
| EPM [2] | Extended Data Pointer Middle | FDH[3] | | | | | | | |
| EPH [2] | Extended Data Pointer HIGH | FEH[3] | | | | | | | |
| | | **Bit address** | **AF** | **AE** | **AD** | **AC** | **AB** | **AA** | **A** |
| IEN0 [1] | Interrupt Enable 0 | A8H | $\overline{EA}$ | EC | ET2 | ES0/ ES0R | ET1 | EX1 | E |
| | | **Bit address** | **EF** | **EE** | **ED** | **EC** | **EB** | $\overline{EA}$ | **E** |
| IEN1 [1] | Interrupt Enable 1 | E8H | - | - | - | - | ESPI | ES1T | E |
| | | **Bit address** | **BF** | **BE** | **BD** | **BC** | **BB** | **BA** | **B** |
| IP0 [1] | Interrupt Priority | B8H | - | PPC | PT2 | PS0/ PS0R | PT1 | PX1 | P |
| IP0H | Interrupt Priority 0 HIGH | B7H | - | PPCH | PT2H | PS0H/ PS0RH | PT1H | PX1H | P |
| | | **Bit address** | **FF** | **FE** | **FD** | **FC** | **FB** | **FA** | **F** |
| IP1 [1] | Interrupt Priority 1 | F8H | - | - | - | - | PSPI | PS1T | P |
| IP1H | Interrupt Priority 1 HIGH | F7H | - | - | - | - | PSPIH | PS1TH | P |
| MXCON [2] | MX Control Register | FFH[3] | - | - | - | ECRM | EAM1 | EAM0 | E |
| | | **Bit address** | **87** | **86** | **85** | **84** | **83** | **82** | **8** |
| P0 [1] | Port 0 | 80H | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | A |
| | | | 97 | 96 | 95 | 94 | 93 | 92 | 9 |
| P1 [1] | Port 1 | 90H | CEX4 | CEX3 | CEX2/ SPICLK | CEX1/ MOSI | CEX0 | ECI | $\overline{T}$ |

9397 750 12302

**Table 4: Special Function Registers** *...continued*

| Name | Description | SFR Addr. | Bit functions and addresses | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | |
| | | Bit address | A7 | A6 | A5 | A4 | A3 | A2 | A |
| P2[1] | Port 2 | A0H | AD15 | AD14/ AD22 | ADA13/ AD21 | AD12/ AD20 | AD11/ AD19 | AD10/ AD18 | AI AI |
| | | Bit address | B7 | B6 | B5 | B4 | B3 | B2 | B |
| P3[1] | Port 3 | B0H | $\overline{RD}$ | $\overline{WR}$ | T1 | T0 | $\overline{INT1}$ | $\overline{INT0}$ | Tx |
| | | Bit address | C7[3] | C6[3] | C5[3] | C4[3] | C3[3] | C2[3] | C |
| P4[1][2] | Port 4 | C0H[3] | - | - | - | - | - | - | Tx SS |
| PCON[2] | Power Control Register | 87H | SMOD1 | SMOD0 | - | POF | GF1 | GF0 | PI |
| PCONA[2] | Power Control Register A | B5H | - | PCAPD | - | SPIPD | BRGPD | T2PD | S1 |
| | | Bit address | D7 | D6 | D5 | D4 | D3 | D2 | D |
| PSW[1] | Program Status Word | D0H | CY | AC | F0 | RS1 | RS0 | OV | F1 |
| RCAP2H[2] | Timer2 Capture HIGH | CBH | | | | | | | |
| RCAP2L[2] | Timer2 Capture LOW | CAH | | | | | | | |
| | | Bit address | 9F | 9E | 9D | 9C | 9B | 9A | 99 |
| S0CON[1] | Serial Port 0 Control | 98H | SM0_0/ FE_0 | SM1_0 | SM2_0 | REN_0 | TB8_0 | RB8_0 | TI |
| S0BUF | Serial Port 0 Data Buffer Register | 99H | | | | | | | |
| S0ADDR | Serial Port 0 Address Register | A9H | | | | | | | |
| S0ADEN | Serial Port 0 Address Enable | B9H | | | | | | | |
| S0STAT[2] | Serial Port 0 Status | 8CH[3] | DBMOD_0 | INTLO_0 | CIDIS_0 | DBISEL_ 0 | FE_0 | BR_0 | O |
| | | Bit address | 87[3] | 86[3] | 85[3] | 84[3] | 83[3] | 82[3] | 81 |
| S1CON[1][2] | Serial Port 1 Control | 80H[3] | SM0_1/ FE_1 | SM1_1 | SM2_1 | REN_1 | TB8_1 | RB8_1 | TI |
| S1BUF[2] | Serial Port 1 Data buffer Register | 81H[3] | | | | | | | |
| S1ADDR[2] | Serial Port 1 Address Register | 82H[3] | | | | | | | |
| S1ADEN[2] | Serial Port 1 Address Enable | 83H[3] | | | | | | | |

9397 750 12302

**Table 4: Special Function Registers** *...continued*

| Name | Description | SFR Addr. | Bit functions and addresses | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | |
| S1STAT [2] | Serial Port 1 Status | 84H[3] | DBMOD_1 | INTLO_1 | CIDIS_1 | DBISEL1 | FE_1 | BR_1 | O |
| SPCTL [2] | SPI Control Register | E2H | SSIG | SPEN | DORD | MSTR | CPOL | CPHA | PS |
| SPCFG [2] | SPI Configuration Register | E1H | SPIF | SPWCOL | - | - | - | - | - |
| SPDAT [2] | SPI Data | E3H | | | | | | | |
| SP | Stack Pointer (or Stack Pointer LOW Byte When EDATA Supported) | 81H | | | | | | | |
| SPE [2] | Stack Pointer HIGH | FBH[3] | | | | | | | |
| | | Bit address | 8F | 8E | 8D | 8C | 8B | 8A | 89 |
| TCON [1] | Timer Control Register | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE |
| | | | CF | CE | CD | CC | CB | CA | C9 |
| T2CON [1] [2] | Timer2 Control Register | C8H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | CA |
| T2MOD [2] | Timer2 Mode Control | C9H | - | - | ENT2 | TF2DE | T2GATE | T2PWME | T2 |
| TH0 | Timer 0 HIGH | 8CH | | | | | | | |
| TH1 | Timer 1 HIGH | 8DH | | | | | | | |
| TH2 | Timer 2 HIGH | CDH | | | | | | | |
| TL0 | Timer 0 LOW | 8AH | | | | | | | |
| TL1 | Timer 1 LOW | 8BH | | | | | | | |
| TL2 | Timer 2 LOW | CCH | | | | | | | |
| TMOD | Timer 0 and 1 Mode | 89H | GATE | C/T | M1 | M0 | GATE | C/T | M |
| WDTRST [2] | Watchdog Timer Reset | A6H | | | | | | | |
| WDCON [2] | Watchdog Timer Control | 8FH[3] | - | - | - | - | - | WDPRE2 | W |

[1] SFRs are bit addressable.

[2] SFRs are modified from or added to the 80C51 SFRs.

[3] Extended SFRs accessed by preceding the instruction with MX escape (opcode A5h).

[4] Power on reset is 10H. Other reset is 00H.

[5] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any of them is written if BRGEN = 1, result is unpredictable.

[6] The unimplemented bits (labeled '-') in the SFRs are X's (unknown) at all times. '1's should **not** be written to these bits, as they may be used fo derivatives. The reset values shown for these bits are '0's although they are unknown when read.

## 8.3 Security bits

The P87C51Mx2 has security bits to protect users' firmware codes. With none of the security bits programmed, the code in the program memory can be verified. When only security bit 1 (see Table 5) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. $\overline{EA}$ is latched on Reset and all further programming of EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

**Table 5: EPROM security bits**

| Security Bits[1][2] | | | | |
|---|---|---|---|---|
| | **Bit 1** | **Bit 2** | **Bit 3** | **Protection description** |
| 1 | U | U | U | No program security features enabled. EEPROM is programmable and verifiable. |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled. |
| 3 | P | P | U | Same as 2, also verification is disabled. |
| 4 | P | P | P | Same as 3, external execution is disabled. |

[1] P - programmed. U - unprogrammed.

[2] Any other combination of security bits is not defined.

# 9. Limiting values

**Table 6: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{amb}$ | operating temperature | under bias | 0 | +70 | °C |
| $T_{stg}$ | storage temperature range | | –65 | +150 | °C |
| $V_I$ | input voltage on $\overline{EA}/V_{PP}$ pin to $V_{SS}$ | | 0 | +13 | V |
| | input voltage on any other pin to $V_{SS}$ | | –0.5 | $V_{DD}$+ 0.5 V | V |
| $I_I$, $I_O$ | maximum $I_{OL}$ per I/O pin | | - | 20 | mA |
| P | power dissipation | based on package heat transfer, not device power consumption | - | 1.5 | W |

[1] The following applies to the Limiting values:

a) Stresses above those listed under Limiting values may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Section 10 "Static characteristics" and Section 11 "Dynamic characteristics" of this specification is not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

# 10. Static characteristics

**Table 7: Static characteristics**

*$T_{amb}$ = 0 °C to +70 °C for commercial, unless otherwise specified; $V_{DD}$ = 2.7 V to 5.5 V unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | | –0.5 | | $0.2V_{DD}$–0.1 | V |
| $V_{IH}$ | Input high voltage (ports 0, 1, 2, 3, 4, $\overline{EA}$) | | $0.2V_{DD}$+0.9 | | $V_{DD}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2, 3, 4[8] | $V_{DD}$ = 4.5 V, $I_{OL}$ = 1.6 mA | - | | 0.4 | V |
| | | $V_{DD}$ = 2.7 V, $I_{OL}$ = 1.6 mA | | | | |
| $V_{OL1}$ | Output LOW voltage, port 0, ALE, $\overline{PSEN}$[7][8] | $V_{DD}$ = 4.5 V, $I_{OL}$ = 3.2 mA | - | | 0.4 | V |
| | | $V_{DD}$ = 2.7 V, $I_{OL}$ = 3.2 mA | | | | |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3, 4 | $V_{DD}$ = 4.5 V, $I_{OH}$ = –30 A | $V_{DD}$ – 0.7 | | - | V |
| | | $V_{DD}$ = 2.7 V, $I_{OH}$ = –10 A | | | - | |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3] | $V_{DD}$ = 4.5 V, $I_{OH}$ = –3.2 mA | $V_{DD}$ – 0.7 | | - | V |
| | | $V_{DD}$ = 2.7 V, $I_{OH}$ = –3.2 mA | | | | |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3, 4 | $V_{IN}$ = 0.4 V | –1 | | –75 | µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3, 4[8] | 4.5 V < $V_{DD}$ < 5.5 V, $V_{IN}$ = 2.0 V [4] | - | | –650 | µA |
| $I_{L1}$ | Input leakage current, port 0 | 0.45 < $V_{IN}$ < $V_{DD}$–0.3 | - | | 10 | µA |
| $I_{CC}$ | Power supply current | [5] | - | | | |
| | Active mode[5] | $V_{DD}$ = 5.5 V | - | | 7 + 2.7 /MHz × $f_{osc}$ | mA |
| | | $V_{DD}$ = 3.6 V | - | | 4 + 1.3 /MHz × $f_{osc}$ | |
| | Idle mode[5] | $V_{DD}$ = 5.5 V | - | | 4 + 1.3 /MHz × $f_{osc}$ | mA |
| | | $V_{DD}$ = 3.6 V | - | | 1 + 1.0 /MHz × $f_{osc}$ | |
| | Power-down mode or clock stopped (see Figure 16 for conditions) | $V_{DD}$ = 5.0 V | - | 20 | - | µA |
| | | $V_{DD}$ = 5.5 V | - | | 100 | µA |
| $R_{RST}$ | Internal reset pull-down resistor | | 40 | | 225 | kΩ |
| $C_{10}$ | Pin capacitance[10] (except $\overline{EA}$) | | - | | 15 | pF |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 ˚C), 5 V, unless otherwise stated.

[2] Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$ of ALE and ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading >100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.

[3] Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{DD}$–0.7 V specification when the address bits are stabilizing.

[4] Pins of ports 1, 2, 3 and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2 V for 4.5 V < $V_{DD}$ < 5.5 V.

[5] See Figure 13 through Figure 16 for $I_{CC}$ test conditions. $f_{osc}$ is the oscillator frequency in MHz.

[6] This value applies to $T_{amb}$ = 0 °C to +70 °C.

[7] Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[8] Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

a) Maximum $I_{OL}$ per port pin: 15 mA

b) Maximum $I_{OL}$ per 8-bit port: 26 mA

c) Maximum total $I_{OL}$ for all outputs: 71 mA

If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[9] ALE is tested to $V_{OH1}$, except when ALE is off then $V_{OH}$ is the voltage specification.

[10] Pin capacitance is characterized but not tested.

# 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

*$T_{amb}$ = 0 to +70 °C for commercial unless otherwise specified. Formulae including $t_{CLCL}$ assume oscillator signal with 50/50 duty cycle.*[1][2][3]

| Symbol | Fig | Parameter | 2.7 V < $V_{DD}$ < 5.5 V | | | | 4.5 V < $V_{DD}$ < 5.5 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Variable clock[4] | | $f_{OSC}$ = 12 MHz[4] | | Variable clock[4] | | $f_{OSC}$ = 24 MHz[4] | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{OSC}$ | 4 | Oscillator frequency | 0 | 12 | | - | 0 | 24 | | - | MHz |
| $t_{CLCL}$ | 4 | Clock cycle | - | - | 83 | - | | - | 41.5 | - | ns |
| $t_{LHLL}$ | 4 | ALE pulse width | $t_{CLCL}$–15 | - | 68 | - | $t_{CLCL}$–15 | - | 26 | - | ns |
| $t_{AVLL}$ | 4, 5, 6 | Address valid to ALE LOW | 0.5$t_{CLCL}$–15 | - | 8 | - | 0.5$t_{CLCL}$–15 | - | 5 | - | ns |
| $t_{LLAX}$ | 4, 5, 6 | Address hold after ALE LOW | 0.5$t_{CLCL}$–25 | - | 16 | - | 0.5$t_{CLCL}$–15 | - | 5 | - | ns |
| $t_{LLIV}$ | 4 | ALE LOW to valid instruction in | - | 0.5$t_{CLCL}$–25 | | 121 | - | 2$t_{CLCL}$ – 30 | | 53 | ns |
| $t_{LLPL}$ | 4 | ALE LOW to $\overline{PSEN}$ LOW | 0.5$t_{CLCL}$–25 | - | 16 | - | 0.5$t_{CLCL}$–12 | - | 8 | - | ns |
| $t_{PLPH}$ | 4 | $\overline{PSEN}$ pulse width | 1.5$t_{CLCL}$–25 | - | 100 | - | 1.5$t_{CLCL}$–20 | - | 42 | - | ns |
| $t_{PLIV}$ | 4 | $\overline{PSEN}$ LOW to valid instruction in | - | 1.5$t_{CLCL}$–45 | - | 80 | - | 1.5$t_{CLCL}$–35 | | 27 | ns |
| $t_{PXIX}$ | 4 | Input instruction hold after $\overline{PSEN}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{PXIZ}$ | 4 | Input instruction float after $\overline{PSEN}$ | - | 0.5$t_{CLCL}$–10 | - | 31 | - | 0.5$t_{CLCL}$–5 | - | 15 | ns |
| $t_{AVIV}$ | 4 | Address to valid instruction in (non-Extended Addressing Mode) | - | 2.5$t_{CLCL}$–35 | - | 173 | - | 2.5$t_{CLCL}$–30 | - | 74 | ns |
| $t_{AVIV1}$ | 4 | Address (A16-A22) to valid instruction in (Extended Addressing Mode) | - | 1.5$t_{CLCL}$–44 | - | 81 | - | 1.5$t_{CLCL}$–34 | - | 28 | ns |
| $t_{PLAZ}$ | 4 | $\overline{PSEN}$ LOW to address float | - | 16 | - | 16 | - | 8 | - | 8 | ns |

**Table 8: Dynamic characteristics** *...continued*

*$T_{amb}$ = 0 to +70 °C for commercial unless otherwise specified. Formulae including $t_{CLCL}$ assume oscillator signal with 50/50 duty cycle.*[1][2][3]

| Symbol | Fig | Parameter | 2.7 V < $V_{DD}$ < 5.5 V | | | | 4.5 V < $V_{DD}$ < 5.5 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Variable clock[4] | | $f_{osc}$ = 12 MHz[4] | | Variable clock[4] | | $f_{osc}$ = 24 MHz[4] | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Data Memory** | | | | | | | | | | | |
| $t_{RLRH}$ | 5 | $\overline{RD}$ pulse width | $3t_{CLCL}-25$ | - | 225 | - | $3t_{CLCL}-20$ | - | 105 | - | ns |
| $t_{WLWH}$ | 6 | $\overline{WR}$ pulse width | $3t_{CLCL}-25$ | - | 225 | - | $3t_{CLCL}-20$ | - | 105 | - | ns |
| $t_{RLDV}$ | 5 | $\overline{RD}$ LOW to valid data in | - | $2.5t_{CLCL}-55$ | - | 153 | - | $2.5t_{CLCL}-40$ | - | 64 | ns |
| $t_{RHDX}$ | 5 | Data hold after $\overline{RD}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{RHDZ}$ | 5 | Data float after $\overline{RD}$ | - | $t_{CLCL}-20$ | - | 63 | - | $t_{CLCL}-15$ | - | 26 | ns |
| $t_{LLDV}$ | 5 | ALE LOW to valid data in | - | $4t_{CLCL}-50$ | - | 283 | - | $4t_{CLCL}-35$ | - | 131 | ns |
| $t_{AVDV}$ | 5 | Address to valid data in (non-Extended Addressing Mode) | - | $4.5t_{CLCL}-40$ | - | 335 | - | $4.5t_{CLCL}-30$ | - | 157 | ns |
| $t_{AVDV1}$ | 5 | Address (A16-A22) to valid data in (Extended Addressing Mode) | - | $3.5t_{CLCL}-45$ | - | 246 | - | $3.5t_{CLCL}-35$ | - | 110 | ns |
| $t_{LLWL}$ | 5, 6 | ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW | $1.5t_{CLCL}-5$ | $1.5t_{CLCL}+20$ | 120 | 145 | $1.5t_{CLCL}-10$ | $1.5t_{CLCL}+20$ | 52 | 82 | ns |
| $t_{AVWL}$ | 5, 6 | Address valid to $\overline{WR}$ or $\overline{RD}$ LOW (non-Extended Addressing Mode) | $2t_{CLCL}-5$ | - | 161 | - | $2t_{CLCL}-5$ | - | 78 | - | ns |
| $t_{AVWL1}$ | 5, 6 | Address (A16-A22) valid to $\overline{WR}$ or $\overline{RD}$ LOW (Extended Addressing Mode) | $t_{CLCL}-10$ | - | 73 | - | $t_{CLCL}-10$ | - | 31 | - | ns |
| $t_{QVWX}$ | 6 | Data valid to $\overline{WR}$ transition | $0.5t_{CLCL}-20$ | - | 21 | - | $0.5t_{CLCL}-15$ | - | 5 | - | ns |
| $t_{WHQX}$ | 6 | Data hold after $\overline{WR}$ | $0.5t_{CLCL}-25$ | - | 16 | - | $0.5t_{CLCL}-11$ | - | 9 | - | ns |
| $t_{QVWH}$ | 6 | Data valid to WR HIGH | $3.5t_{CLCL}-10$ | - | 281 | - | $3.5t_{CLCL}-10$ | - | 135 | - | ns |

**Table 8: Dynamic characteristics** *...continued*

*$T_{amb}$ = 0 to +70 °C for commercial unless otherwise specified. Formulae including $t_{CLCL}$ assume oscillator signal with 50/50 duty cycle.*[1][2][3]

| Symbol | Fig | Parameter | 2.7 V < $V_{DD}$ < 5.5 V | | | | 4.5 V < $V_{DD}$ < 5.5 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Variable clock[4] | | $f_{osc}$ = 12 MHz[4] | | Variable clock[4] | | $f_{osc}$ = 24 MHz[4] | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RLAZ}$ | 5 | $\overline{RD}$ LOW to address float | - | 0 | - | 0 | - | 0 | - | 0 | ns |
| $t_{WHLH}$ | 5, 6 | $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH | $0.5t_{CLCL}-20$ | $0.5t_{CLCL}+10$ | 21 | 51 | $0.5t_{CLCL}-11$ | $0.5t_{CLCL}+10$ | 9 | 30 | ns |
| **External Clock** | | | | | | | | | | | |
| $t_{CHCX}$ | 12 | HIGH time | 33 | $t_{CLCL}-t_{CLCX}$ | 33 | - | 16 | $t_{CLCL}-t_{CLCX}$ | 16 | - | ns |
| $t_{CLCX}$ | 12 | LOW time | 33 | $t_{CLCL}-t_{CHCX}$ | 33 | - | 16 | $t_{CLCL}-t_{CHCX}$ | 16 | - | ns |
| $t_{CLCH}$ | 12 | Rise time | - | 8 | - | 8 | - | 4 | - | 4 | ns |
| $t_{CHCL}$ | 12 | Fall Time | - | 8 | - | 8 | - | 4 | - | 4 | ns |
| **Shift Register** | | | | | | | | | | | |
| $t_{XLXL}$ | 7 | Serial port clock cycle time | $6t_{CLCL}$ | - | 500 | - | $t_{CLCL}-t_{CLCX}$ | - | 250 | - | ns |
| $t_{QVXH}$ | 7 | Output data setup to clock rising edge | $5t_{CLCL}-10$ | - | 406 | - | $t_{CLCL}-t_{CHCX}$ | - | 198 | - | ns |
| $t_{XHQX}$ | 7 | Output data hold after clock rising edge | $t_{CLCL}-10$ | - | 68 | - | $t_{CLCL}-15$ | - | 26 | - | ns |
| $t_{XHDX}$ | 7 | Input data hold after clock rising edge | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{XHDV}$ | 7 | Clock rising edge to input data valid | - | $5t_{CLCL}-55$ | - | 361 | - | $5t_{CLCL}-35$ | - | 173 | ns |
| **SPI Interface** | | | | | | | | | | | |
| $f_{SPI}$ | | | | | | | | | | | MHz |
| | | | - | - | - | - | - | - | - | - | |
| | | | 0 | 2.0 | 0 | 2.0 | 0 | 2.0 | 0 | 2.0 | |
| | | | - | - | - | - | - | - | - | - | |
| | | | 0 | 3.0 | 0 | 3.0 | 0 | 3.0 | 0 | 3.0 | |
| $t_{SPICYC}$ | 8, 9, 10, 11 | Cycle time | | | | | | | | | ns |
| | | 2.0 MHz (Master) | - | - | - | - | - | - | - | - | |
| | | 2.0 MHz (Slave) | 500 | - | 500 | - | 500 | - | 500 | - | |
| | | 3.0 MHz (Master) | - | - | - | - | - | - | - | - | |
| | | 3.0 MHz (Slave) | 333 | - | 333 | - | 333 | - | 333 | - | |

**Table 8: Dynamic characteristics** *...continued*

*$T_{amb}$ = 0 to +70 °C for commercial unless otherwise specified. Formulae including $t_{CLCL}$ assume oscillator signal with 50/50 duty cycle.*[1][2][3]

| Symbol | Fig | Parameter | 2.7 V < $V_{DD}$ < 5.5 V | | | | 4.5 V < $V_{DD}$ < 5.5 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Variable clock[4] | | $f_{OSC}$ = 12 MHz[4] | | Variable clock[4] | | $f_{OSC}$ = 24 MHz[4] | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{SPILEAD}$ | 10, 11 | Enable lead time (Slave) | | | | | | | | | ns |
| | | 2.0 MHz | 250 | - | 250 | - | 250 | - | 250 | - | |
| | | 3.0 MHz | 240 | - | 240 | - | 240 | - | 240 | - | |
| $t_{SPILAG}$ | 10, 11 | Enable lag time (Slave) | | | | | | | | | ns |
| | | 2.0 MHz | 250 | - | 250 | - | 250 | - | 250 | - | |
| | | 3.0 MHz | 240 | - | 240 | - | 240 | - | 240 | - | |
| $t_{SPICLKH}$ | 8, 9, 10, 11 | SPICLK HIGH time | | | | | | | | | ns |
| | | Master | 340 | - | 340 | - | 340 | - | 340 | - | |
| | | Slave | 190 | - | 190 | - | 190 | - | 190 | - | |
| $t_{SPICLKL}$ | 8, 9, 10, 11 | SPICLK LOW time | | | | | | | | | ns |
| | | Master | 340 | - | 340 | - | 340 | - | 340 | - | |
| | | Slave | 190 | - | 190 | - | 190 | - | 190 | - | |
| $t_{SPIDSU}$ | 8, 9, 10, 11 | Data setup time (Master or Slave) | 100 | - | 100 | - | 100 | - | 100 | - | ns |
| $t_{SPIDH}$ | 8, 9, 10, 11 | Data hold time (Master or Slave) | 100 | - | 100 | - | 100 | - | 100 | - | ns |
| $t_{SPIA}$ | 10, 11 | Access time (Slave) | 0 | 120 | 0 | 120 | 0 | 120 | 0 | 120 | ns |
| $t_{SPIDIS}$ | 10, 11 | Disable time (Slave) | | | | | | | | | ns |
| | | 2.0 MHz | 0 | 240 | - | 240 | 0 | 240 | - | 240 | |
| | | 3.0 MHz | 0 | 167 | - | 167 | 0 | 167 | - | 167 | |
| $t_{SPIDV}$ | 8, 9, 10, 11 | Enable to output data valid | | | | | | | | | ns |
| | | 2.0 MHz | - | 240 | - | 240 | - | 240 | - | 240 | |
| | | 3.0 MHz | - | 167 | - | 167 | - | 167 | - | 167 | |
| $t_{SPIOH}$ | 8, 9, 10, 11 | Output data hold time | 0 | - | 0 | - | 0 | - | 0 | - | ns |

**Table 8: Dynamic characteristics** *...continued*

*$T_{amb}$ = 0 to +70 °C for commercial unless otherwise specified. Formulae including $t_{CLCL}$ assume oscillator signal with 50/50 duty cycle.*[1][2][3]

| Symbol | Fig | Parameter | 2.7 V < $V_{DD}$ < 5.5 V | | | | 4.5 V < $V_{DD}$ < 5.5 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Variable clock[4] | | $f_{OSC}$ = 12 MHz[4] | | Variable clock[4] | | $f_{OSC}$ = 24 MHz[4] | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{SPIR}$ | 8, 9, 10, 11 | Rise time | | | | | | | | | ns |
| | | SPI outputs (SPICLK, MOSI, MISO) | - | 100 | - | 100 | - | 100 | - | 100 | |
| | | SPI outputs (SPICLK, MOSI, MISO, $\overline{SS}$) | - | 2000 | - | 2000 | - | 2000 | - | 2000 | |
| $t_{SPIF}$ | 8, 9, 10, 11 | Fall time | | | | | | | | | ns |
| | | SPI outputs (SPICLK, MOSI, MISO) | - | 100 | - | 100 | - | 100 | - | 100 | |
| | | SPI outputs (SPICLK, MOSI, MISO, $\overline{SS}$) | - | 2000 | - | 2000 | - | 2000 | - | 2000 | |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.

[3] Interfacing the microcontroller to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

[4] Parts are tested down to 2 MHz, but are guaranteed to operate down to 0 Hz.

## 11.1 Explanation of AC symbols

Each timing symbol has five characters. The first character is always ‘t’ (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

**A —** Address

**C —** Clock

**D —** Input data

**H —** Logic level HIGH

**I —** Instruction (program memory contents)

**L —** Logic level LOW, or ALE

**P —** $\overline{\text{PSEN}}$

**Q —** Output data

**R —** $\overline{\text{RD}}$ signal

**t —** Time

**V —** Valid

**W —** $\overline{\text{WR}}$ signal

**X —** No longer a valid logic level

**Z —** Float

**Examples:**

$\mathbf{t_{AVLL}}$ **—** Time for address valid to ALE LOW

$\mathbf{t_{LLPL}}$ **—** Time for ALE LOW to $\overline{\text{PSEN}}$ LOW

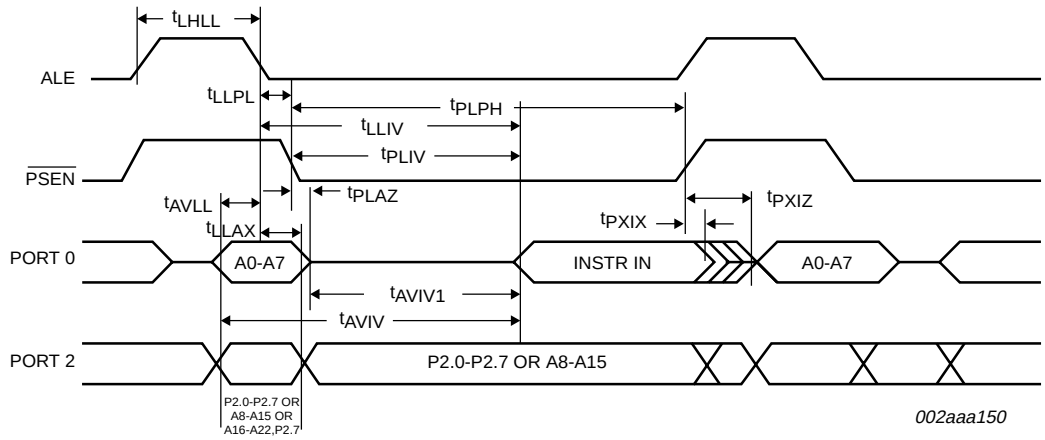



**Fig 4. External program memory read cycle (extended memory cycle).**

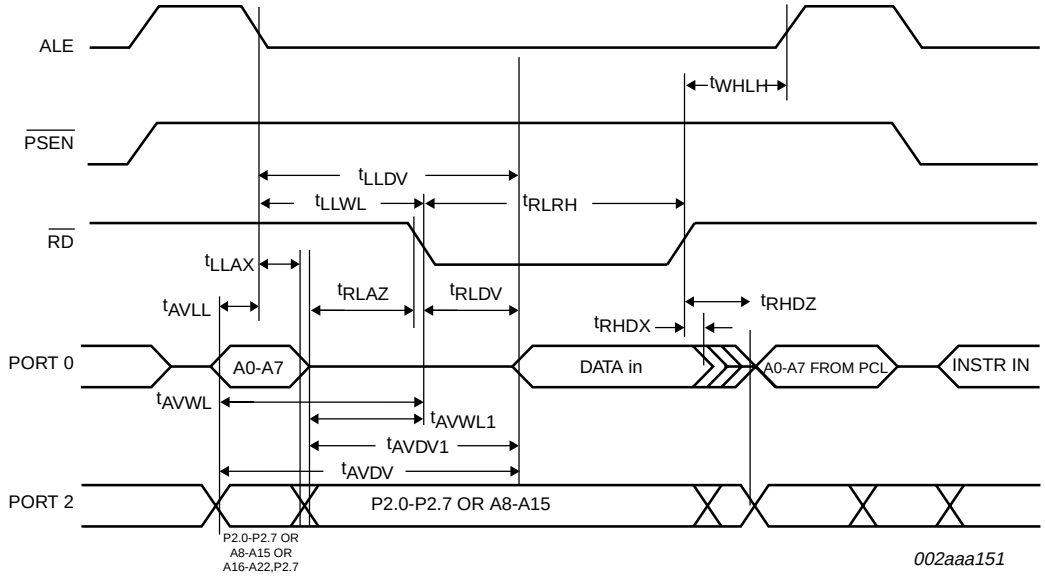



**Fig 5. External data memory read cycle.**

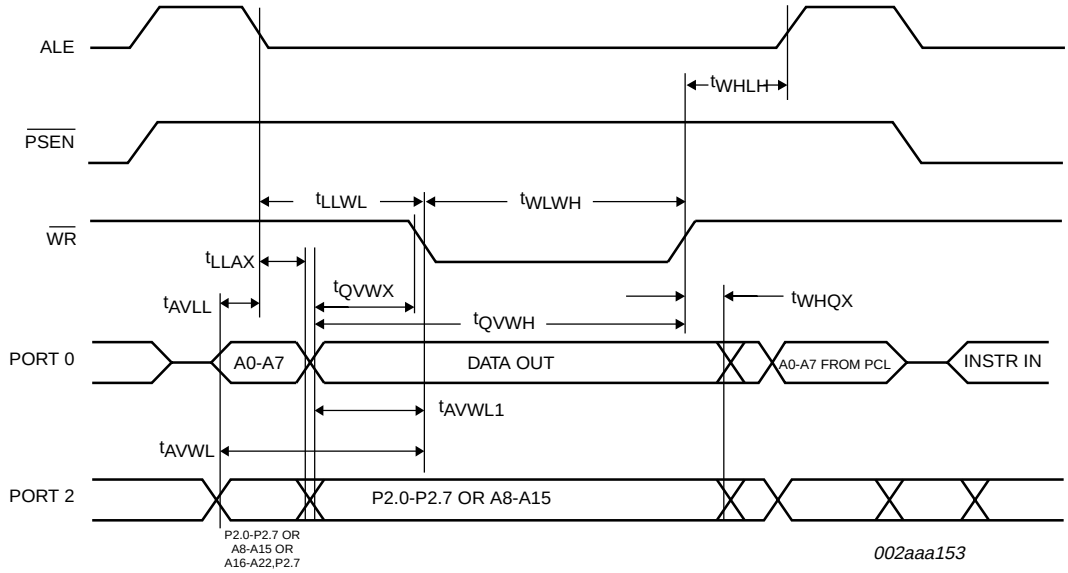



**Fig 6. External data memory write cycle.**

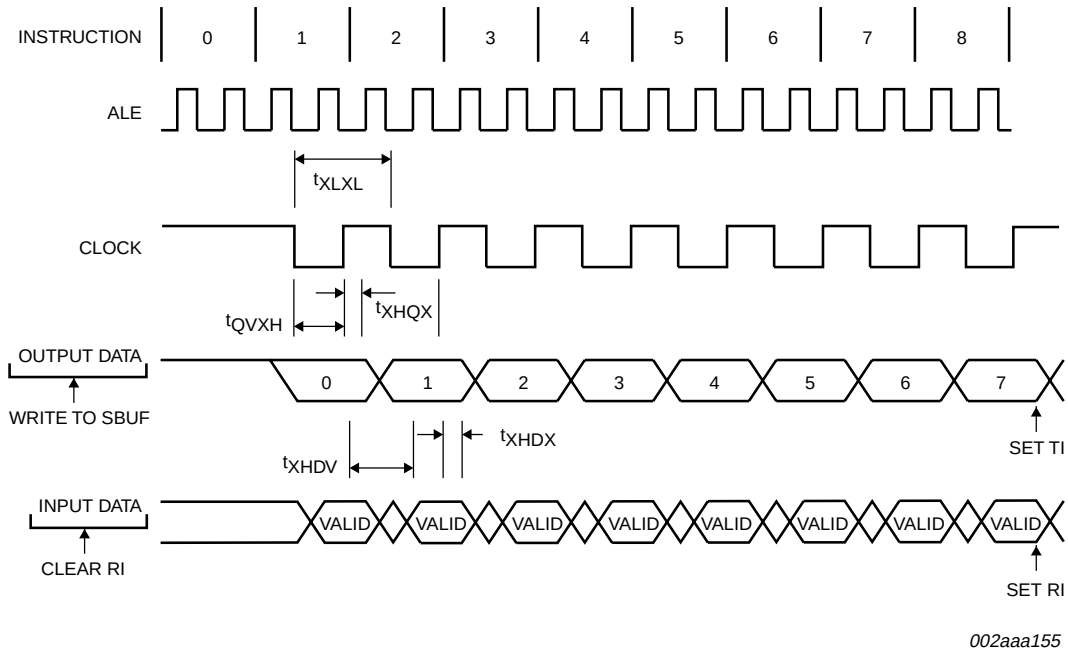



**Fig 7. Shift register mode timing.**

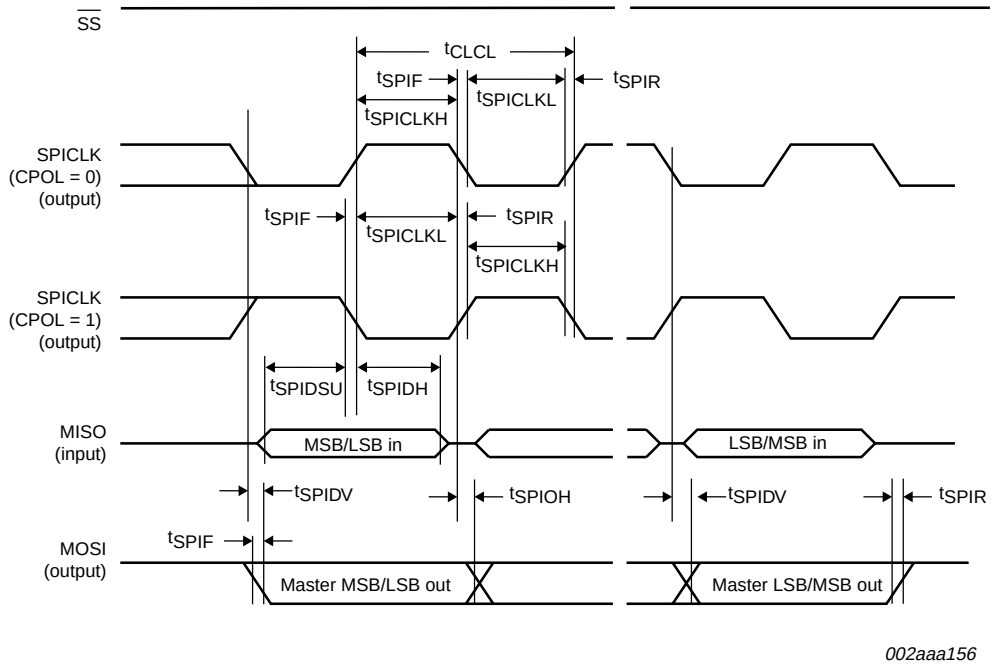



**Fig 8. SPI master timing (CPHA = 0).**

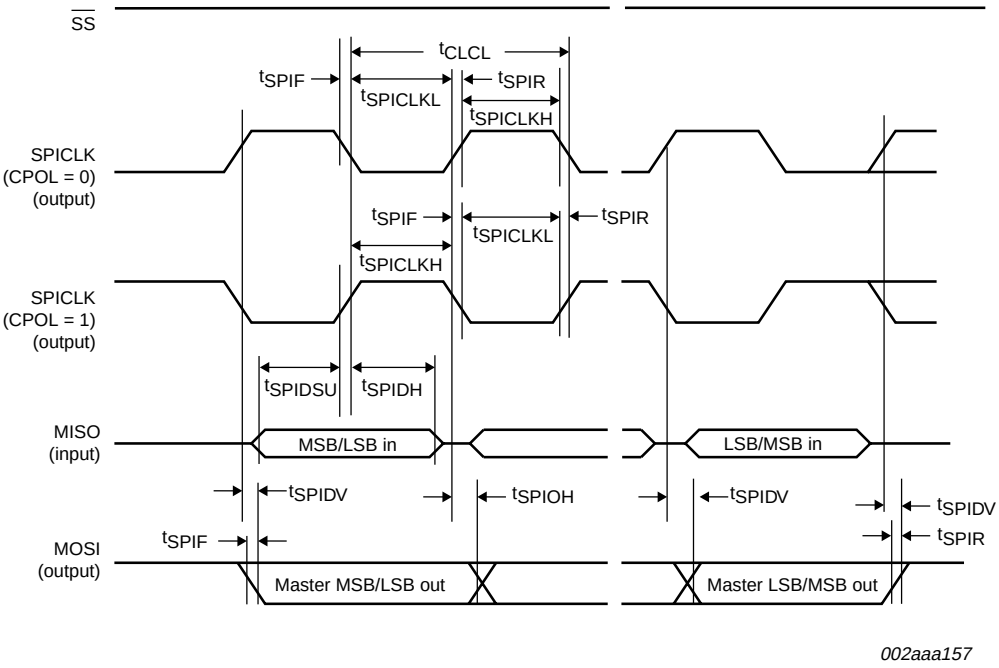



**Fig 9. SPI master timing (CPHA = 1).**

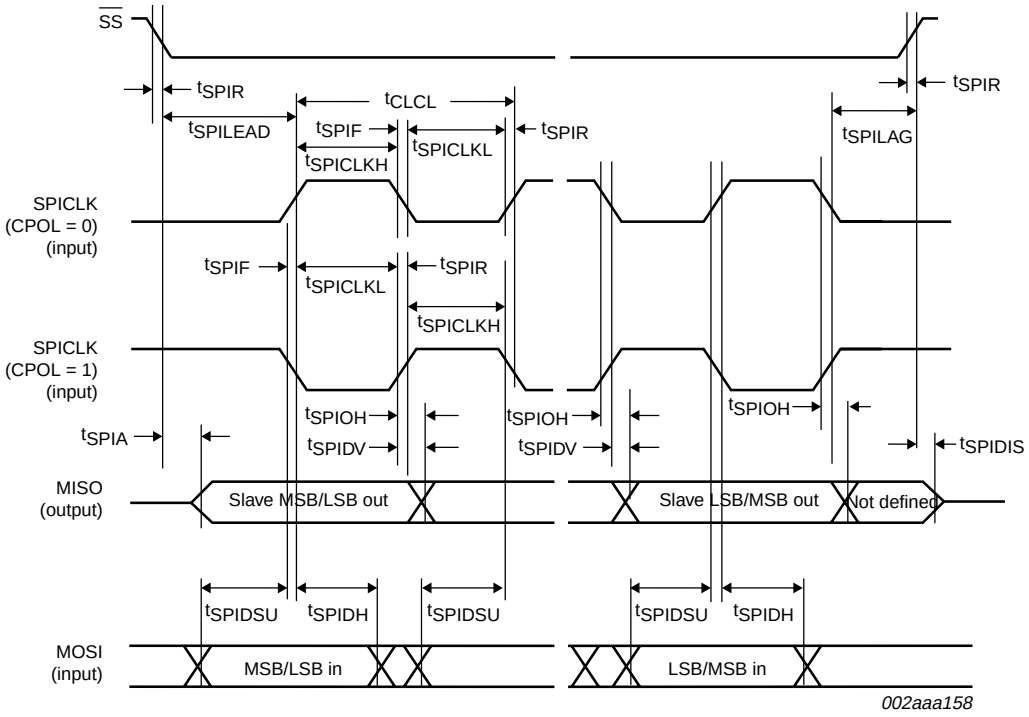



**Fig 10. SPI slave timing (CPHA = 0).**

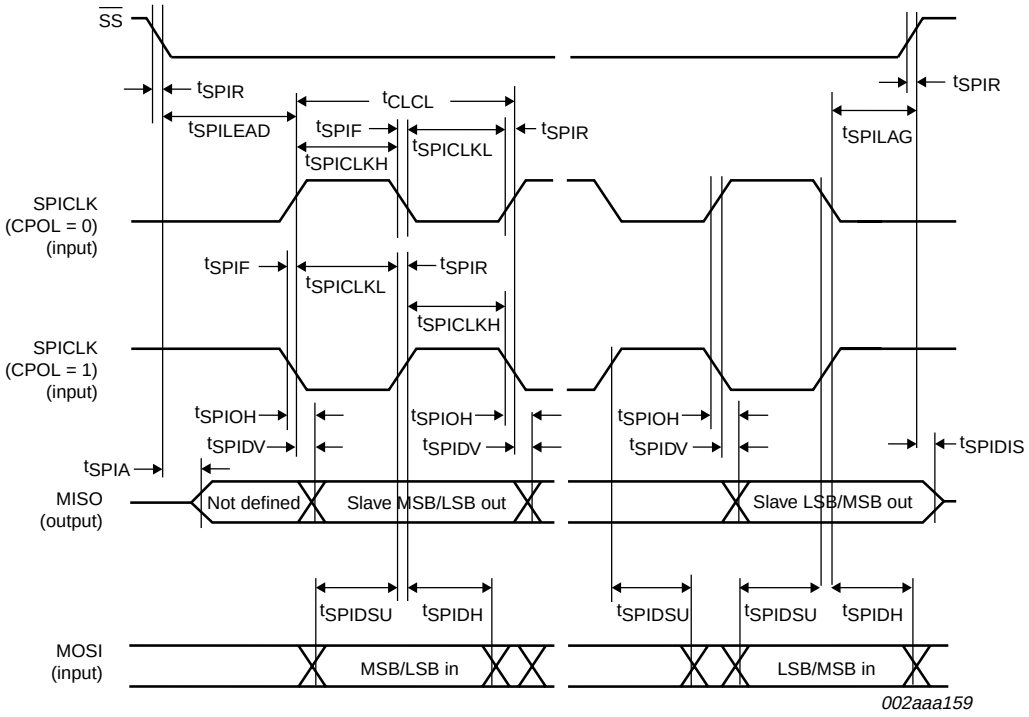



**Fig 11. SPI slave timing (CPHA = 1).**

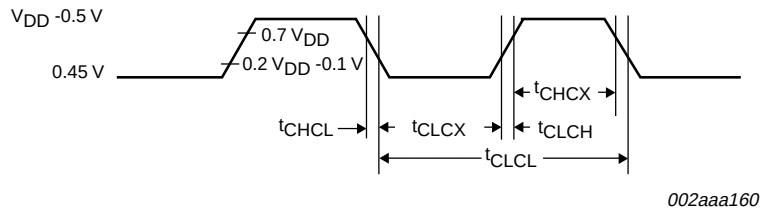



**Fig 12. External clock drive.**

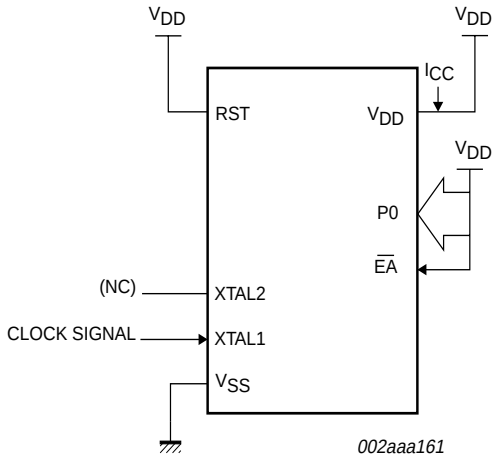



**Fig 13. $I_{CC}$ test condition, active mode (all other pins are disconnected).**

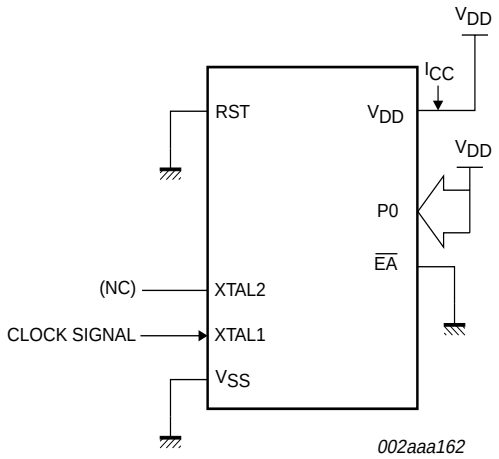



**Fig 14. $I_{CC}$ test condition, idle mode (all other pins are disconnected).**

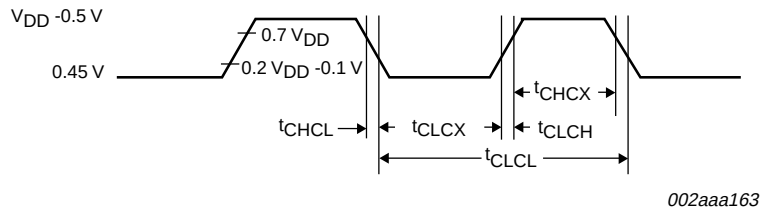



**Fig 15. Clock signal waveform for $I_{CC}$ tests in active and idle modes ($t_{CLCH}$ = $t_{CHCL}$ = 5 ns).**

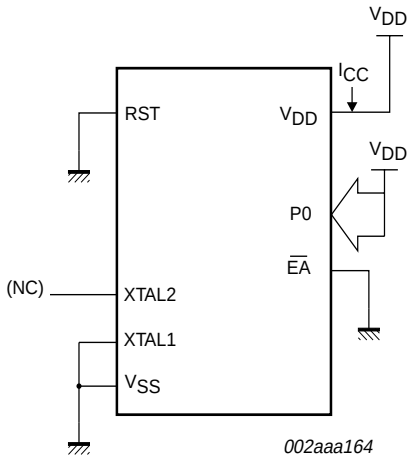
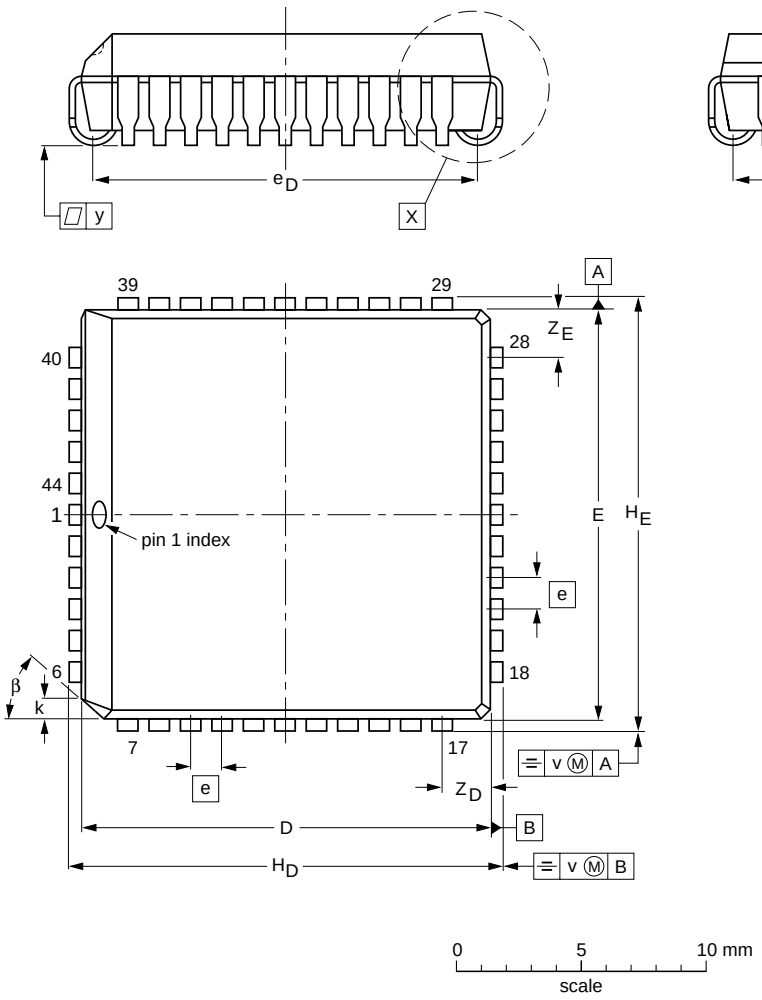



**Fig 16. $I_{CC}$ test condition, power-down mode (all other pins are disconnected, $V_{DD}$ = 2.0 V to 5.5 V).**

## 12. Package outline

**PLCC44: plastic leaded chip carrier; 44 leads** **SOT187-2**




**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | $D^{(1)}$ | $E^{(1)}$ | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $L_p$ | v | w | y | $Z_D^{(1)}$ max. | $Z_E^{(1)}$ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 16.66<br>16.51 | 16.66<br>16.51 | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07 | 1.44<br>1.02 | 0.18 | 0.18 | 0.1 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.02 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650 | 0.656<br>0.650 | 0.05 | 0.63<br>0.59 | 0.63<br>0.59 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT187-2 | 112E10 | MS-018 | EDR-7319 | | | ~~99-12-27~~<br>01-11-14 |

**Fig 17. SOT187-2.**

# 13. Soldering

## 13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

## 13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 $mm^3$ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 $mm^3$ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

## 13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 13.5 Package related soldering information

**Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package[1] | Soldering method | |
|---|---|---|
| | Wave | Reflow[2] |
| BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[4] | suitable |
| PLCC[5], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[5][6] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended[7] | suitable |
| CWQCCN..L[8], PMFP[9], WQCCN..L[8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 14. Revision history

**Table 10: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 03 | 20031113 | - | **Product data (9397 750 12302); ECN 853-2426 01-A14402 dated 6 November 2003**<br>Modifications:<br>• Figure 5 “External data memory read cycle.” on page 24; added $t_{RLDV}$, removed ‘non-extended memory cycle’ from figure title.<br>• Figure 6 “External data memory write cycle.” on page 25; removed ‘non-extended memory cycle’ from figure title. |
| 02 | 20030519 | - | **Product data (9397 750 11517)** |
| _1 | 20010406 | - | **Preliminary specification (9397 750 08199)** |

## 15. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 16. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 17. Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

9397 750 12302

# Contents


| | | |
|---|---|---|
| **1** | **General description** | **1** |
| **2** | **Features** | **1** |
| 2.1 | Key features | 1 |
| 2.2 | Key benefits | 2 |
| 2.3 | Complete features | 2 |
| **3** | **Differences between P87C51MX2/02 part and previous revisions of P87C51MX2** | **3** |
| **4** | **Ordering information** | **3** |
| **5** | **Block diagram** | **4** |
| **6** | **Functional diagram** | **5** |
| **7** | **Pinning information** | **6** |
| 7.1 | Pinning | 6 |
| 7.2 | Pin description | 7 |
| **8** | **Functional description** | **10** |
| 8.1 | Memory arrangement | 10 |
| 8.2 | Special Function Registers | 10 |
| 8.3 | Security bits | 15 |
| **9** | **Limiting values** | **15** |
| **10** | **Static characteristics** | **16** |
| **11** | **Dynamic characteristics** | **18** |
| 11.1 | Explanation of AC symbols | 23 |
| **12** | **Package outline** | **30** |
| **13** | **Soldering** | **31** |
| 13.1 | Introduction to soldering surface mount packages | 31 |
| 13.2 | Reflow soldering | 31 |
| 13.3 | Wave soldering | 31 |
| 13.4 | Manual soldering | 32 |
| 13.5 | Package related soldering information | 32 |
| **14** | **Revision history** | **34** |
| **15** | **Data sheet status** | **35** |
| **16** | **Definitions** | **35** |
| **17** | **Disclaimers** | **35** |




**Date of release: 13 November 2003** **Document order number: 9397 750 12302**

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View P87C51MC2BA/02,529 on WIN SOURCE
- NXP / Nexperia Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management