THE DATASHEET OF

P3PS850BHG-08CR

P3PS850BH

Timing-Safe™ Peak EMI Reduction IC

Functional Description

P3PS850BH is a versatile, Timing−Safe peak EMI reduction IC. P3PS850BH accepts one input from an external reference, and locks on to it delivering a 1x Timing−Safe output clock. P3PS850BH has a Frequency Selection (FS) control that facilitates selecting one of the two operating frequency ranges. Refer to the *frequency Selection table.* The device has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected at this pin to GND. P3PS850BH has an MR pin for selecting one of the two Modulation Rates. PD#/OE provides the Power Down option. Outputs will be tri−stated when power down is active.

P3PS850BH operates over a supply voltage range of 2.3 V to 3.6 V, and is available in an 8 Pin WDFN (2 mm x 2 mm) Package.

General Features

- 1x , LVCMOS Timing−Safe Peak EMI Reduction
- Input Clock Frequency:
  - 18 MHz − 72 MHz
- Output Clock Frequency(Timing−Safe):
  - 18 MHz − 72 MHz
- Analog Frequency Deviation Selection
- Two different Modulation Rate Selection
- Power Down Option for Power Save
- Output Buffer Strength: 16 mA
- Supply Voltage: 2.3 V − 3.6 V
- 8 pin WDFN 2 mm x 2 mm, (TDFN) Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Application

- P3PS850BH is targeted for use in consumer electronic applications like mobile phones, Camera modules, MFP and DPF.

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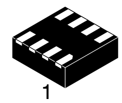
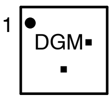
MARKING DIAGRAMS

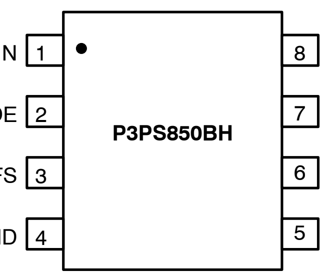


WDFN8
CASE 511AQ



DG = Specific Device Code
M = Date Code
▪ = Pb−Free Device

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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January, 2012 − Rev. 1

Publication Order Number:
P3PS850BH/D

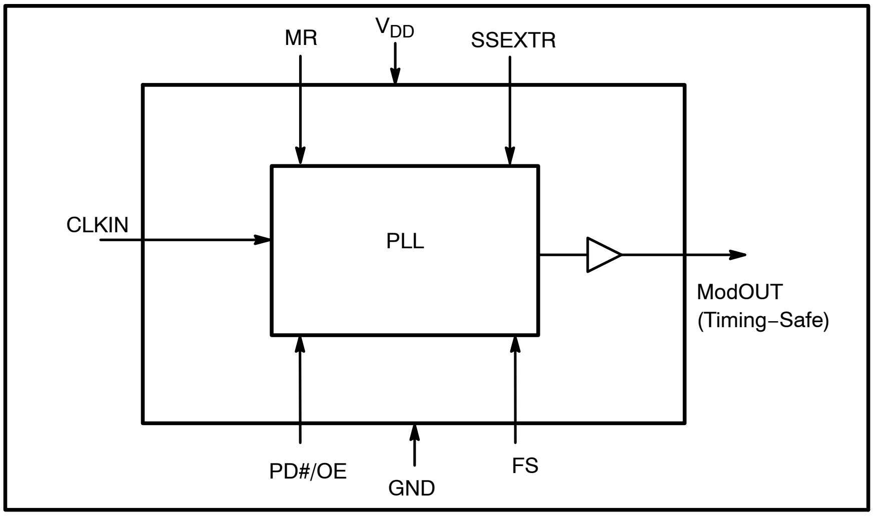


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference Clock input.
2	PD# / OE	I	Power Down. Pull LOW to enable Power Down. Outputs will be tri−stated when power down is enabled. Pull HIGH to disable power down and enable output. NO default state.
3	FS	I	Frequency Select .NO default state. Refer to the *Frequency Selection* table
4	GND	P	Ground
5	ModOUT	O	Buffered modulated Timing−Safe clock output
6	MR	I	Modulation Rate Select. When LOW, selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull−up resistor.
7	SSEXTR	I	Analog Deviation Selection through external resistor to GND.
8	V_{DD}	P	Supply Voltage

Table 2. FREQUENCY SELECTION TABLE

FS	Frequency (MHz)
0	18−36
1	36−72

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.3	3.6	V
T_A	Operating Temperature	−20	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 4. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			2.3	2.7	3.6	V
V_{IH}	Input HIGH Voltage			0.65 * V_{DD}			V
V_{IL}	Input LOW Voltage					0.35 * V_{DD}	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$				10	μA
I_{IL}	Input LOW Current	V_{IN} = 0 V for MR pin				10	μA
V_{OH}	Output HIGH Voltage	I_{OH} = −16 mA		0.75 * V_{DD}			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA				0.25 * V_{DD}	V
I_{CC}	Static Supply Current	PD#/OE pin pulled to GND				10	μA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS = 0, @ 18 MHz		6	10	mA
			FS = 0, @ 24 MHz		7	12	
			FS = 0, @ 36 MHz		10	17	
			FS = 1, @ 36 MHz		9	14	
			FS = 1, @ 48 MHz		11	19	
			FS = 1, @ 72 MHz		16	28	
Z_o	Output Impedance				13		Ω

Table 6. AC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency	FS = 0	18	24	36	MHz
	FS = 1	36	48	72	
ModOUT	FS = 0	18	24	36	
	FS = 1	36	48	72	
Duty Cycle (Note 1 and 2)	Measured at V_{DD} / 2	45	50	55	%
Rise Time (Note 1 and 2)	Measured between 20% to 80%		0.8	1.2	ns
Fall Time (Note 1 and 2)	Measured between 80% to 20%		0.8	1.2	ns

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 6. AC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions		Min	Typ	Max	Unit
Cycle−to−Cycle Jitter (Note 2)	Unloaded output with SSEXTR pin OPEN	FS = 0, 18 MHz		± 250	± 350	ps
		FS = 0, 24 MHz		± 150	± 225	
		FS = 0, 36 MHz		± 75	± 125	
		FS = 1, 36 MHz		± 150	± 200	
		FS = 1, 48 MHz		± 100	± 150	
		FS = 1, 72 MHz		± 75	± 125	
PLL Lock Time (Note 2)	Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High				1	ms

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

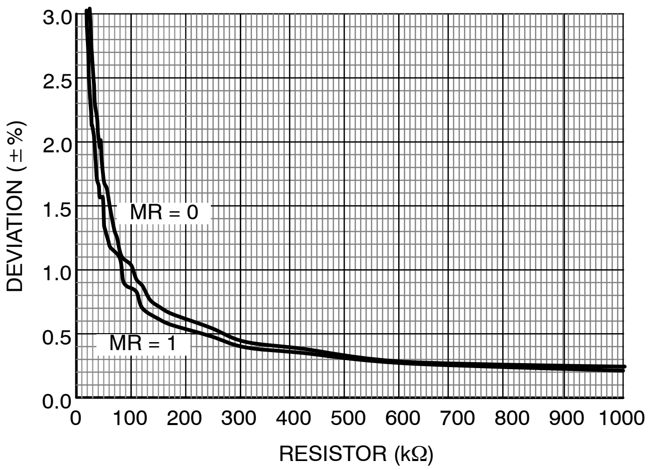


Figure 2. Deviation vs. SSEXTR @ 18 MHz (FS = 0)

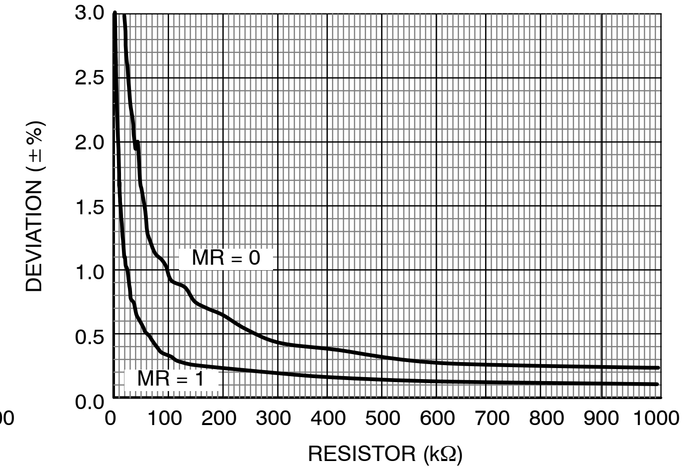


Figure 3. Deviation vs. SSEXTR @ 24 MHz (FS = 0)

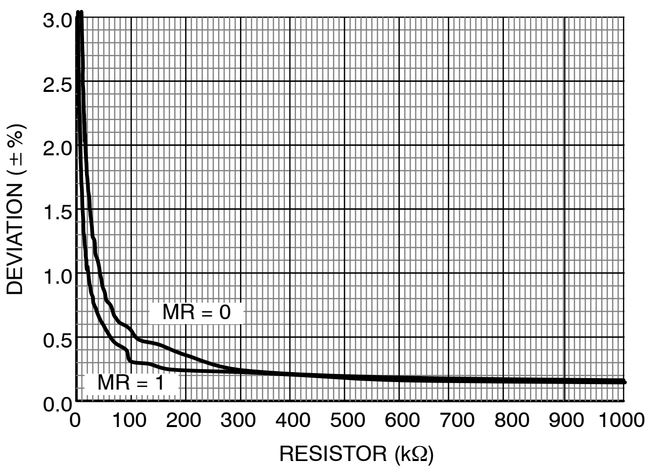


Figure 4. Deviation vs. SSEXTR @ 27 MHz (FS = 0)

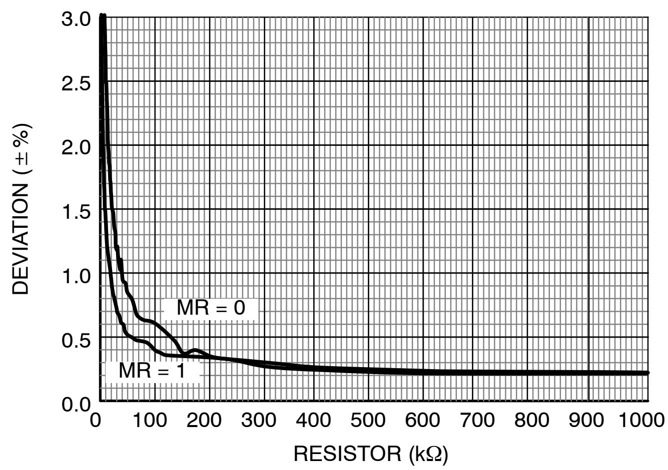


Figure 5. Deviation vs. SSEXTR @ 30 MHz (FS = 0)

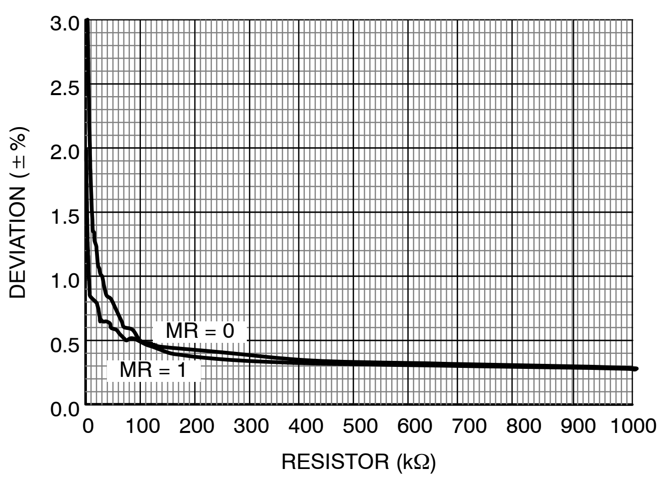


Figure 6. Deviation vs. SSEXTR @ 36 MHz (FS = 0)

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

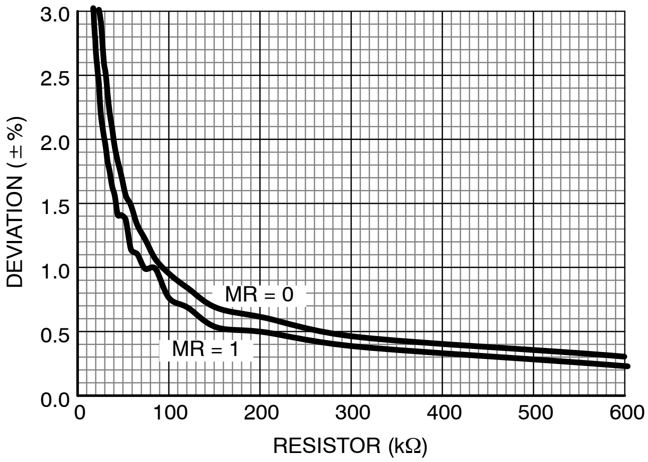


Figure 7. Deviation vs. SSEXTR @ 36 MHz (FS = 1)

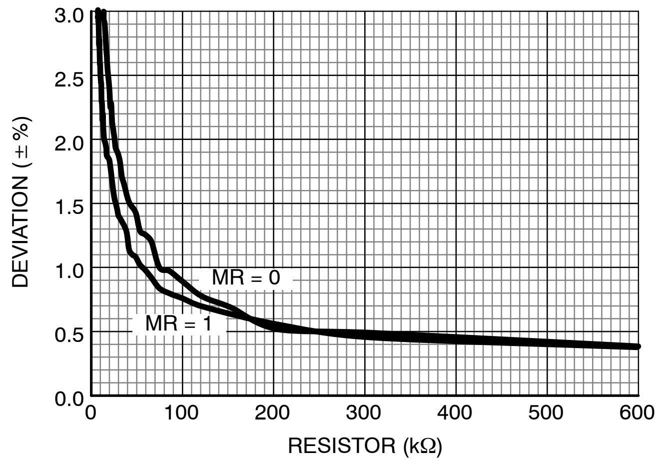


Figure 8. Deviation vs. SSEXTR @ 48 MHz (FS = 1)

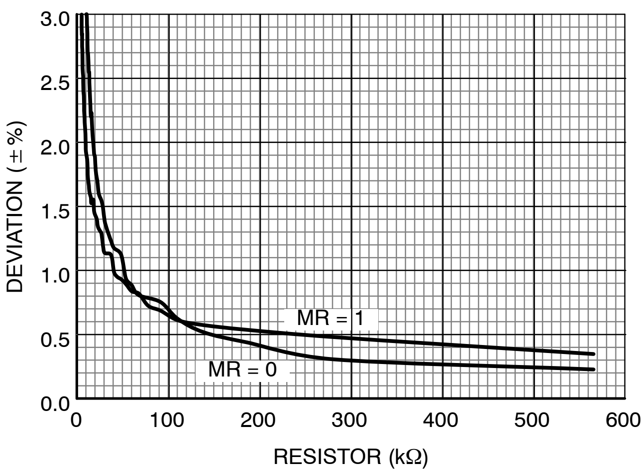


Figure 9. Deviation vs. SSEXTR @ 54 MHz (FS = 1)

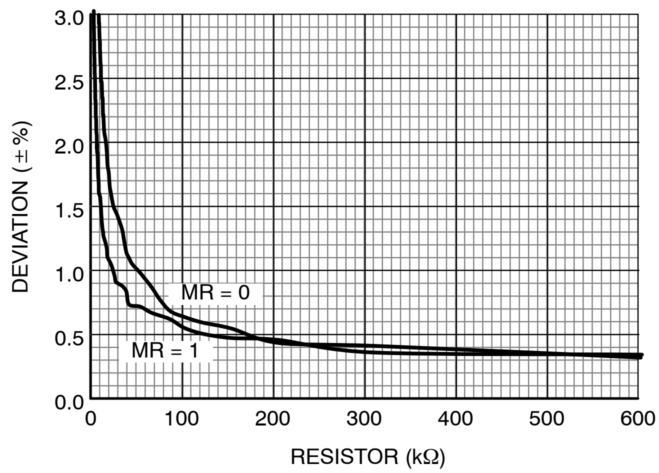


Figure 10. Deviation vs. SSEXTR @ 60 MHz (FS = 1)

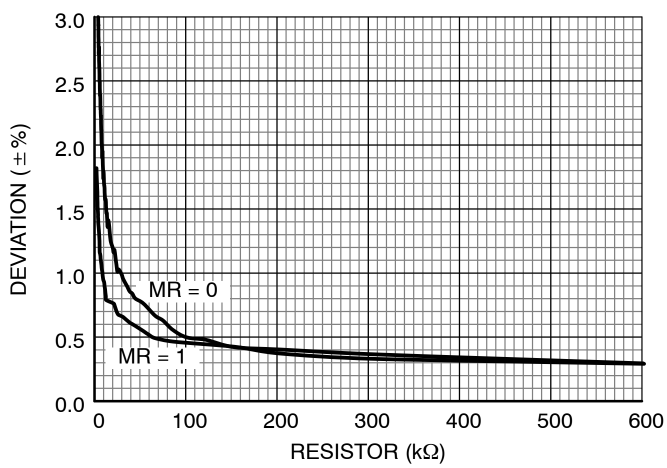


Figure 11. Deviation vs. SSEXTR @ 72 MHz (FS = 1)

TSKEW VERSUS SSEXTR RESISTANCE CHARTS

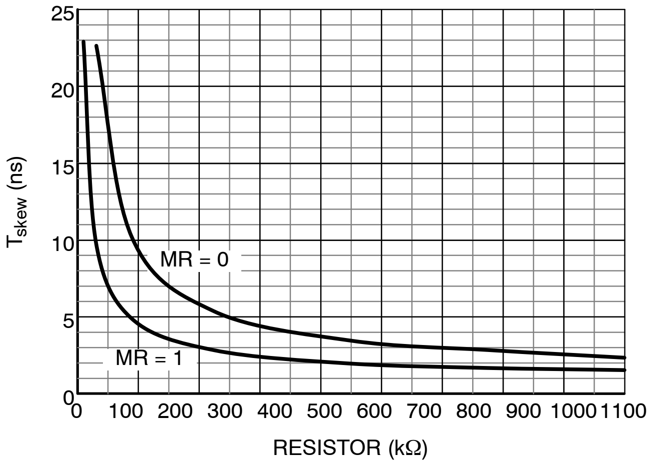


Figure 12. Tskew vs. SSEXTR @ 18 MHz (FS = 0)

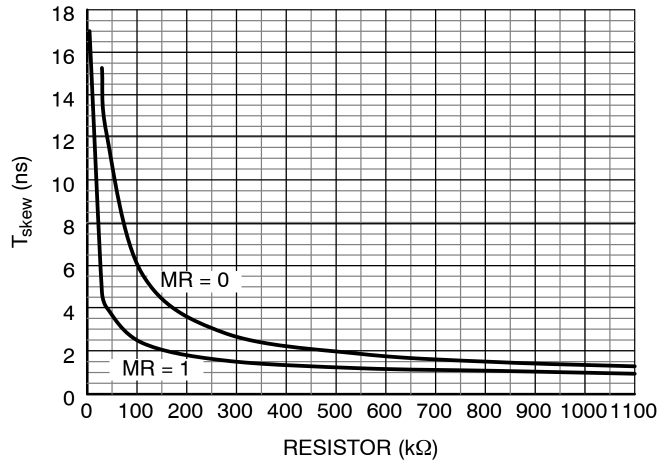


Figure 13. Tskew vs. SSEXTR @ 24 MHz (FS = 0)

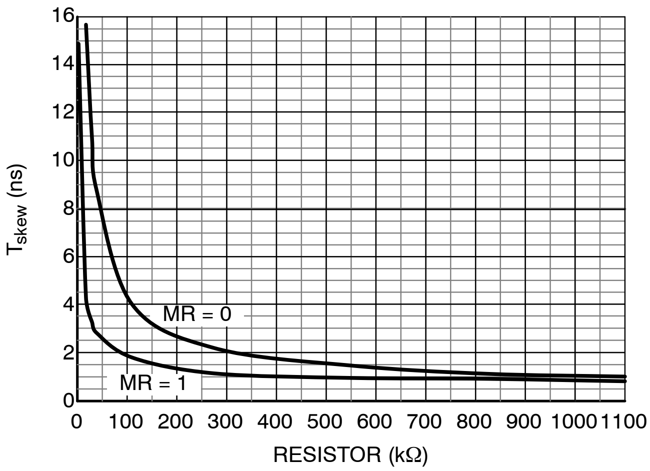


Figure 14. Tskew vs. SSEXTR @ 27 MHz (FS = 0)

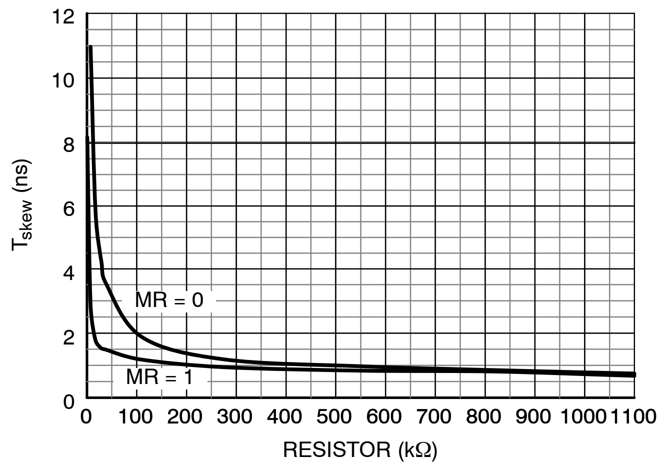


Figure 15. Tskew vs. SSEXTR @ 36 MHz (FS = 0)

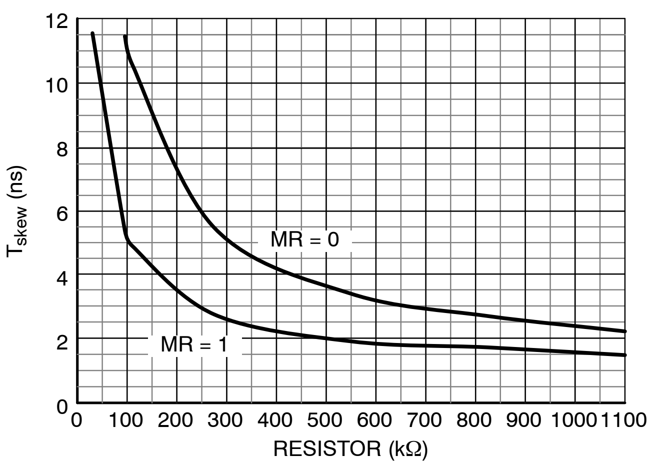


Figure 16. Tskew vs. SSEXTR @ 36 MHz (FS = 1)

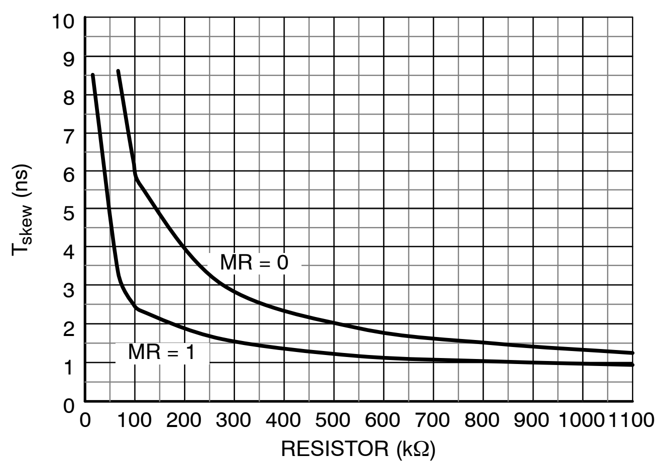


Figure 17. Tskew vs. SSEXTR @ 48 MHz (FS = 1)

TSKEW VERSUS SSEXTR RESISTANCE CHARTS

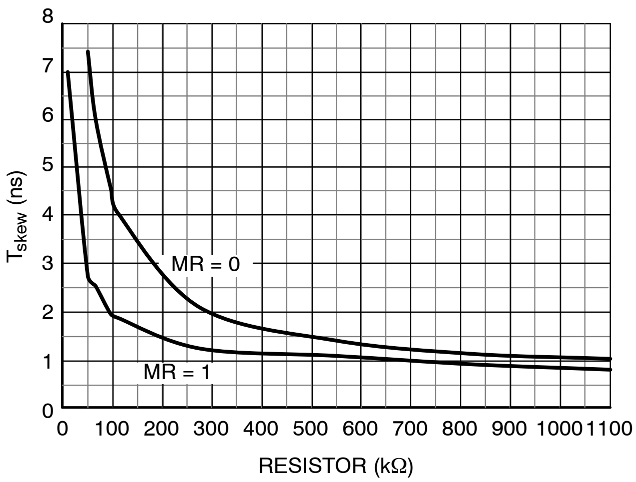


Figure 18. Tskew vs. SSEXTR @ 54 MHz (FS = 1)

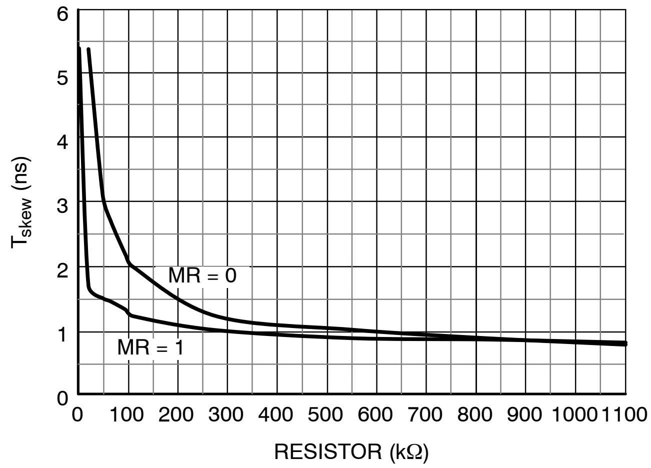


Figure 19. Tskew vs. SSEXTR @ 72 MHz (FS = 1)

MINIMUM SSEXTR RESISTANCE VERSUS FREQUENCY(FOR TIMING−SAFE OPERATION) CHARTS

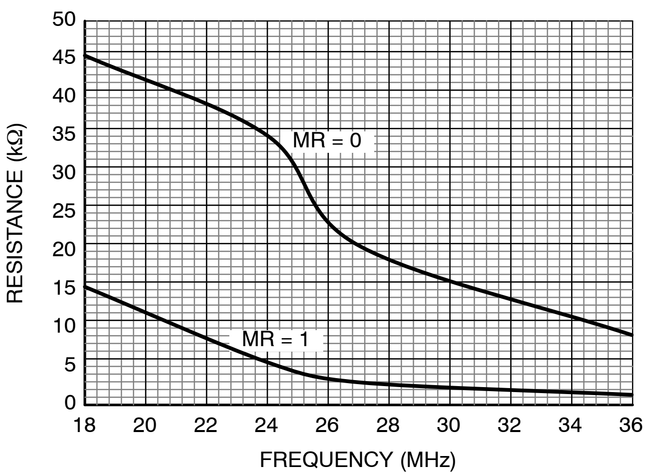


Figure 20. Frequency vs. Resistance (FS = 0)

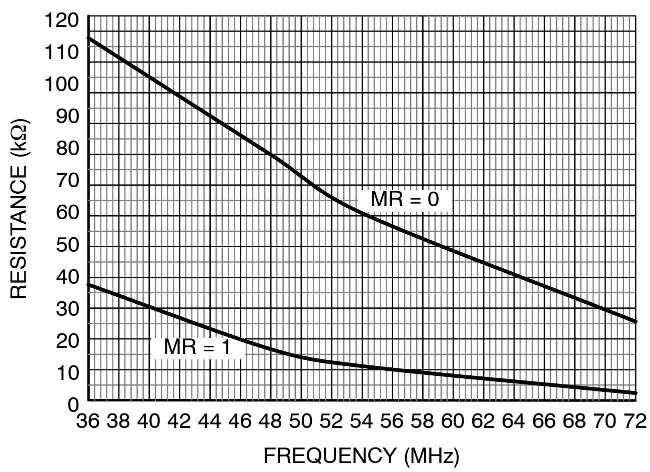


Figure 21. Frequency vs. Resistance (FS = 1)

NOTE: Device−to−Device variation of Deviation and Tskew is ±10%

SWITCHING WAVEFORMS

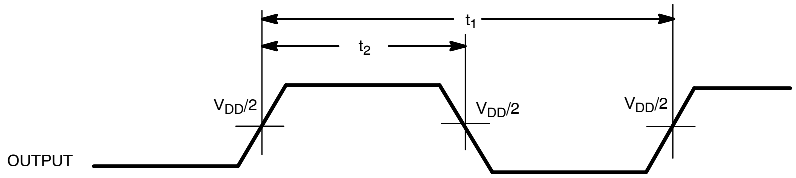


Figure 22. Duty Cycle Timing

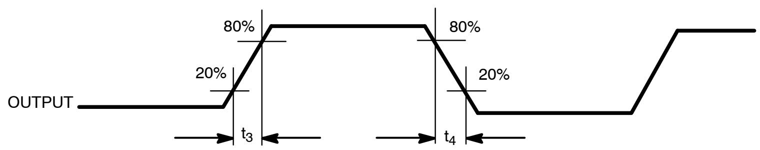
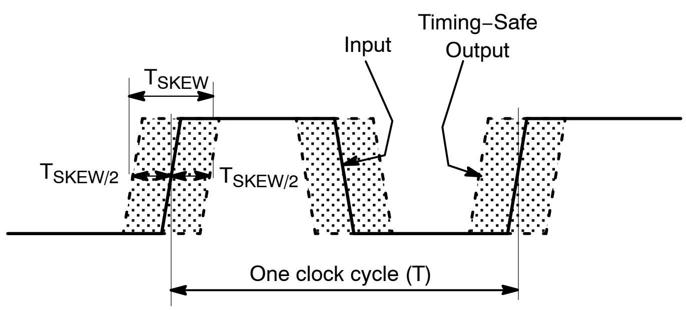


Figure 23. Output Rise/Fall Time



T_{SKEW} represents input−output skew
when spread spectrum is ON
For example, T_{SKEW} / 2 = 0.20 * T for an
Input clock of 24 MHz, translates in to
(1/24 MHz) * 0.20 = 8.33 ns

Figure 24. Input−Output Skew

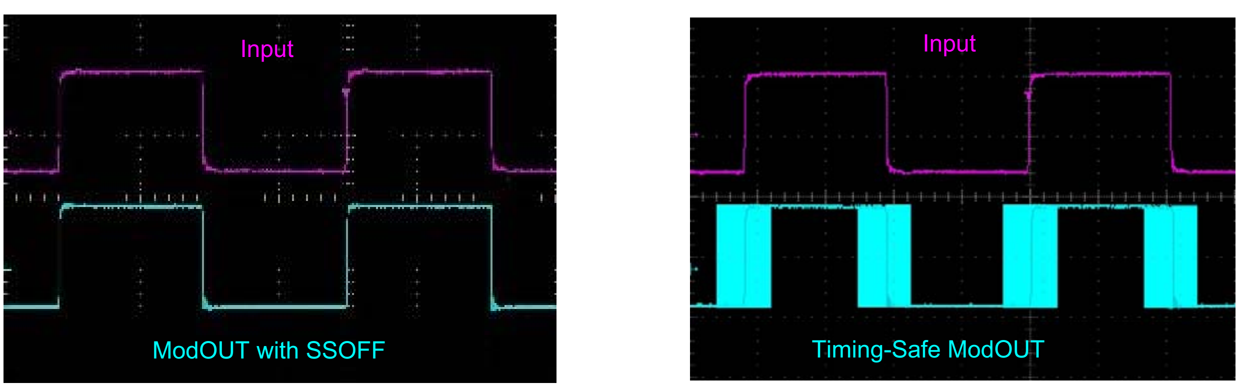
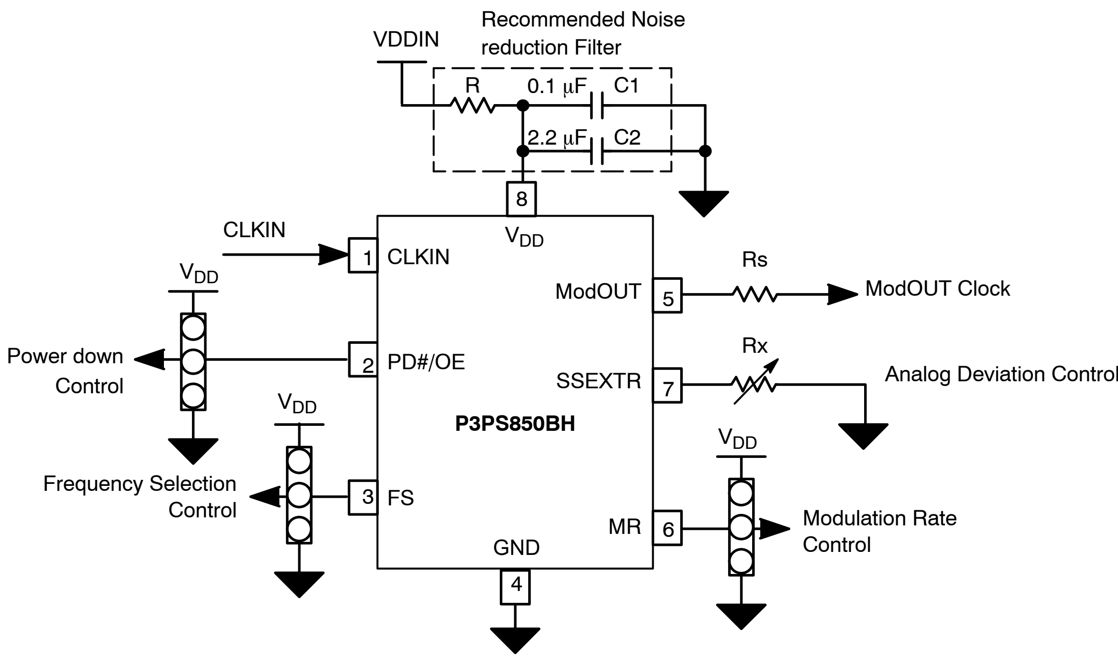


Figure 25. Typical Example of Timing−Safe Waveform



NOTE: Refer Pin Description table for Functionality details.

Figure 26. Typical Application Schematic

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated V_{DD} and GND planes.
- The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the V_{DD} pin as possible. No vias should be used between the decoupling capacitor and V_{DD} pin. The PCB trace to V_{DD} pin and the ground via should be kept as short as possible. All the V_{DD} pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in Figure 27.

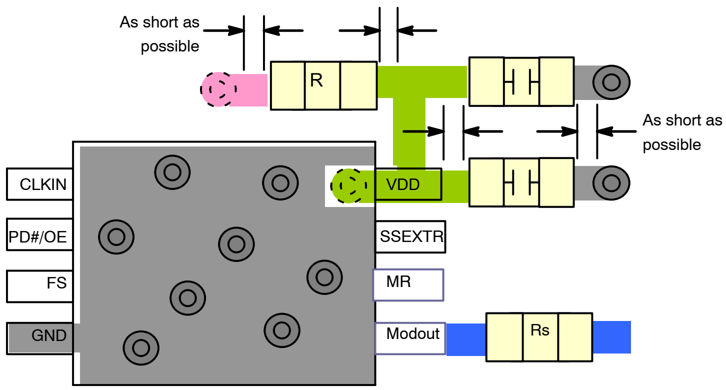


Figure 27.

ORDERING INFORMATION

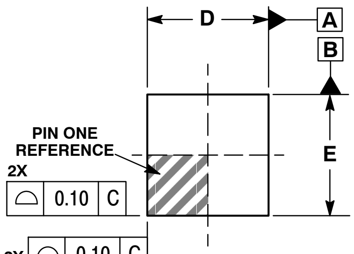
Part Number	Top Marking	Temperature	Package Type	Shipping†
P3PS850BHG−08CR	DG	−20°C to +85°C	8−Pin (2 mm x 2 mm) WDFN(TDFN) (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

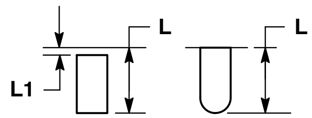
*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

PACKAGE DIMENSIONS

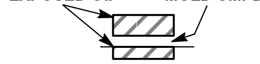
WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A



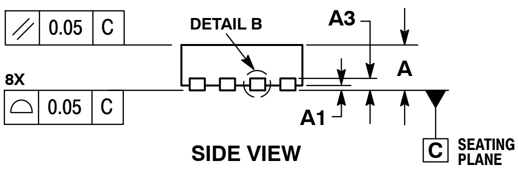
TOP VIEW



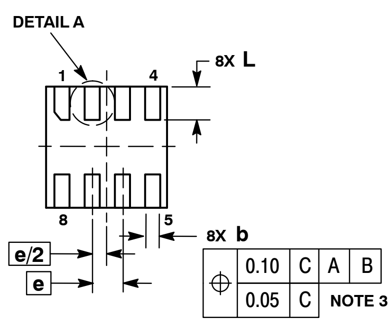
DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
OPTIONAL CONSTRUCTION



SIDE VIEW

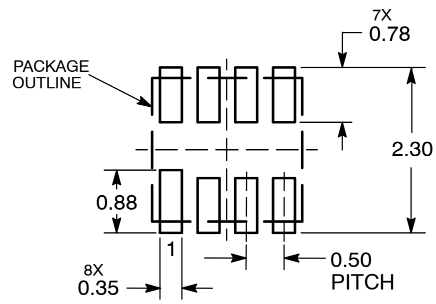


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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