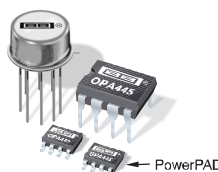




THE DATASHEET OF OPA445AU/2K5





High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- **WIDE-POWER SUPPLY RANGE:**
±10V to ±45V
- **HIGH SLEW RATE:** 15V/μs
- **LOW INPUT BIAS CURRENT:** 10pA
- **STANDARD-PINOUT TO-99, DIP, SO-8 PowerPAD™, AND SO-8 SURFACE-MOUNT PACKAGES**

APPLICATIONS

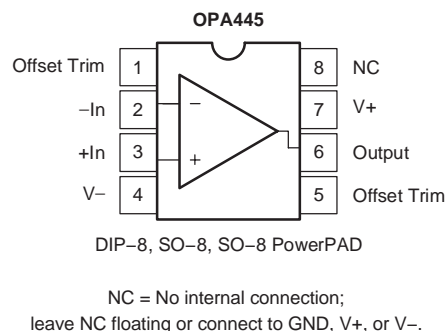
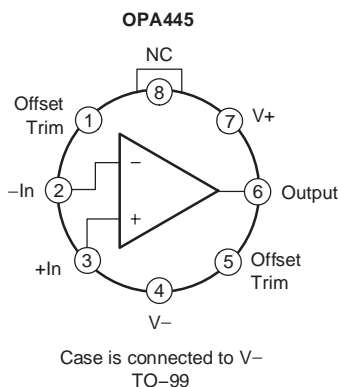
- TEST EQUIPMENT
- HIGH-VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING
- AUDIO
- PIEZO DRIVERS

DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high-voltage applications. FET input circuitry allows the use of high-impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is available in standard pinout TO-99, DIP-8, and SO-8 surface-mount packages as well as an SO-8 PowerPAD package for reducing junction temperature. It is fully specified from -25°C to +85°C and operates from -55°C to +125°C. A SPICE macromodel is available for design analysis (from www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments, Inc. All other trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS(1)

| | |
|--|------------------------|
| Power Supply | ±50V |
| Differential Input Voltage | ±80V |
| Input Voltage Range | ±V _S – 3V |
| Storage Temperature Range: M | –65°C to +150°C |
| P, U, DDA | –55°C to +125°C |
| Operating Temperature Range | –55°C to +125°C |
| Output Short-Circuit to Ground (T _J < +125°C) | Continuous |
| Junction Temperature: M | +175°C |
| Junction Temperature: P, U, DDA | +150°C |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

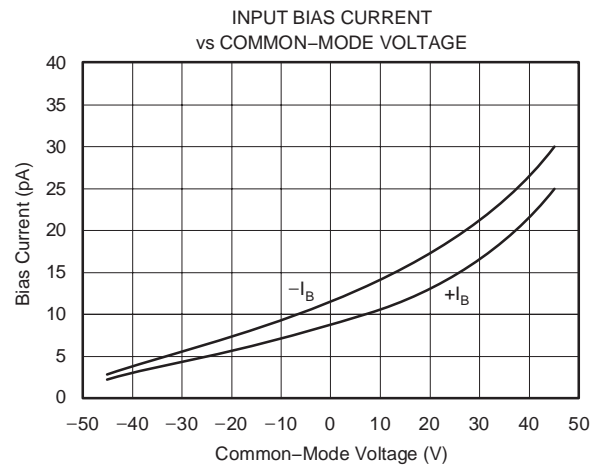
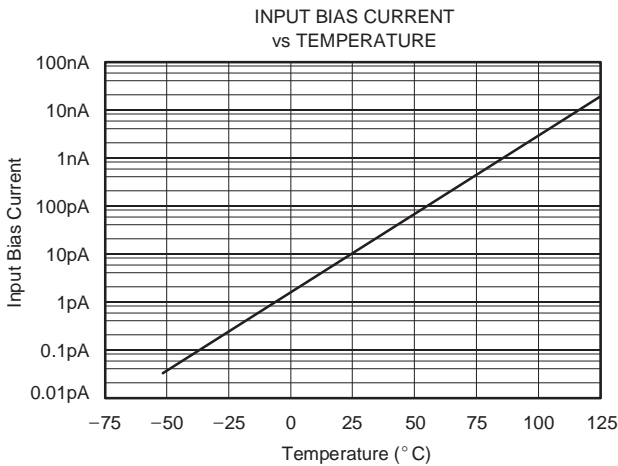
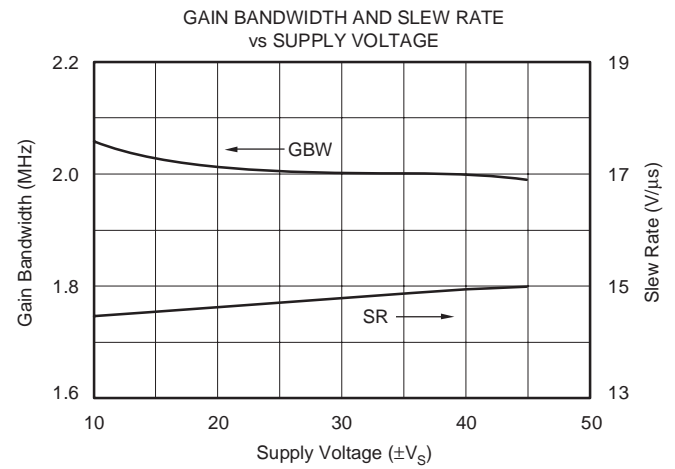
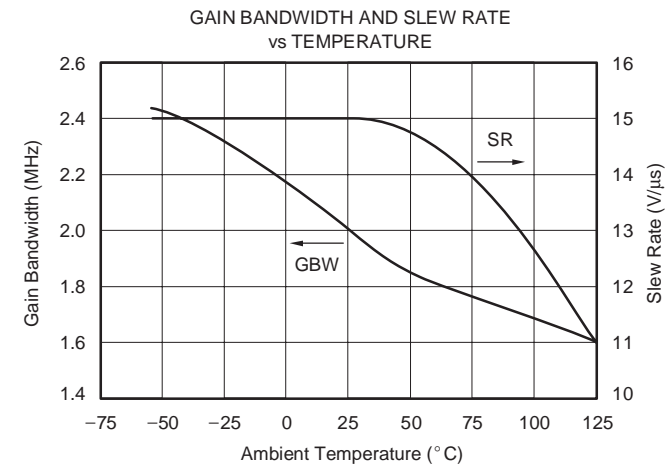
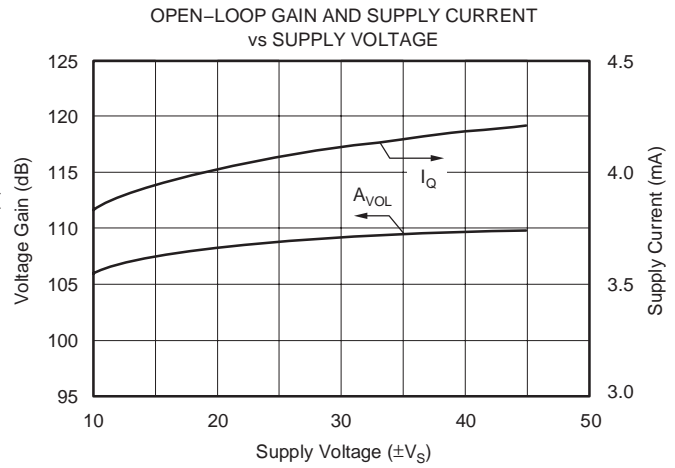
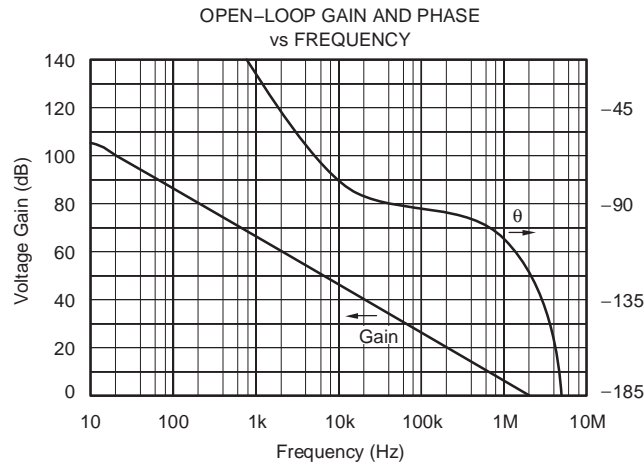
ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|------------|--------------------|--------------------|-----------------|
| OPA445AP | DIP-8 | P | OPA445AP |
| OPA445AU | SO-8 Surface-Mount | D | OPA445AU |
| OPA445ADDA | SO-8 PowerPAD | DDA | OPA445 |
| OPA445BM | TO-99 8-Pin | LMC | OPA445BM |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

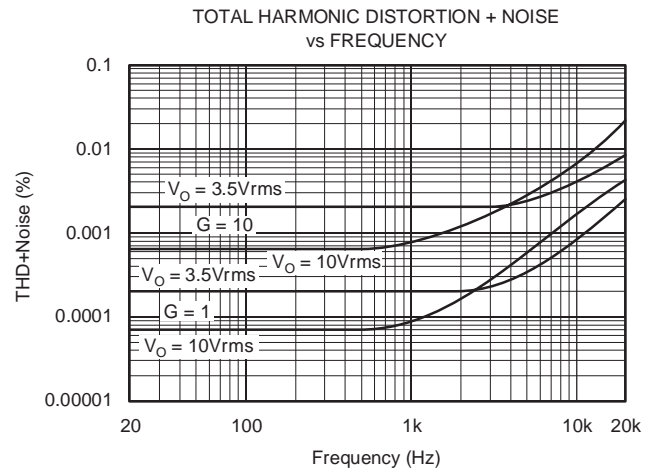
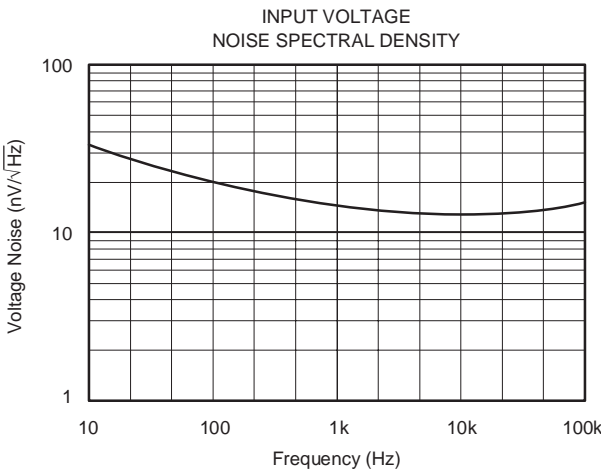
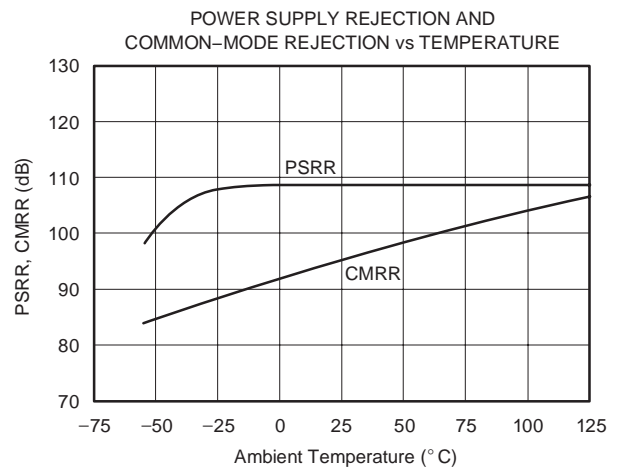
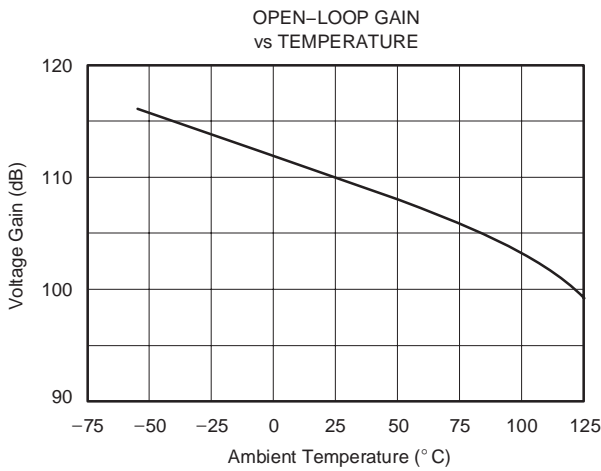
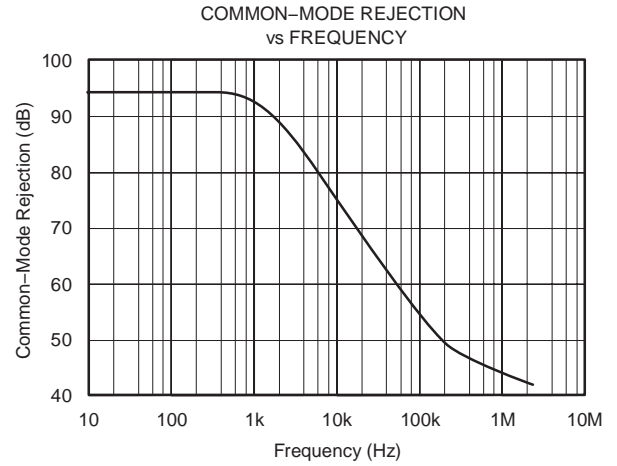
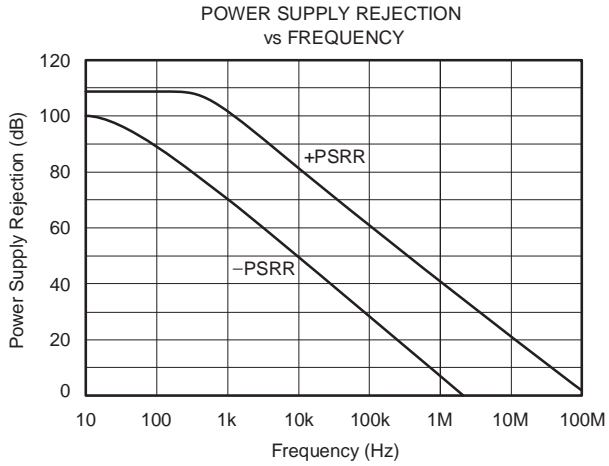
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 40\text{V}$, unless otherwise noted.



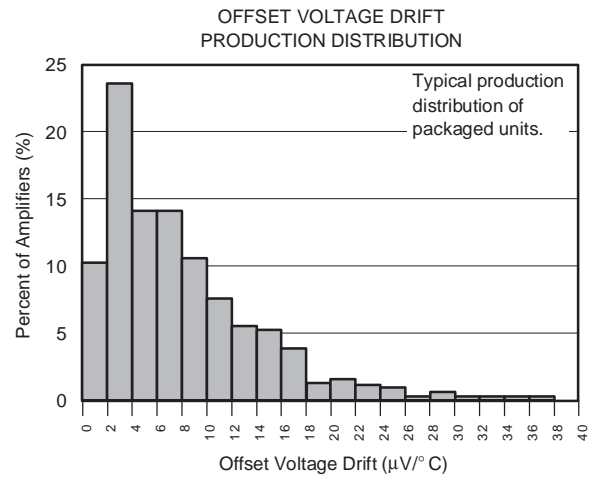
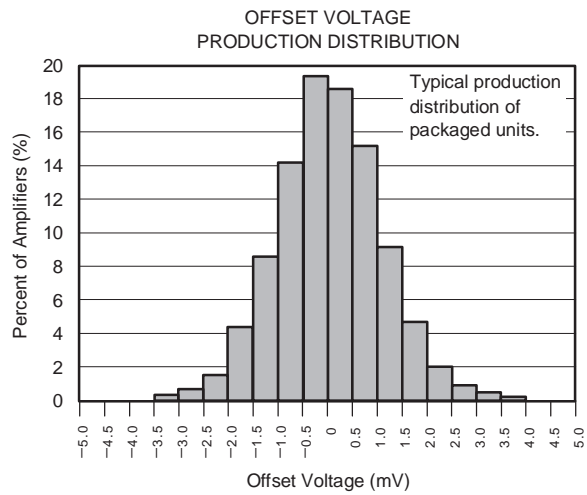
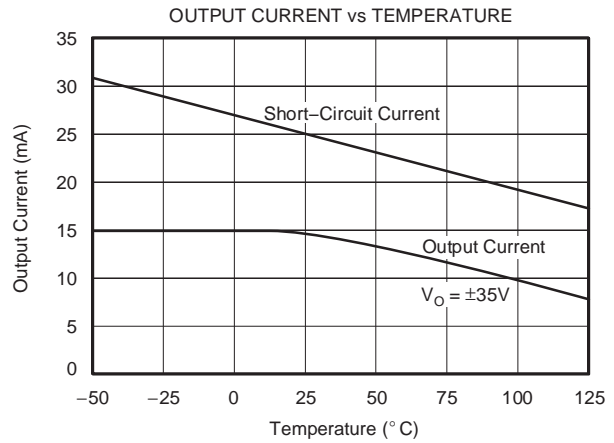
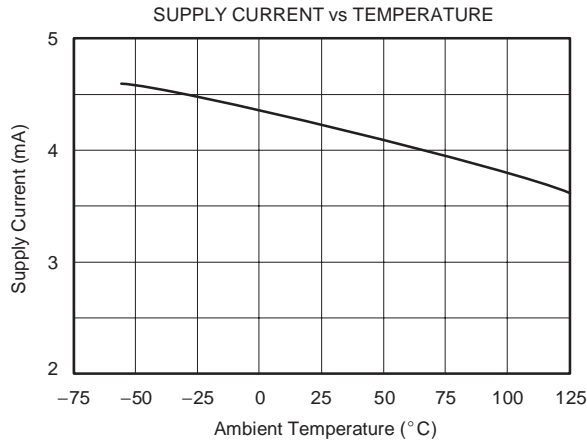
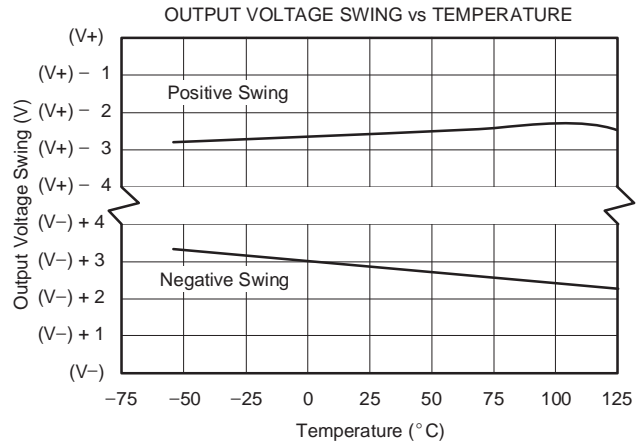
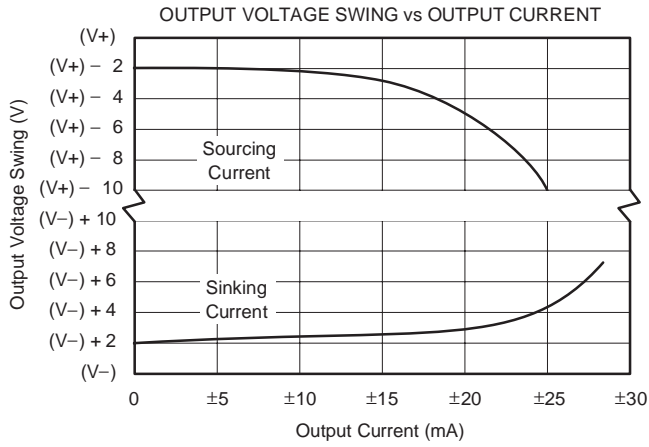
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 40\text{V}$, unless otherwise noted.



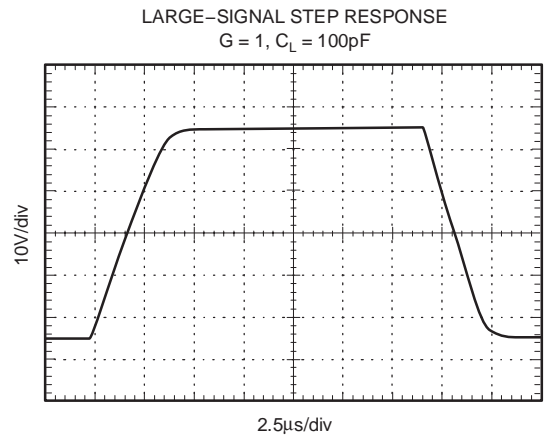
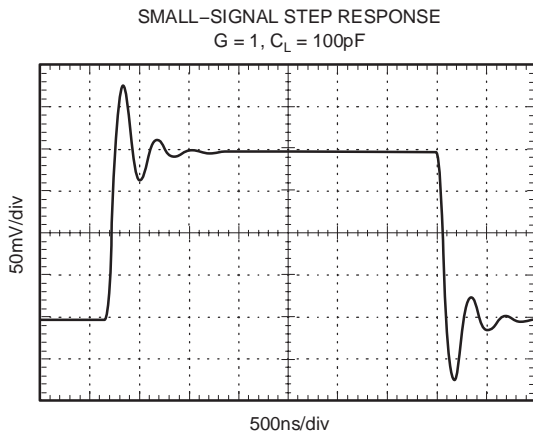
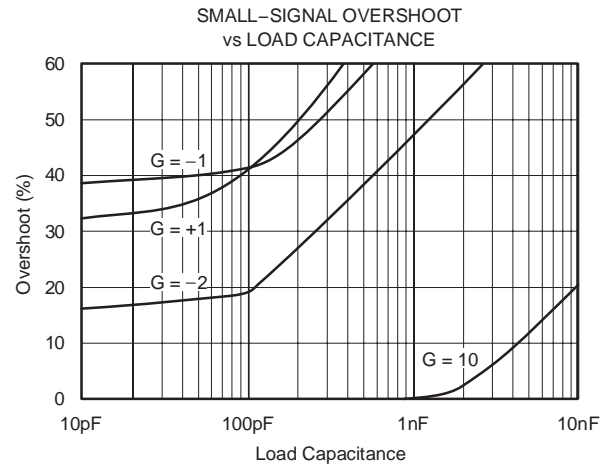
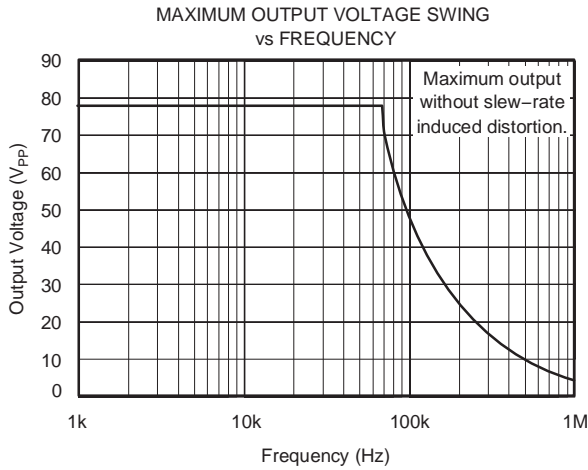
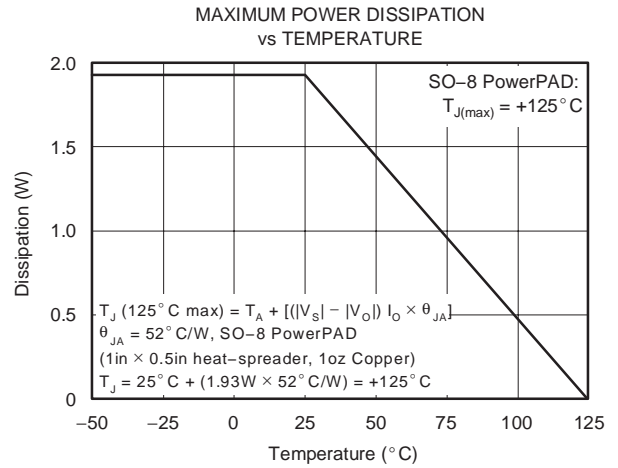
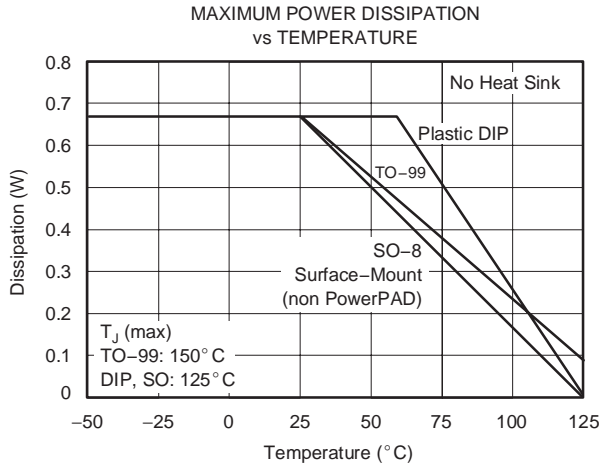
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 40\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 40\text{V}$, unless otherwise noted.



APPLICATIONS

Figure 1 shows the OPA445 connected as a basic noninverting amplifier. The OPA445 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used.

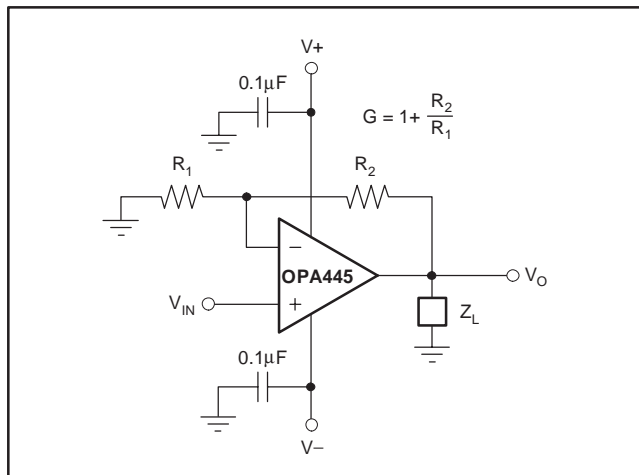


Figure 1. The OPA445 Configured as a Noninverting Amplifier

POWER SUPPLIES

The OPA445 may be operated from power supplies up to ±45V or a total of 90V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA445 can operate with as little as 20V between the supplies and with up to 90V between the supplies. For example, the positive supply could be set to 80V with the negative supply at -10V, or vice-versa.

INPUT PROTECTION

The inputs of conventional FET-input op amps should be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. This can occur if the input voltage exceeds the power supplies or there is an input voltage with $V_S = 0V$. Protection is easily accomplished with a resistor in series with the input. Care should be taken because the resistance in series with the input capacitance may affect stability. Many input signals are inherently current-limited; therefore, a limiting resistor may not be required.

OFFSET VOLTAGE TRIM

The OPA445 provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 2. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling system offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

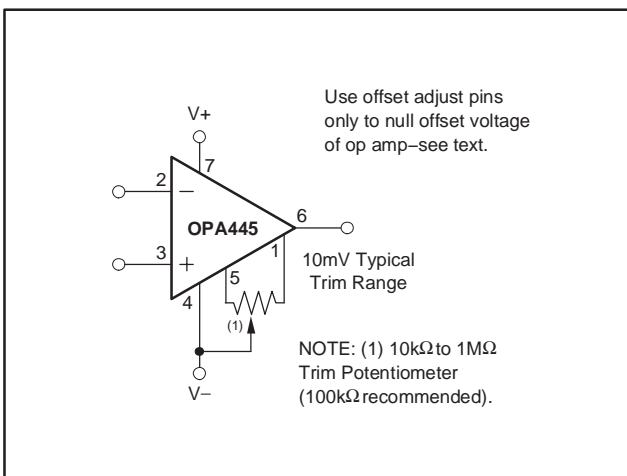


Figure 2. Offset Voltage Trim

CAPACITIVE LOADS

The dynamic characteristics of the OPA445 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 3 shows a circuit which preserves phase margin with capacitive load. The circuit does not suffer a voltage drop due to load current; however, input impedance is reduced at high frequencies. Consult Application Bulletin SBOA015, available for download at www.ti.com, for details of analysis techniques and application circuits.

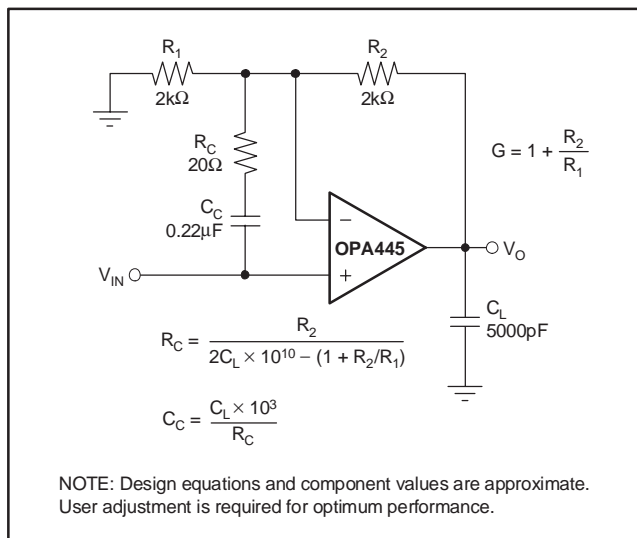


Figure 3. Driving Large Capacitive Loads

INCREASING OUTPUT CURRENT

In those applications where the 15mA of output current is not sufficient to drive the required load, output current can be increased by connecting two or more OPA445s in parallel as shown in Figure 4. Amplifier A1 is the master amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the slave, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 5 is capable of supplying output currents up to 1A.

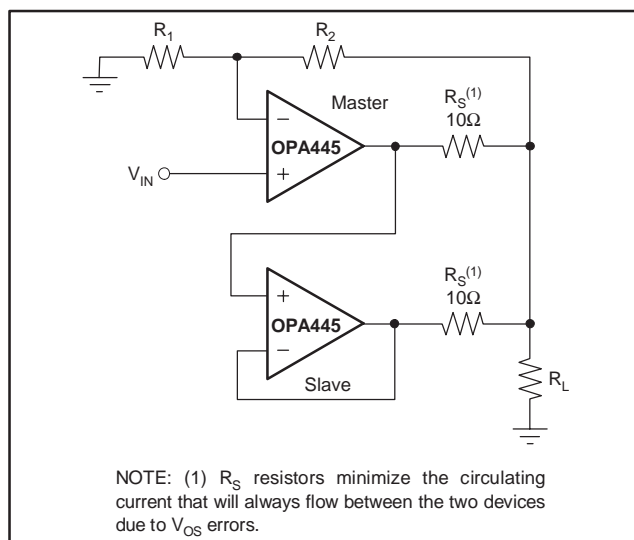


Figure 4. Parallel Amplifiers Increase Output Current Capability

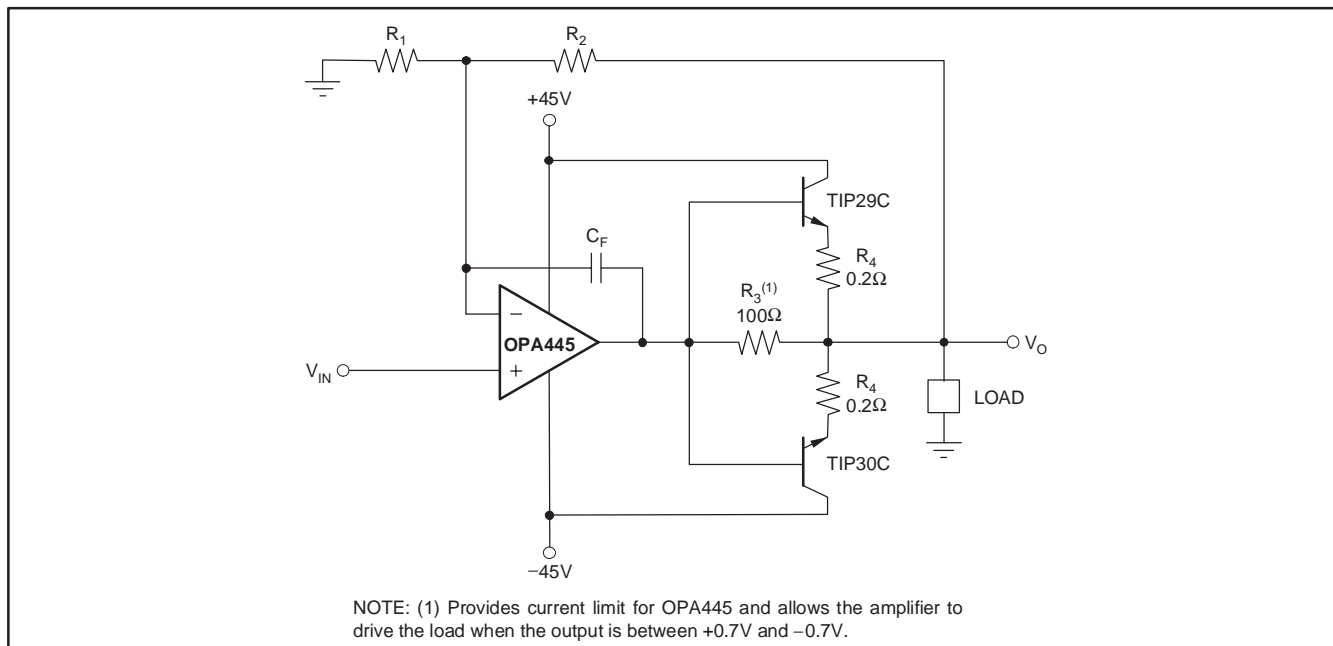


Figure 5. External Output Transistors Boost Output Current Up to 1 Amp

SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistors, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 6 through Figure 10) illustrates the permissible range of voltage and current. The curves shown represent devices soldered to a printed circuit board (PCB) with no heat sink. Increasing printed circuit trace area or the use of a heat sink (TO-99 package) can significantly reduce thermal resistance (θ), resulting in increased output current for a given output voltage (see Figure 11, Figure 12, and the *Heat Sink* section).

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ($V+$ or $V-$) across the conducting transistor and produces a typical output current of 25mA. With $\pm 40V$ power supplies, this creates an internal dissipation of 1W. This exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, a heat sink is required. For further insight on SOA, consult Application Bulletin SBOA022 (available for download at www.ti.com).

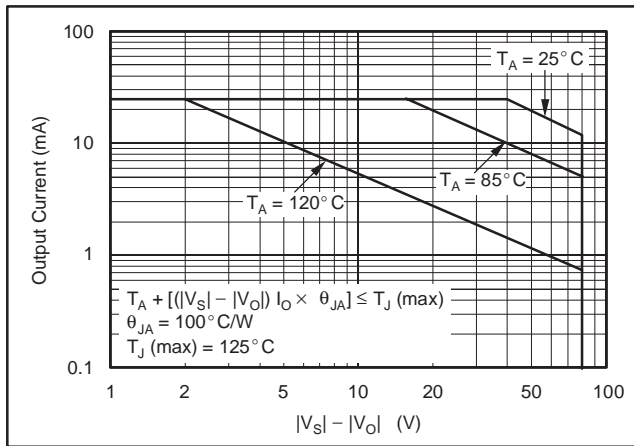


Figure 6. DIP-8 Safe Operating Area

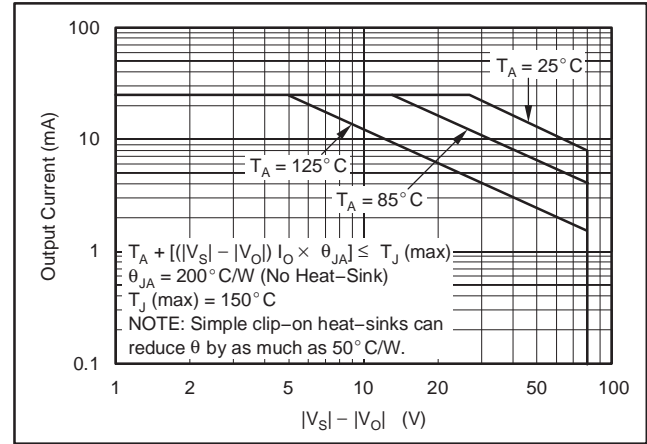


Figure 7. TO-99 Safe Operating Area

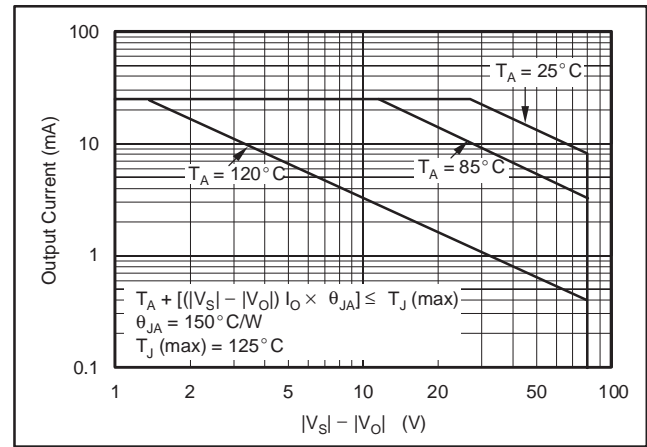


Figure 8. SO-8 (non PowerPAD) Safe Operating Area

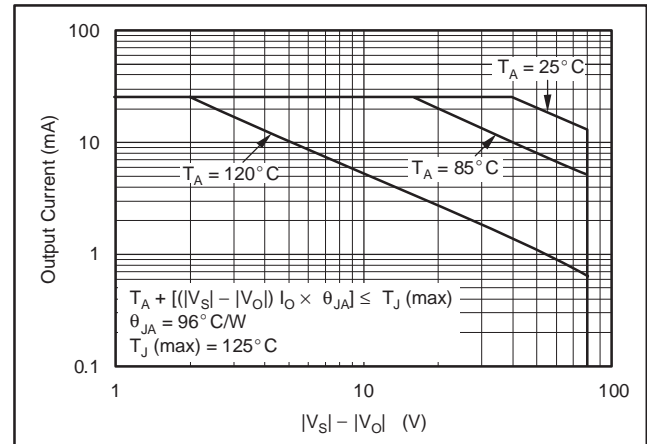


Figure 9. SO-8 PowerPAD Safe Operating Area (no heat-spreader, no airflow)

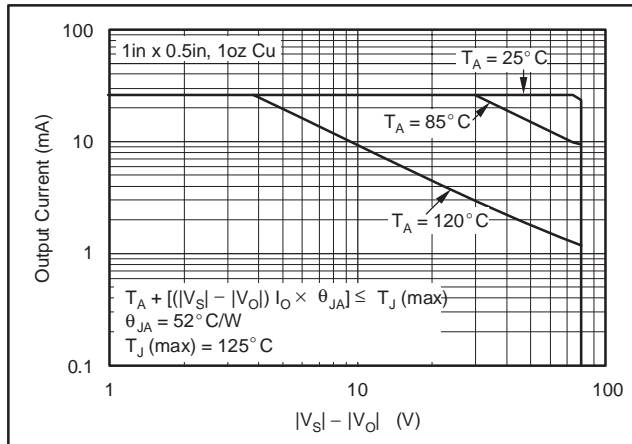


Figure 10. SO-8 PowerPAD Safe Operating Area (with heat-spreader, no airflow)

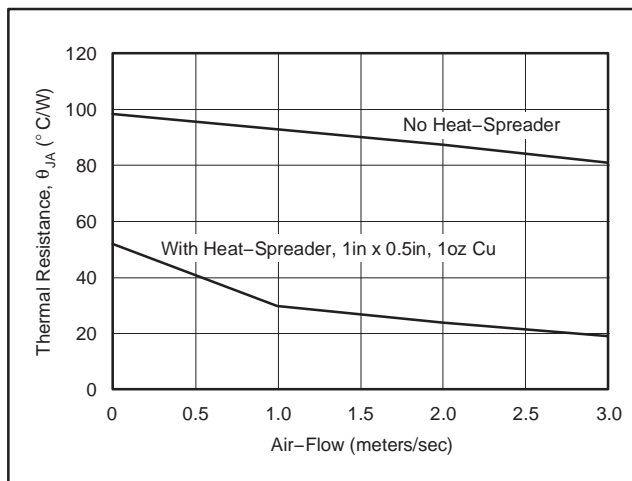


Figure 11. SO-8 PowerPAD Thermal Resistance (with and without heat-spreader)

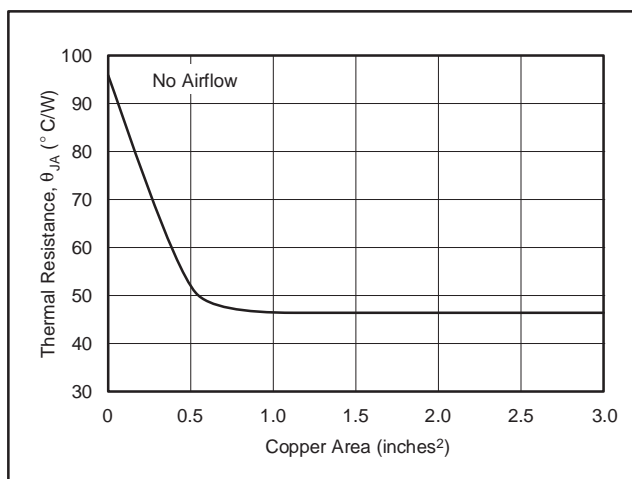


Figure 12. Thermal Resistance vs Circuit Board Copper Area

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin SBOA022 explains how to calculate or measure dissipation with unusual loads or signals.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from $\pm 15V$ supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a large voltage is impressed across the conducting output transistor. Applications with large power dissipation may require a heat-sink.

HEAT SINKING

Power dissipated in the OPA445 will cause the junction temperature to rise. For reliable operation junction temperature should be limited to 125°C, maximum (150°C for TO-99 package). Some applications will require a heat-sink to assure that the maximum operating junction temperature is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the following equation:

$$T_J = T_A + P_D \theta_{JA} \quad (1)$$

Package thermal resistance, θ_{JA} , is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks (such as a Thermalloy 2257) can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W. The SO-8 PowerPAD package will provide lower thermal resistance, especially with a simple heat-spreader—even lower with a heat-sink. For additional information on determining heat-sink requirements, consult Application Bulletin SBOA021.

PowerPAD THERMALLY-ENHANCED PACKAGE

In addition to the SO-8, DIP-8, and TO-99 packages, the OPA445 also comes in an SO-8 PowerPAD. The SO-8 PowerPAD is a standard-size SO-8 package where the exposed leadframe on the bottom of the package can be soldered directly to the PCB to create an extremely low thermal resistance. This architecture enhances the OPA445's power dissipation capability significantly and eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques. NOTE: Since the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA445 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Soldering the device to the PCB provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC; see Figure 13. This design provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

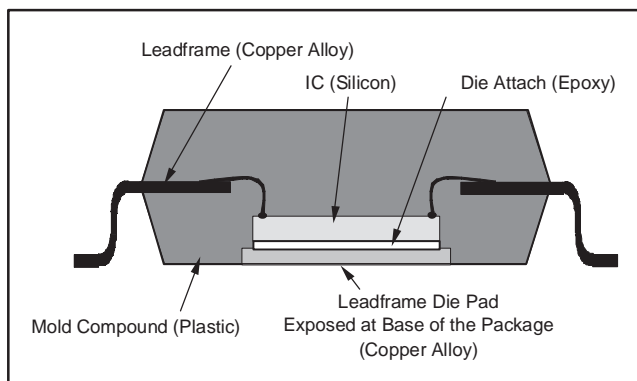


Figure 13. Section View of a PowerPAD Package

GENERAL PowerPAD LAYOUT GUIDELINES

The OPA445 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Follow these steps:

1. The PowerPAD must be connected to the most negative supply voltage on the device, V^- .
2. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
3. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package is shown in Figure 14. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA445 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
5. Connect all holes to the internal power plane of the correct voltage potential (V^-).
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA445 PowerPAD package should make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

9. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see technical brief SLMA002 *PowerPAD Thermally-Enhanced Package* available for download at www.ti.com.

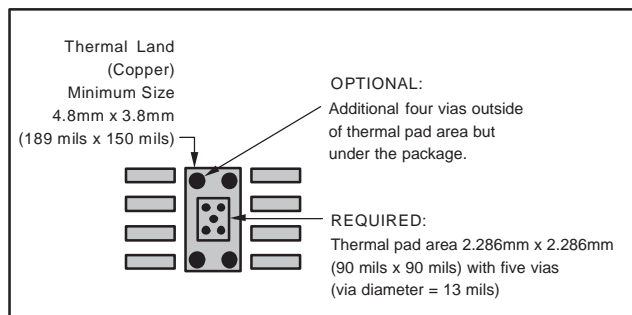


Figure 14. 8-Pin PowerPAD PCB Etch and Via Pattern

TYPICAL APPLICATIONS

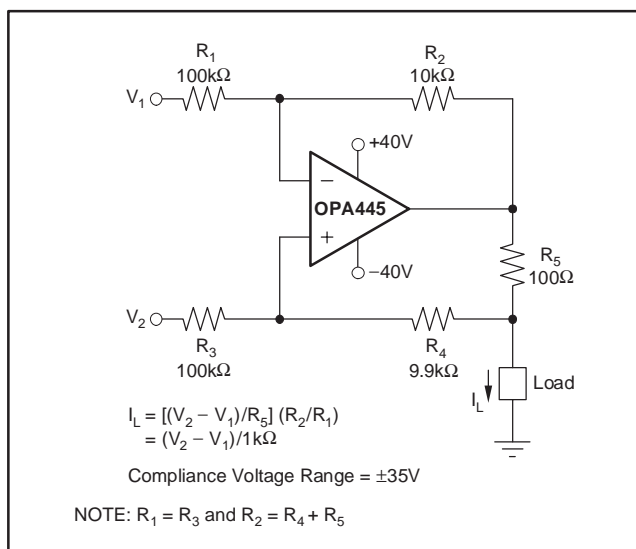


Figure 15. Voltage-to-Current Converter

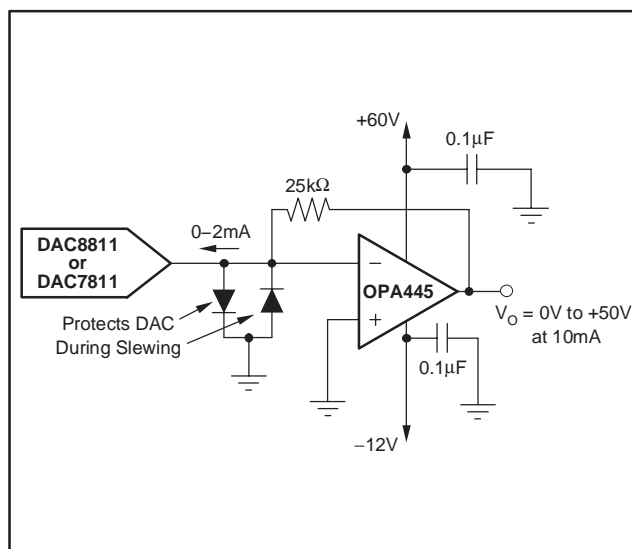


Figure 16. Programmable Voltage Source

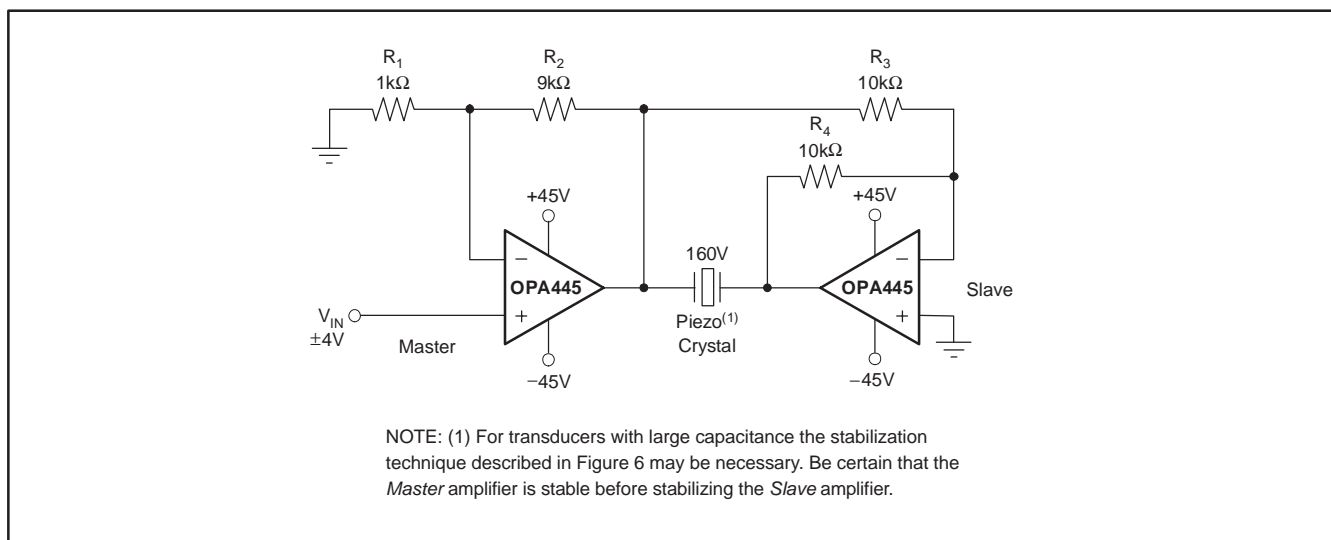


Figure 17. Bridge Circuit Doubles Voltage for Piezo Crystals

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| OPA445ADDA | ACTIVE | SO PowerPAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | OPA445 | Samples |
| OPA445ADDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | OPA445 | Samples |
| OPA445AP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | OPA445AP | Samples |
| OPA445APG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | OPA445AP | Samples |
| OPA445AU | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | OPA 445AU | Samples |
| OPA445AU/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | OPA 445AU | Samples |
| OPA445AUG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to 125 | OPA 445AU | Samples |
| OPA445BM | ACTIVE | TO-99 | LMC | 8 | 20 | Green (RoHS & no Sb/Br) | AU | N / A for Pkg Type | | OPA445BM | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

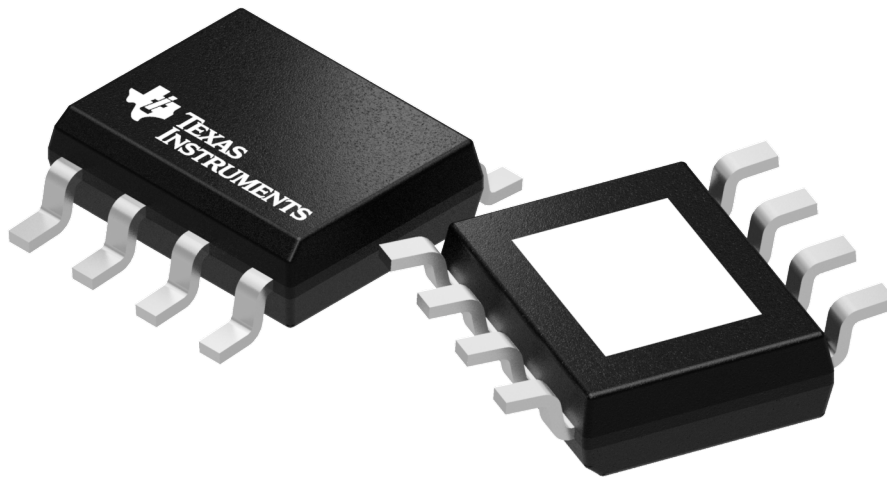
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA445ADDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA445AU/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

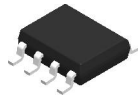

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA445ADDAR | SO PowerPAD | DDA | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA445AU/2K5 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

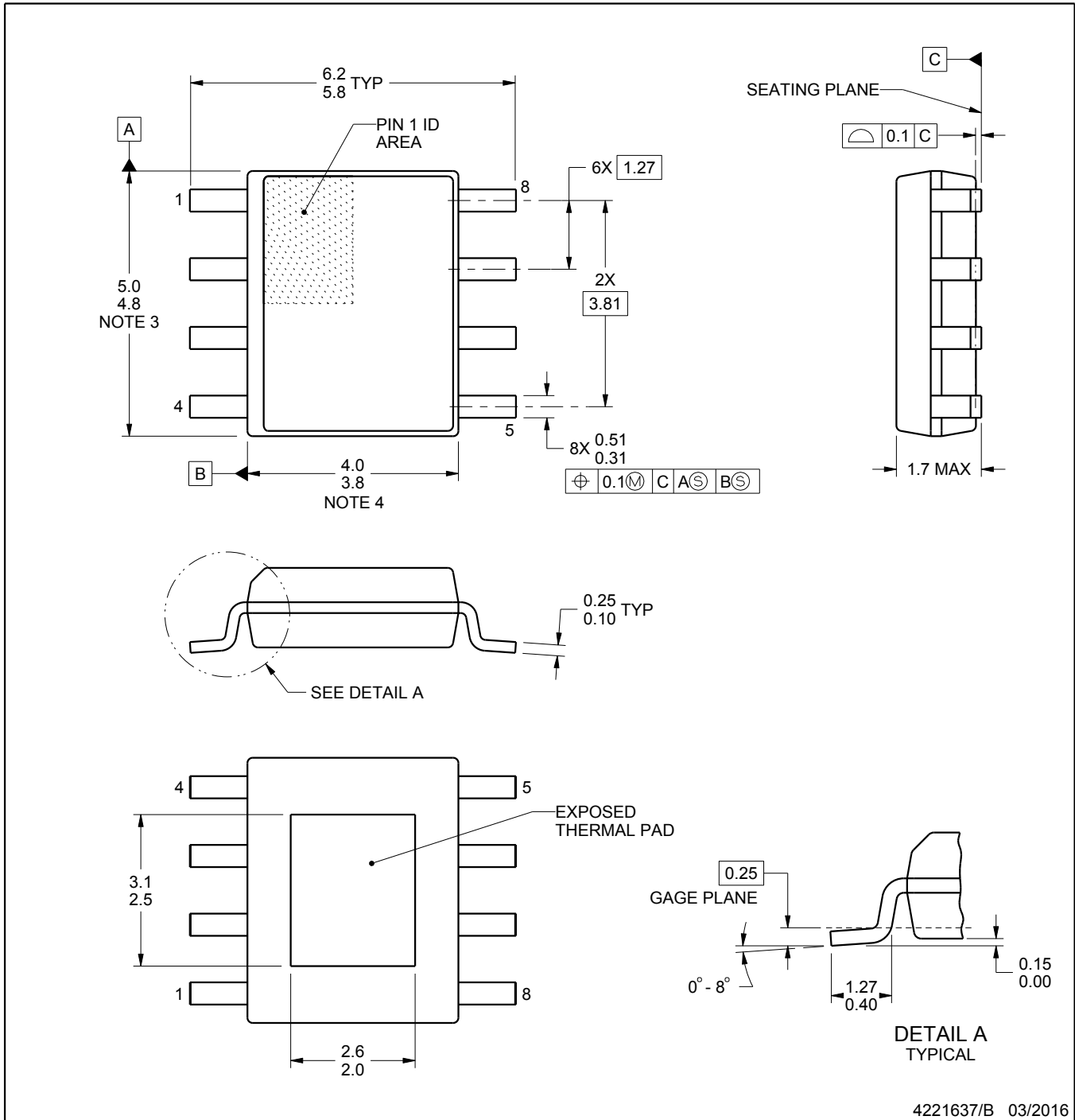
DDA0008J



PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

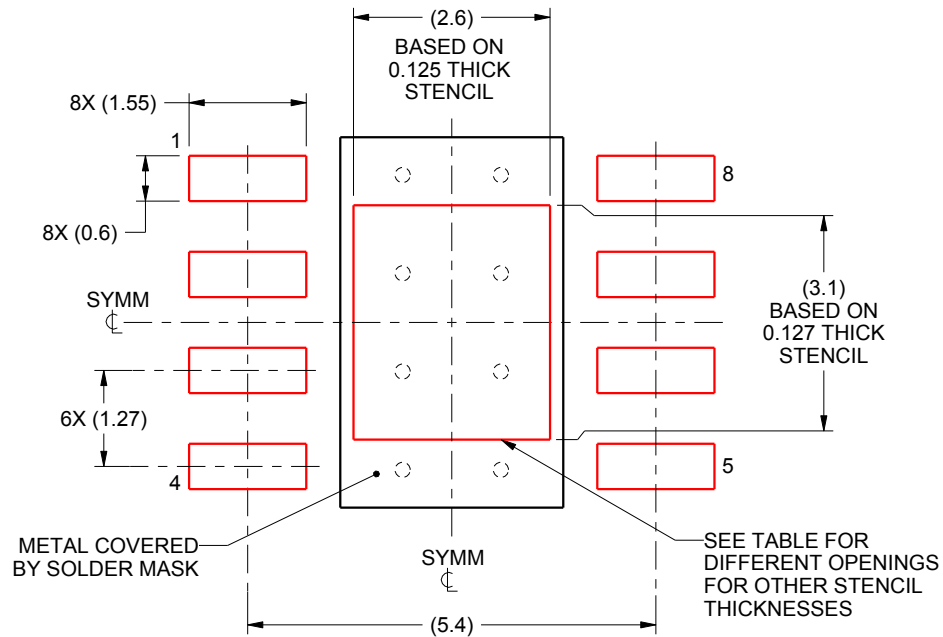
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 2.91 X 3.47 |
| 0.125 | 2.6 X 3.1 (SHOWN) |
| 0.150 | 2.37 X 2.83 |
| 0.175 | 2.20 X 2.62 |

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

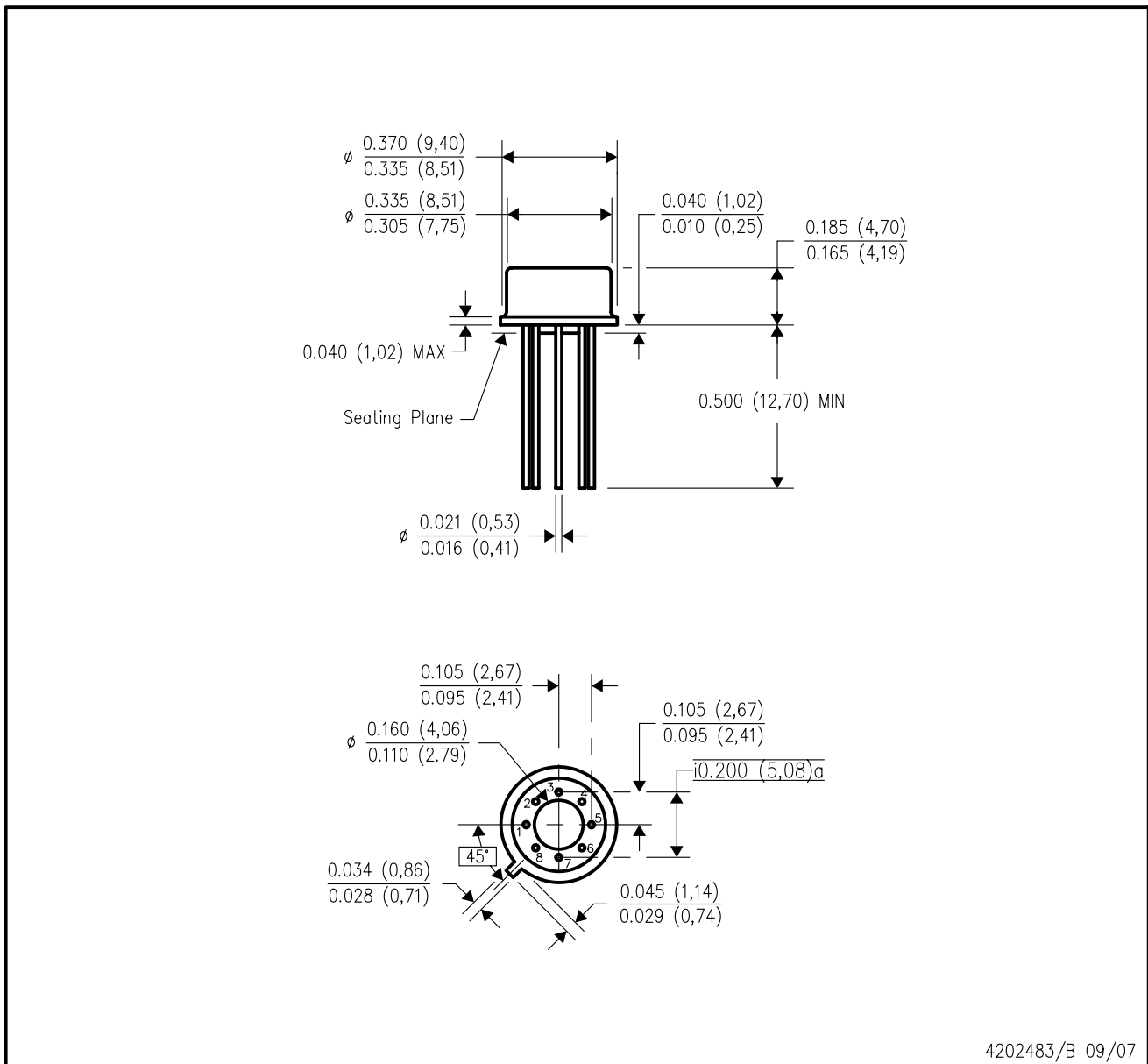
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - D. Pin numbers shown for reference only. Numbers may not be marked on package.
 - E. Falls within JEDEC MO-002/TO-99.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View OPA445AU/2K5 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management