# THE DATASHEET OF

# OPA404KP

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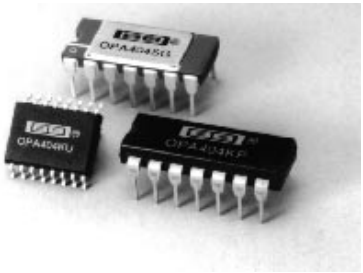


# OPA404

# Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

## FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/µs
- LOW OFFSET: ±750µV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5µs to 0.01%
- STANDARD QUAD PINOUT

## APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

## DESCRIPTION

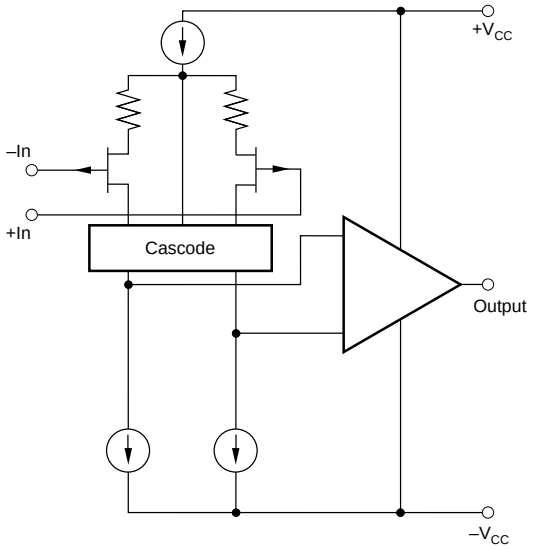
The OPA404 is a high performance monolithic ***Difet***®(dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.




OPA404 Simplified Circuit
(Each Amplifier)

***Difet***®, Burr-Brown Corp.
BIFET®, National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
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SBOS149

# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±15VDC and $T_A$ = +25°C unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU (1) | | | OPA404BG | | | OPA404SG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT** | | | | | | | | | | | |
| **NOISE** | | | | | | | | | | | |
| Voltage: $f_O$ = 10Hz | | | 32 | | | * | | | * | | nV/√Hz |
| $f_O$ = 100Hz | | | 19 | | | * | | | * | | nV/√Hz |
| $f_O$ = 1kHz | | | 15 | | | * | | | * | | nV/√Hz |
| $f_O$ = 10kHz | | | 12 | | | * | | | * | | nV/√Hz |
| $f_B$ = 10Hz to 10kHz | | | 1.4 | | | * | | | * | | µVrms |
| $f_B$ = 0.1Hz to 10Hz | | | 0.95 | | | * | | | * | | µVp-p |
| Current: $f_B$ = 0.1Hz to 10Hz | | | 12 | | | * | | | * | | fA, p-p |
| $f_O$ = 0.1Hz thru 20kHz | | | 0.6 | | | * | | | * | | fA/√Hz |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±260 | ±1mV | | * | ±750 | | * | * | µV |
| KP, KU | | | ±750 | ±2.5mV | | | | | | | µV |
| Average Drift | $T_A = T_{MIN}$ to $T_{MAX}$ | | ±3 | | | * | | | * | | µV/°C |
| KP, KU | | | ±5 | | | | | | | | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 12V to 18V | 80 | 100 | | 86 | * | | * | * | | dB |
| KP, KU | | 76 | 100 | | | | | | | | dB |
| Channel Separation | 100Hz, $R_L$ = 2kΩ | | 125 | | | * | | | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±1 | ±8 | | * | ±4 | | * | * | pA |
| KP, KU | | | ±1 | ±12 | | | | | | | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.5 | 8 | | * | 4 | | * | * | pA |
| KP, KU | | | 0.5 | 12 | | | | | | | pA |
| **IMPEDANCE** | | | | | | | | | | | |
| Differential | | | $10^{13}$ \|\| 1 | | | * | | | * | | Ω \|\| pF |
| Common-Mode | | | $10^{14}$ \|\| 3 | | | * | | | * | | Ω \|\| pF |
| **VOTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10.5 | +13, –11 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 88 | 100 | | 92 | * | | * | * | | dB |
| KP, KU | | 84 | 100 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L \geq$ 2kΩ | 88 | 100 | | 92 | * | | * | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Gain Bandwidth | Gain = 100 | 4 | 6.4 | | 5 | * | | * | * | | MHz |
| Full Power Response | 20Vp-p, $R_L$ = 2kΩ | | 570 | | | * | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, $R_L$ = 2kΩ | 24 | 35 | | 28 | * | | * | * | | V/µs |
| Settling Time: 0.1% | Gain = –1, $R_L$ = 2kΩ | | 0.6 | | | * | | | * | | µs |
| 0.01% | $C_L$ = 100 pF, 10V Step | | 1.5 | | | * | | | * | | µs |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.5 | +13.2, –13.8 | | * | * | | * | * | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±10 | | * | * | | * | * | | mA |
| Output Resistance | 1MHz, Open Loop | | 80 | | | * | | | * | | Ω |
| Load Capacitance Stability | Gain = +1 | | 1000 | | | * | | | * | | pF |
| Short Circuit Current | | ±10 | ±27 | ±40 | * | * | * | * | * | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | | | ±15 | | | * | | | * | | VDC |
| Voltage Range, Derated Performance | | ±5 | | ±18 | * | | * | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 9 | 10 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification | Ambient Temperature | –25 | | +85 | * | | * | –55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| Operating | Ambient Temperature | –55 | | +125 | * | | * | * | | * | °C |
| KP, KU | | –25 | | +85 | | | | | | | °C |
| Storage | Ambient Temperature | –65 | | +150 | * | | * | * | | * | °C |
| KP, KU | | –40 | | +125 | | | | | | | °C |
| θ Junction-Ambient | | | 100 | | | * | | | * | | °C/W |
| KP, KU | | | 120/100 | | | | | | | | °C/W |

*Specifications same as OPA404AG.
NOTE: (1) OPA404KU may be marked OPA404U.

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## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±15VDC and $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.

| PARAMETER | CONDITIONS | OPA404AG, KP, KU | | | OPA404BG | | | OPA404SG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification Range | Ambient Temperature | –25 | | +85 | * | | * | –55 | | +125 | °C |
| KP, KU | | 0 | | +70 | | | | | | | °C |
| **INPUT** | | | | | | | | | | | |
| **OFFSET VOLTAGE** | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±450 | 2mV | | * | ±1.5mV | | ±550 | ±2.5mV | µV |
| KP KU | | | ±1 | ±3.5 | | | | | | | mV |
| Average Drift | | | ±3 | | | * | | | * | | µV/°C |
| KP, KU | | | ±5 | | | | | | | | µV/°C |
| Supply Rejection | | 75 | 96 | | 80 | * | | 70 | 93 | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | ±32 | ±200 | | * | ±100 | | ±500 | ±5nA | pA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 17 | 100 | | * | 50 | | 260 | 2.5nA | pA |
| **VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±10 | ±12.7, –10.6 | | * | * | | ±10 | +12.6, –10.5 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±10VDC | 82 | 99 | | 86 | * | | 80 | 88 | | dB |
| KP, KU | | 80 | 99 | | | | | | | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ ≥ 2kΩ | 82 | 94 | | 86 | * | | 80 | 88 | | dB |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 2kΩ | ±11.5 | ±12.9, –13.8 | | * | * | | ±11 | +12.7, –13.8 | | V |
| Current Output | $V_O$ = ±10VDC | ±5 | ±9 | | * | * | | * | ±8 | | mA |
| Short Circuit Current | $V_O$ = 0VDC | ±8 | ±20 | ±50 | * | * | * | * | * | * | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 9.3 | 10.5 | | * | * | | 9.4 | 11 | mA |

* Specification same as OPA404AG.

## ORDERING INFORMATION

| MODEL | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| OPA404KP | 14-Pin Plastic DIP | 0°C to +70°C |
| OPA404KU(1) | 16-Pin Plastic SOIC | 0°C to +70°C |
| OPA404AG | 14-Pin Ceramic DIP | –25°C to +85°C |
| OPA404BG | 14-Pin Ceramic DIP | –25°C to +85°C |
| OPA404SG | 14-Pin Ceramic DIP | –55°C to +125°C |

NOTE: (1) OPA404KU may be marked OPA404U.

## PACKAGE INFORMATION

| MODEL | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA404KP | 14-Pin Plastic DIP | 010 |
| OPA404KU(2) | 16-Pin Plastic SOIC | 211 |
| OPA404AG | 14-Pin Ceramic DIP | 169 |
| OPA404BG | 14-Pin Ceramic DIP | 169 |
| OPA404SG | 14-Pin Ceramic DIP | 169 |

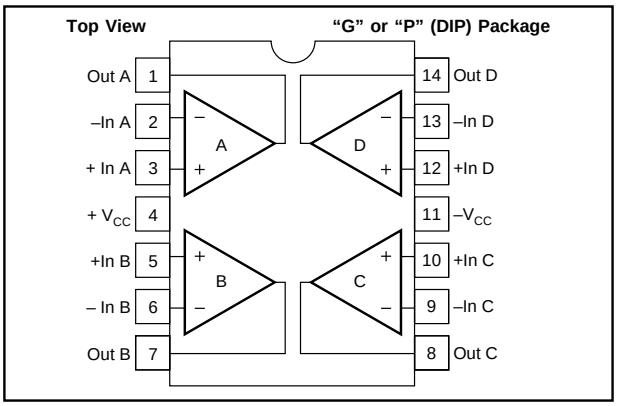
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

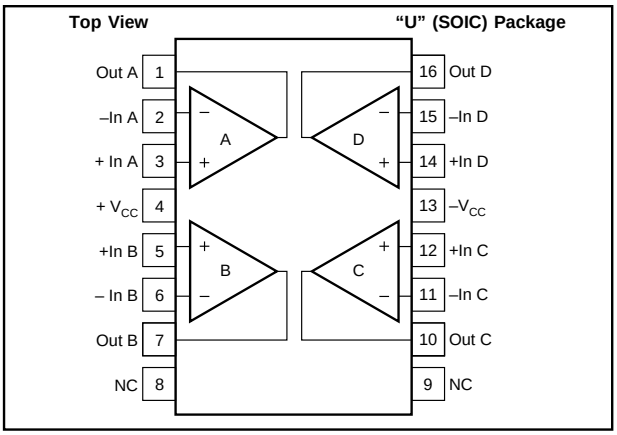
## ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation(1) ..... 1000mW
Differential Input Voltage(2) ..... ±36VDC
Input Voltage Range(2) ..... ±18VDC
Storage Temperature Range ... P, U = –40°C/+125°C, G = –65°C/+150°C
Operating Temperature Range .. P, U = –25°C/+85°C, G = –55°C/+125°C
Lead Temperature (soldering, 10s) ..... 300°C
SOIC (soldering, 3s) ..... +260°C
Output Short-Circuit Duration(3) ..... Continuous
Junction Temperature ..... +175°C

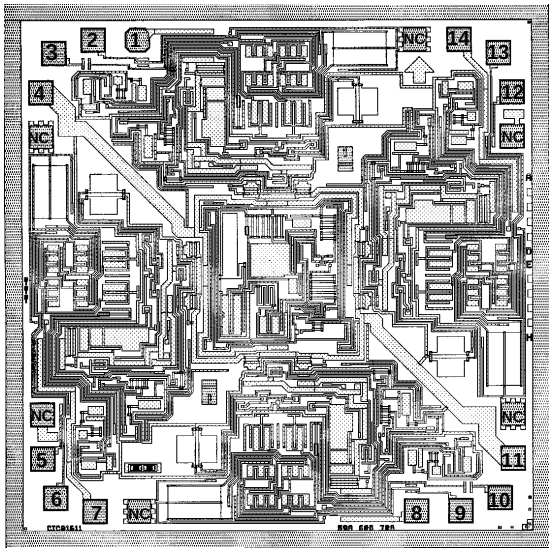
NOTES: (1) Packages must be derated based on $\theta_{JC}$ = 30°C/W or $\theta_{JA}$ = 120°C/W. (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to: 18V > $V_{IN}$ > –$V_{CC}$ – 8V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and $T_J$.

## PIN CONFIGURATION



## DICE INFORMATION




OPA404 DIE TOPOGRAPHY

| PAD | FUNCTION | PAD | FUNCTION |
|---|---|---|---|
| 1 | Output A | 8 | Output C |
| 2 | –Input A | 9 | –Input C |
| 3 | +Input A | 10 | +Input C |
| 4 | $+V_{CC}$ | 11 | $-V_{CC}$ |
| 5 | +Input B | 12 | +Input D |
| 6 | –Input B | 13 | –Input D |
| 7 | Output B | 14 | Output D |

**Substrate Bias:** $-V_{CC}$
NC: No connection

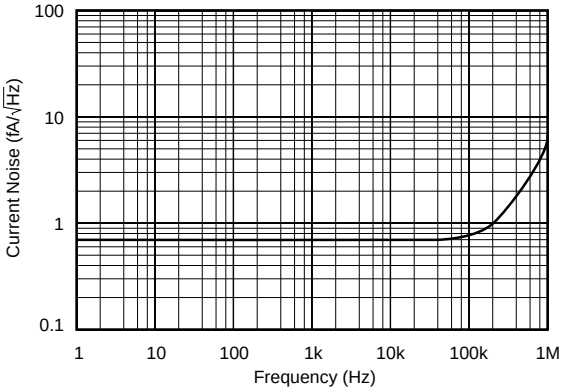
### MECHANICAL INFORMATION

| | MILS (0.001") | MILLIMETERS |
|---|---|---|
| Die Size | 108 x 108 ±5 | 2.74 x 2.74 ±0.13 |
| Die Thickness | 20 ±3 | 0.51 ±0.08 |
| Min. Pad Size | 4 x 4 | 0.10 x 0.10 |
| Backing | | None |

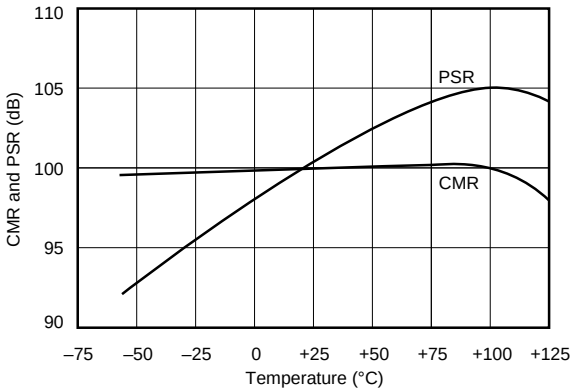
# TYPICAL PERFORMANCE CURVES

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

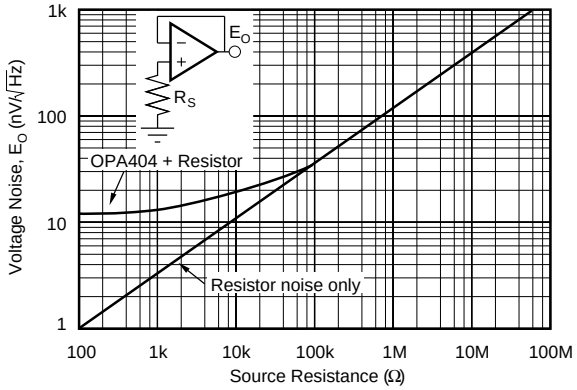
INPUT CURRENT NOISE SPECTRAL DENSITY



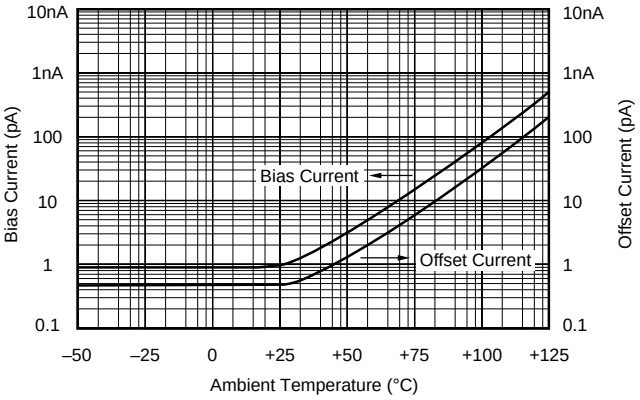

POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE




TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



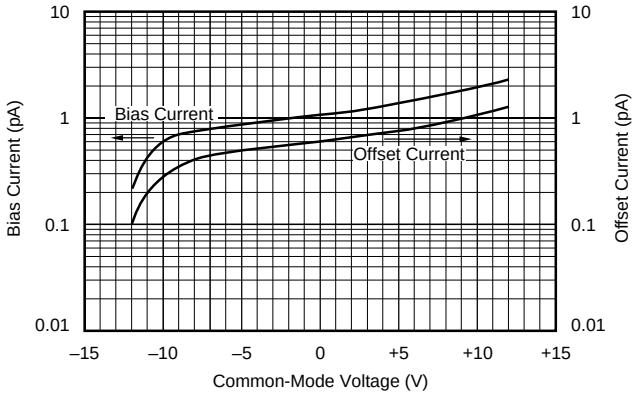

BIAS AND OFFSET CURRENT vs TEMPERATURE



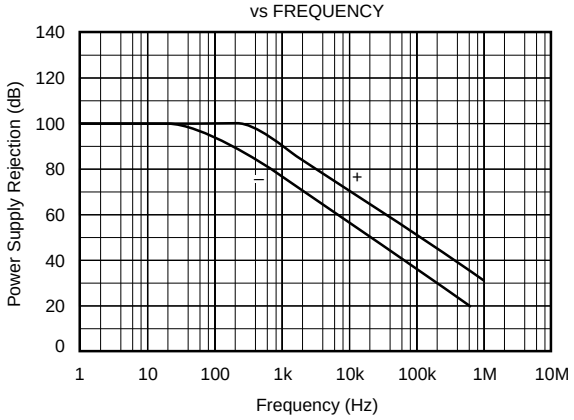
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

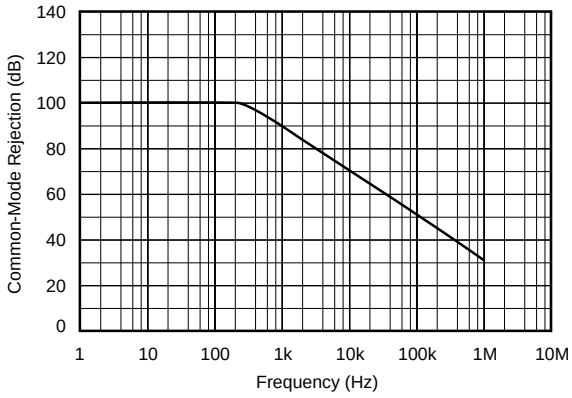
BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



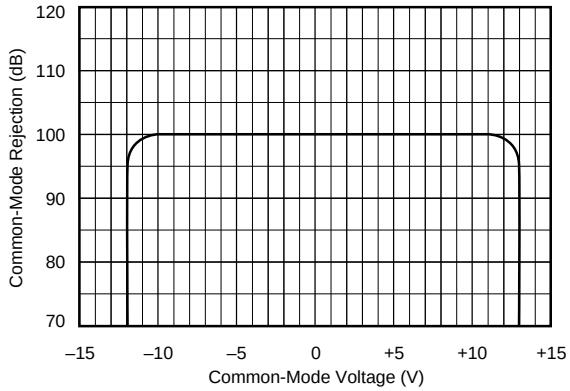

POWER SUPPLY REJECTION
vs FREQUENCY



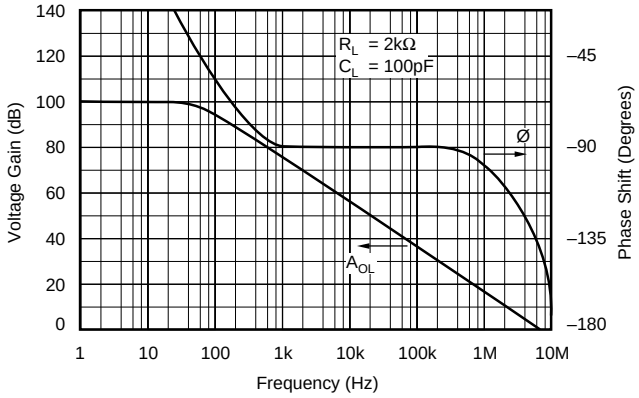

COMMON-MODE REJECTION
vs FREQUENCY



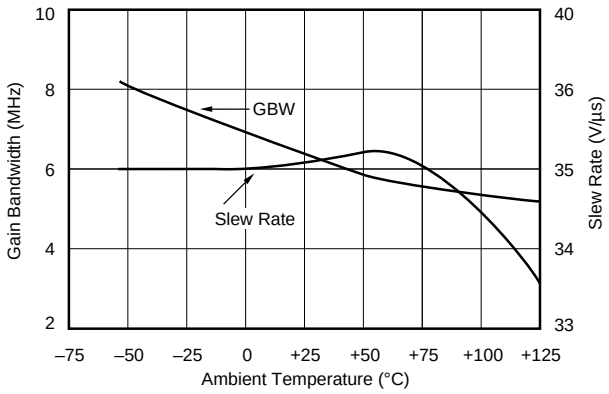

COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE




OPEN-LOOP FREQUENCY RESPONSE



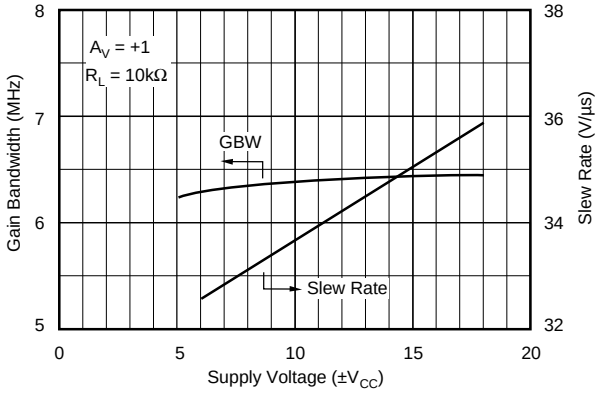

GAIN BANDWIDTH AND SLEW RATE
vs TEMPERATURE



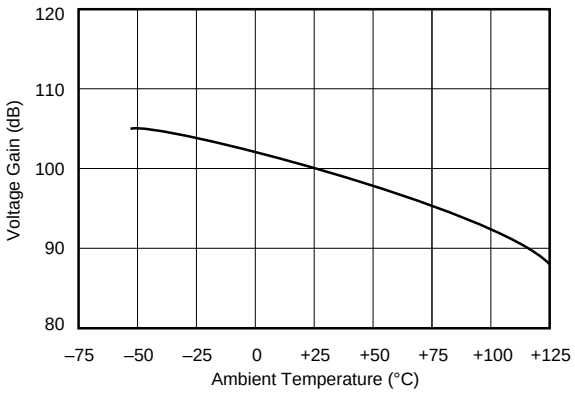
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

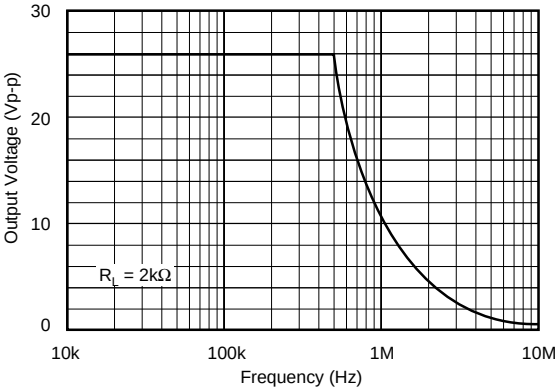
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



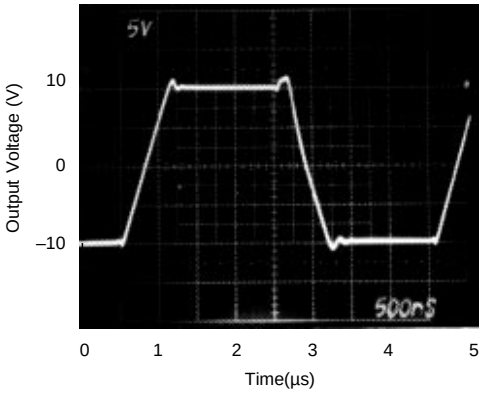

OPEN-LOOP GAIN vs TEMPERATURE



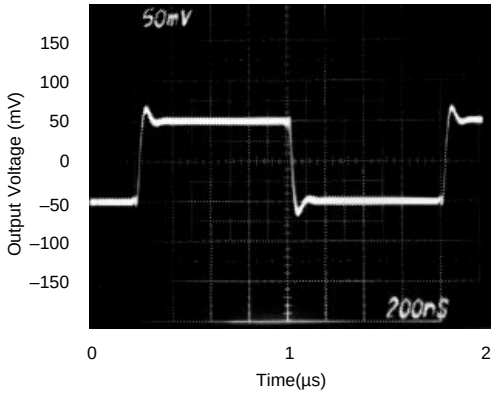

MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



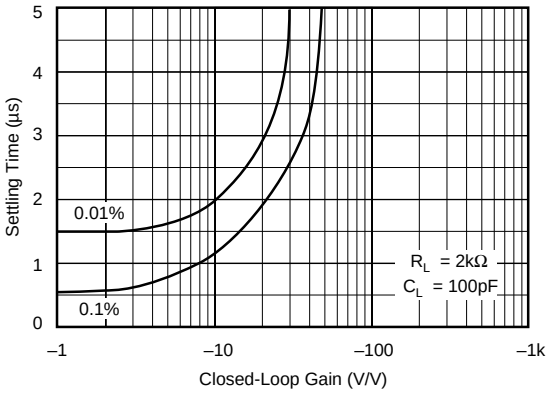

LARGE SIGNAL TRANSIENT RESPONSE




SMALL SIGNAL TRANSIENT RESPONSE



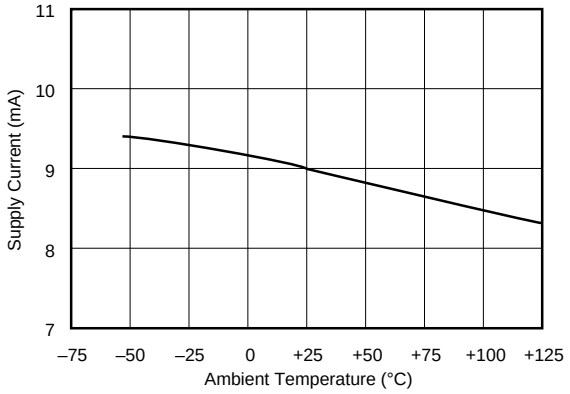

SETTLING TIME vs CLOSED-LOOP GAIN



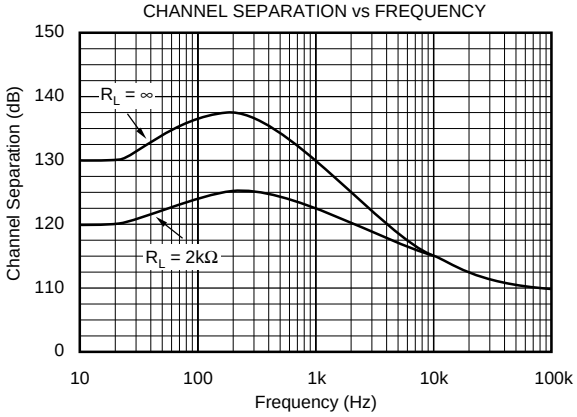
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A$ = +25°C, $V_{CC}$ = ±15VDC unless otherwise noted.

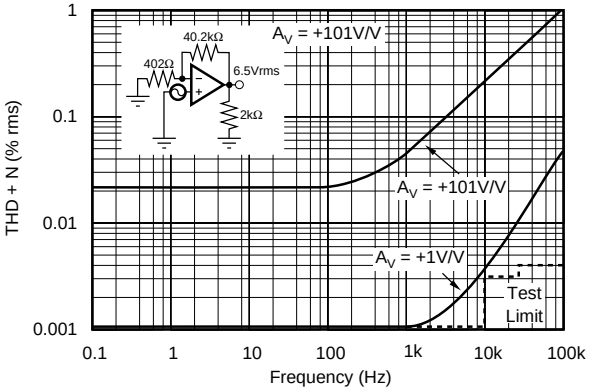
SUPPLY CURRENT vs TEMPERATURE



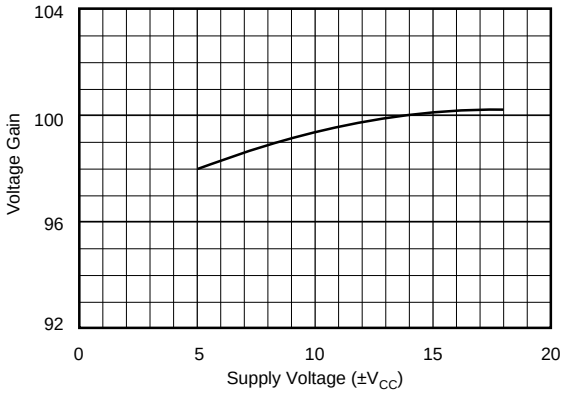

CHANNEL SEPARATION vs FREQUENCY



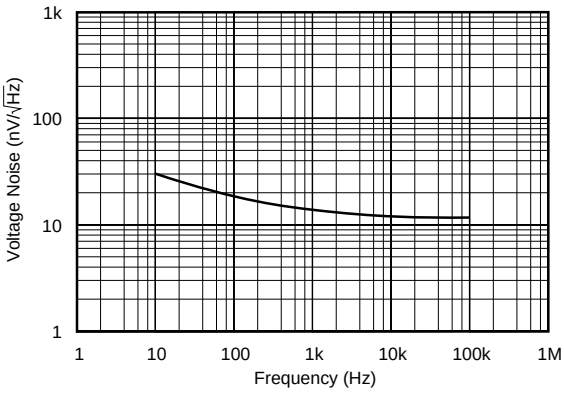

TOTAL HARMONIC DISTORTION vs FREQUENCY




OPEN-LOOP GAIN vs SUPPLY VOLTAGE




INPUT VOLTAGE NOISE SPECTRAL DENSITY



# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

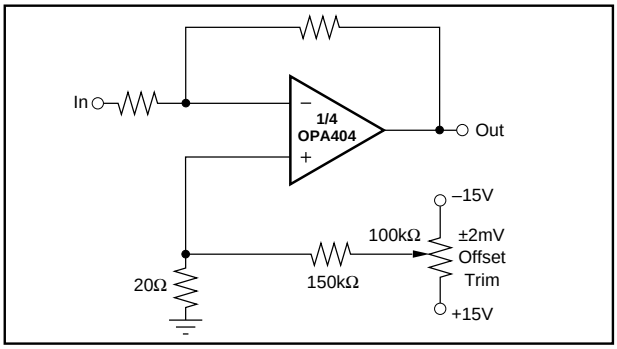



FIGURE 1. Offset Voltage Trim.

## INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA404 requires input current limiting resistors only if its input voltage is greater than 8 volts more negative than $-V_{CC}$. A 10kΩ series resistor will limit the input current to a safe value with up to ±15V input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

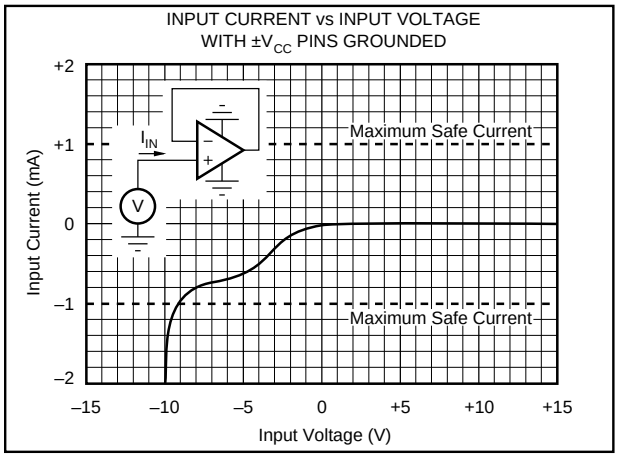



FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

## GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low-impedance point which is at the signal input potential. (See Figure 3).

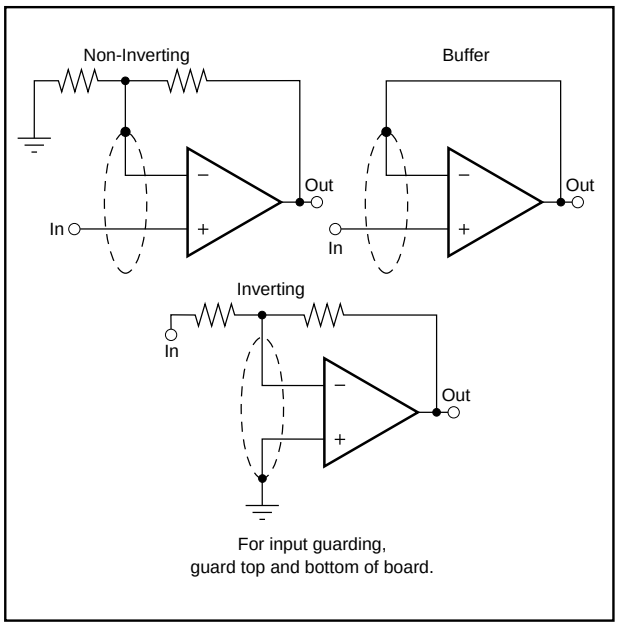



FIGURE 3. Connection of Input Guard.

## HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

## BIAS CURRENT CHANGE vs COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA404 is not compromised by common-mode voltage.

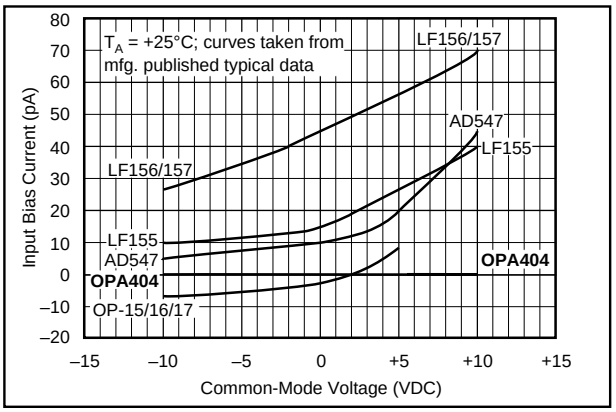



FIGURE 4. Input Bias Current vs Common-Mode Voltage.

## APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

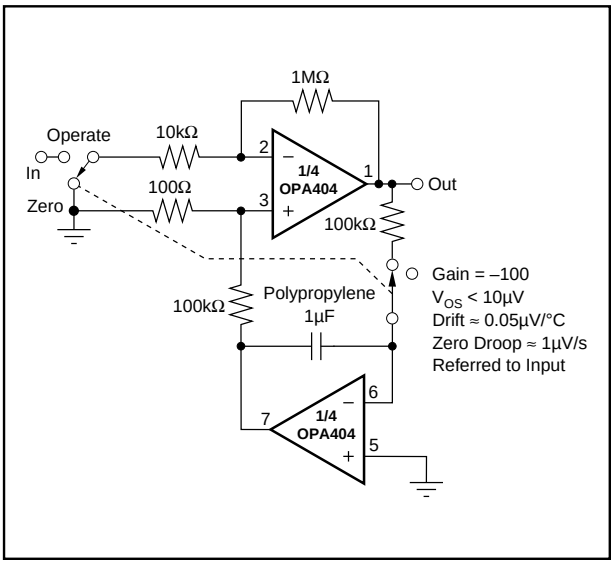



FIGURE 5. Auto-Zero Amplifier.

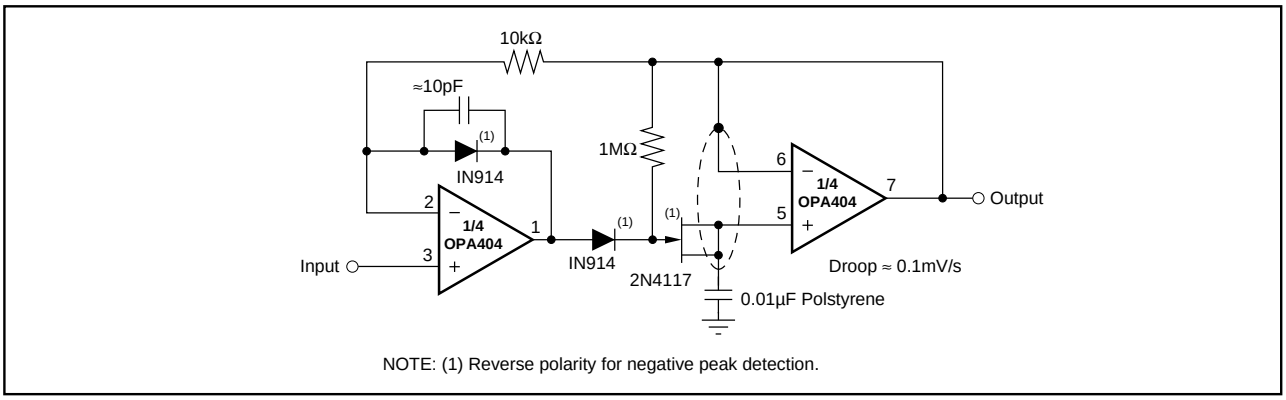



FIGURE 6. Low-Droop Positive Peak Detector.

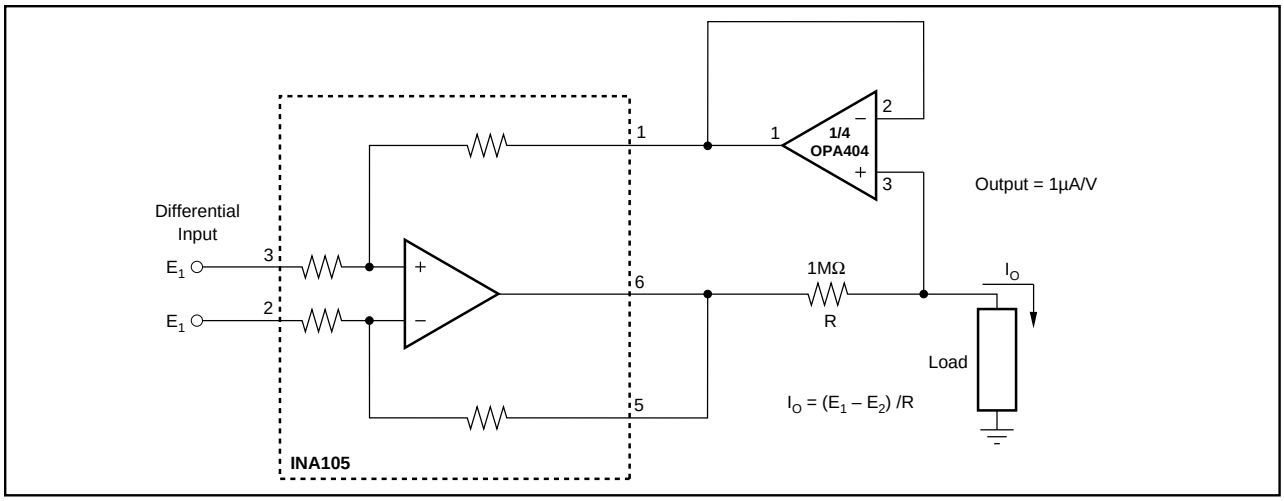



FIGURE 7. Voltage-Controlled Microamp Current Source.

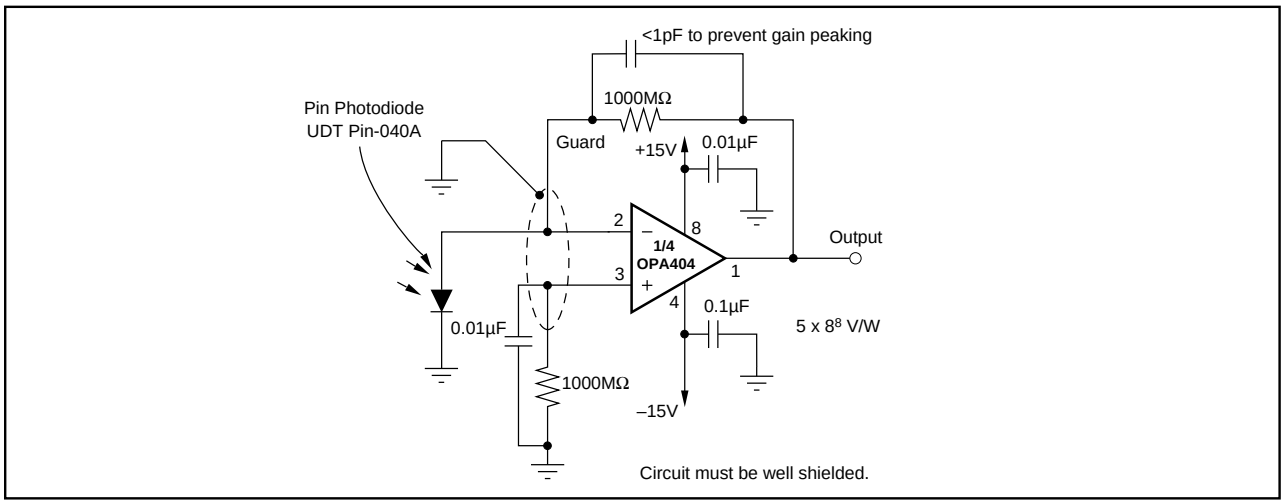



FIGURE 8. Sensitive Photodiode Amplifier.

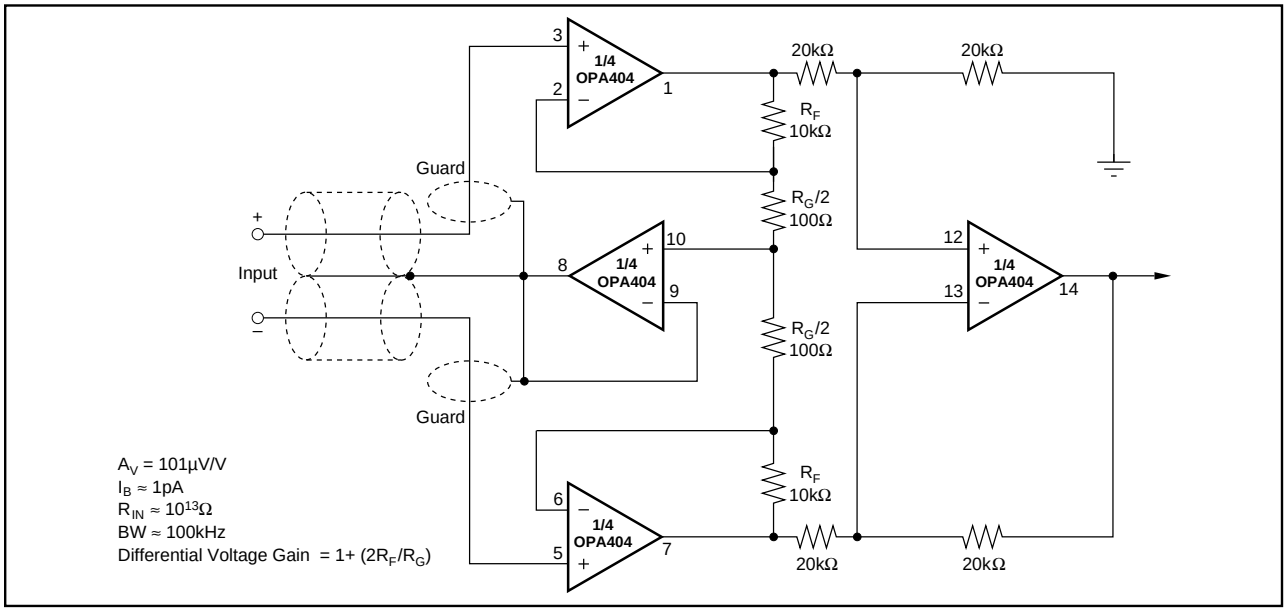



FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

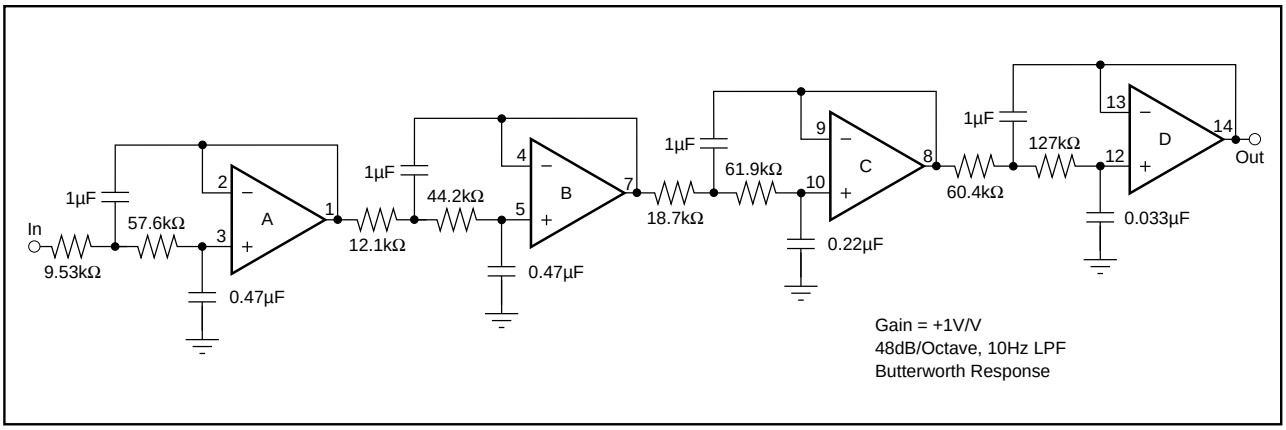



FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

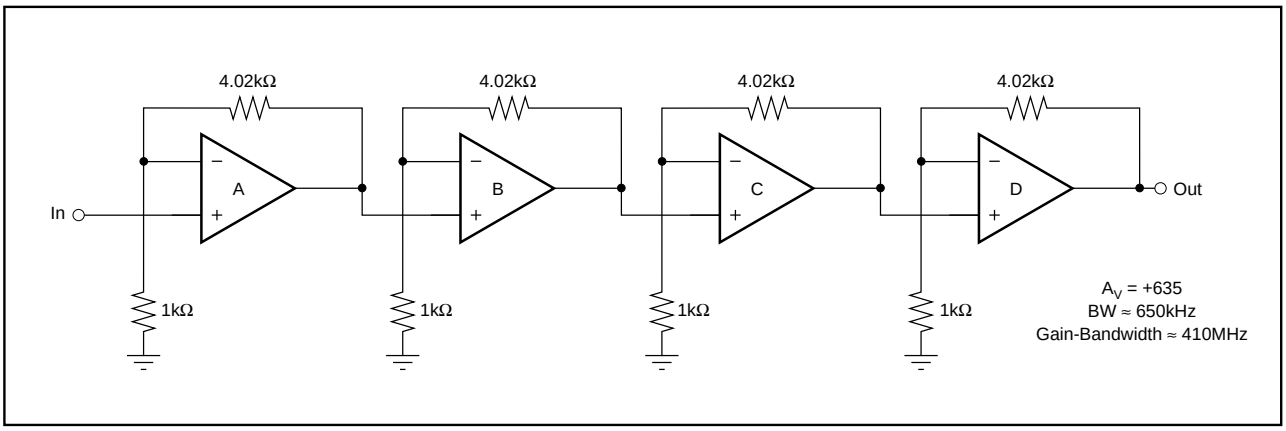



FIGURE 11. Wide-Band Amplifier.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA404AG | NRND | CDIP SB | JD | 14 | 1 | Green (RoHS & no Sb/Br) | AU | N / A for Pkg Type | | OPA404AG | |
| OPA404BG | NRND | CDIP SB | JD | 14 | 1 | Green (RoHS & no Sb/Br) | AU | N / A for Pkg Type | | OPA404BG | |
| OPA404KP | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | | OPA404KP | Samples |
| OPA404KPG4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | | OPA404KP | Samples |
| OPA404KU | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | 0 to 70 | OPA404KU | Samples |
| OPA404KU/1K | ACTIVE | SOIC | DW | 16 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | 0 to 70 | OPA404KU | Samples |
| OPA404SG | NRND | CDIP SB | JD | 14 | 1 | Green (RoHS & no Sb/Br) | AU | N / A for Pkg Type | | OPA404SG | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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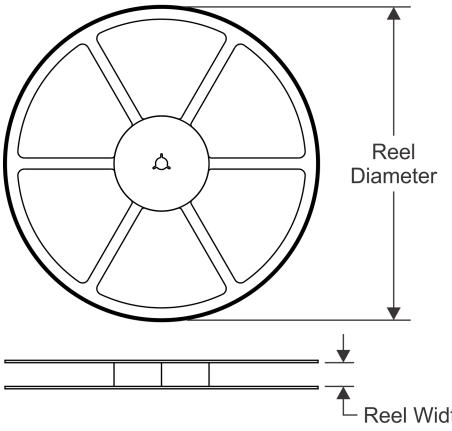
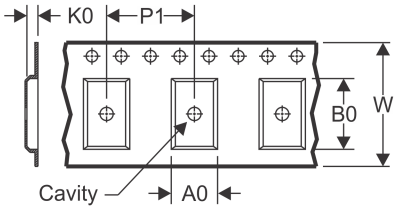
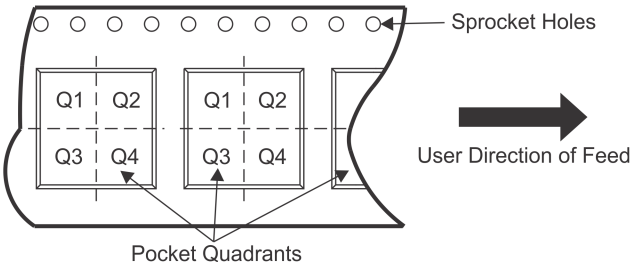



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

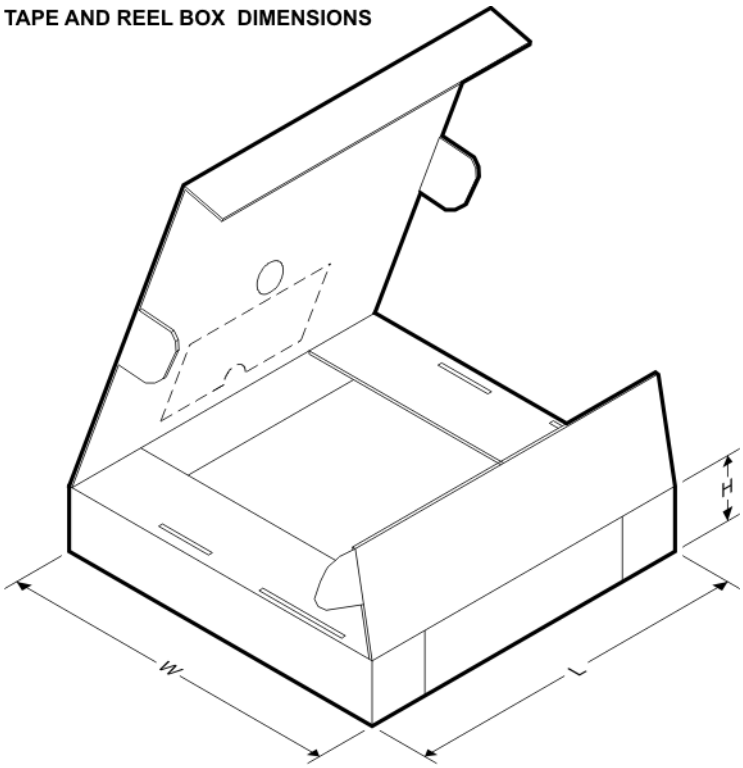
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA404KU/1K | SOIC | DW | 16 | 1000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA404KU/1K | SOIC | DW | 16 | 1000 | 367.0 | 367.0 | 38.0 |

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