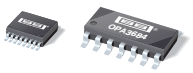
THE DATASHEET OF

OPA3684IDBQT



Low-Power, Triple Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- MINIMAL BANDWIDTH CHANGE VERSUS GAIN
- 170MHz BANDWIDTH: G = +2
- > 120MHz BANDWIDTH TO GAIN > +10
- LOW DISTORTION: < –82dBc at 5MHz
- HIGH OUTPUT CURRENT: 120mA
- SINGLE +5V TO +12V SUPPLY OPERATION
- DUAL ±2.5V TO ±6.0V SUPPLY OPERATION
- LOW SUPPLY CURRENT: 1.7mA/ch
- LOW SHUTDOWN CURRENT: 100µA/ch

APPLICATIONS

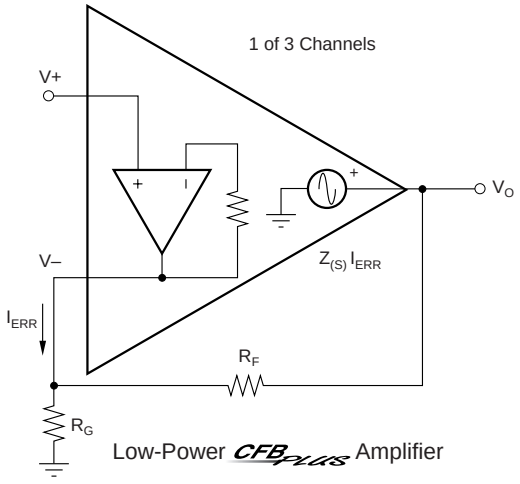
- RGB LINE DRIVERS
- LOW-POWER BROADCAST VIDEO DRIVERS
- EQUALIZING FILTERS
- MULTICHANNEL SUMMING AMPLIFIERS
- PROFESSIONAL CAMERAS
- ADC INPUT DRIVERS

DESCRIPTION

The OPA3684 provides a new level of performance in low-power, wideband, current-feedback (CFB) amplifiers. This CFB_{PLUS} amplifier among the first to use an internally closed-loop input buffer stage that enhances performance significantly over earlier low-power CFB amplifiers. While retaining the benefits of very low power operation, this new architecture provides many of the benefits of a more ideal CFB amplifier. The closed-loop input stage buffer gives a very low and linearized impedance path at the inverting input to sense the feedback error current. This improved inverting input impedance retains exceptional bandwidth to much higher gains and improves harmonic distortion over earlier solutions limited by inverting input linearity. Beyond simple high-gain applications, the OPA3684 CFB_{PLUS} amplifier permits the gain setting element to be set with considerable freedom from amplifier bandwidth interaction. This allows frequency response peaking elements to be added, multiple input inverting summing circuits to have greater bandwidth, and low-power line drivers to meet the demanding requirements of studio cameras and broadcast video.

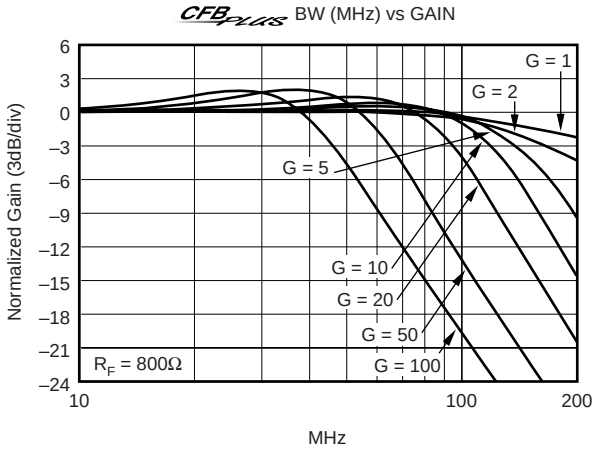
The output capability of the OPA3684 also sets a new mark in performance for low-power current-feedback amplifiers. Delivering a full ±4Vp-p swing on ±5V supplies, the OPA3684 also has the output current to support > ±3Vp-p into 50Ω. This minimal output headroom requirement is complemented by a similar 1.2V input stage headroom giving exceptional capability for single +5V operation.

The OPA3684's low 1.7mA/ch supply current is precisely trimmed at 25°C. This trim, along with low shift over temperature and supply voltage, gives a very robust design over a wide range of operating conditions. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA3684 supply current drops to less than 100µA/ch while the I/O pins go to a high impedance state.



Low-Power CFB_{PLUS} Amplifier

Patent Pending



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5 V_{DC}$
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: ID, IDBQ	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C
ESD Rating: HBM	1900V
CDM	1500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

OPA3684 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA684	OPA2684	—	OPA4684	Low-Power CFB_{plus}
OPA691	OPA2691	OPA3691	—	High Slew Rate CFB
OPA685	—	—	—	> 500MHz CFB
OPA692	—	OPA3692	—	Fixed-Gain Video Buffers

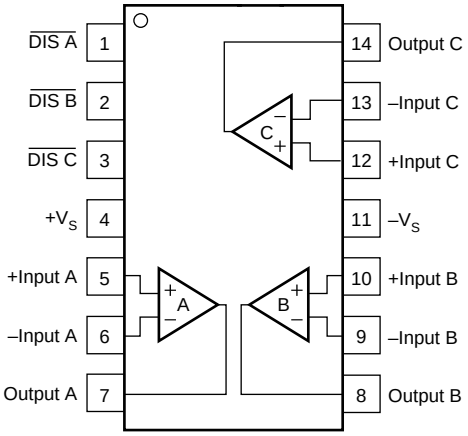
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3684	SO-14	D	–40°C to +85°C	OPA3684	OPA3684ID	Rails, 58
"	"	"	"	"	OPA3684IDR	Tape and Reel, 2500
OPA3684	SSOP-16	DBQ	–40°C to +85°C	OPA3684	OPA3684IDBQT	Tape and Reel, 250
"	"	"	"	"	OPA3684IDBQR	Tape and Reel, 2500

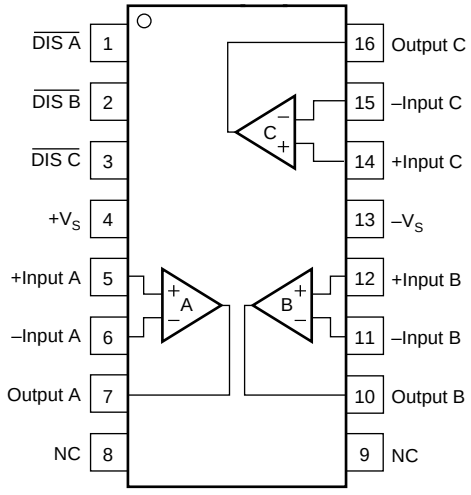
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **SO**



Top View **SSOP**



ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 800\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3684ID, IDBQ						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 800Ω	250				MHz	typ	C
	G = +2, R_F = 800Ω	170	120	118	117	MHz	min	B
	G = +5, R_F = 800Ω	138				MHz	typ	C
	G = +10, R_F = 800Ω	120				MHz	typ	C
	G = +20, R_F = 800Ω	95				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O = 0.5V_{PP}, R_F = 800Ω	19	16	14	14	MHz	min	B
Peaking at a Gain of +1	R_F = 800Ω, V_O = 0.5V_{PP}	1.4	4.8	5.9	6.3	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 4V_{PP}	90				MHz	typ	C
Slew Rate	G = –1, V_O = 4V Step	780	675	650	575	V/µs	min	B
	G = +2,V_O = 4V Step	750	680	660	650	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	3				ns	typ	C
	G = +2, V_O = 4VStep	6.8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–67	–59	–59	–58	dBc	max	B
	R_L ≥ 1kΩ	–82	–66	–65	–65	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–70	–66	–65	–65	dBc	max	B
	R_L ≥ 1kΩ	–84	–82	–81	–81	dBc	max	B
Input Voltage Noise	f > 1MHz	3.7	4.1	4.2	4.4	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	9.4	11	12	12.5	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	17	18	18.5	19	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.04				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.02				deg	typ	C
All Hostile Crosstalk	2 Channels, f = 5MHz 3rd-Channel Measured	70				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, R_L = 1kΩ	355	**160**	155	153	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.5	**±3.9**	±4.5	±4.7	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±5.0	**±12**	±13.5	±14	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			±25	±30	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5.0	**±17**	±18.5	±19.5	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±35	±40	nA°/C	max	B
INPUT								
Common-Mode Input Range(5) (CMIR)		±3.75	**±3.65**	±3.65	±3.6	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	60	**53**	52	52	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop, DC	4.0				Ω	typ	C
OUTPUT								
Voltage Output Swing	1kΩ Load	±4.1	**±3.9**	±3.9	±3.8	V	min	A
Current Output, Sourcing	V_O = 0	160	**120**	115	110	mA	min	A
Current Output, Sinking	V_O = 0	–120	**–100**	–95	–90	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.006				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0 (all channels)	–300	**–500**	–580	–600	µA	max	A
Disable Time	V_{IN} = +1V, G = +2	4				ms	typ	C
Enable Time	V_{IN} = +1V, G = +2	40				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Enable Voltage		3.4	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V/Channel	80	**120**	130	135	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Minimum Operating Voltage Range		±1.4				V	min	C
Max Quiescent Current	V_S = ±5V/per Channel	1.7	**1.8**	1.85	1.85	mA	max	A
Min Quiescent Current	V_S = ±5V/per Channel	1.7	**1.6**	1.55	1.45	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	60	**54**	53	53	dB	typ	A
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-14		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications. (2) Junction temperature = ambient at low temperature limit, junction temperature = ambient +2°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 1.0kΩ, R_L = 100Ω, and G = +2, unless otherwise noted.

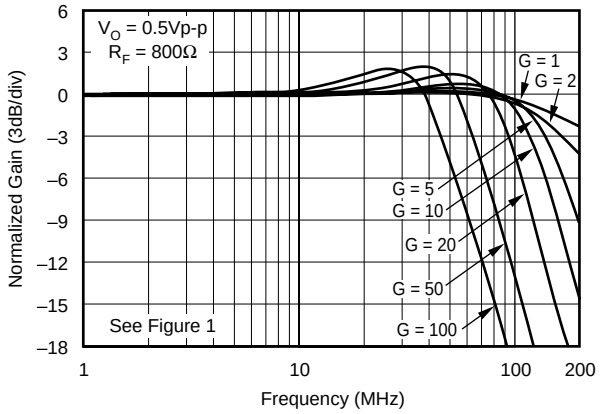
PARAMETER	CONDITIONS	OPA3684ID, IDBQ						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 1.0kΩ	140				MHz	typ	C
	G = +2, R_F = 1.0kΩ	110	86	85	82	MHz	min	B
	G = +5, R_F = 1.0kΩ	100				MHz	min	C
	G = +10, R_F = 1.0kΩ	90				MHz	typ	C
	G = +20, R_F = 1.0kΩ	75				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}, R_F = 1.0kΩ	21	12	11	10	MHz	min	B
Peaking at a Gain of +1	R_F = 1.0kΩ, V_O < 0.5V_{PP}	0.5	2.6	3.4	3.7	dB	max	B
Large-Signal Bandwidth	G = 2, V_O = 2V_{PP}	86				MHz	typ	C
Slew Rate	G = 2, V_O = 2V Step	380	300	290	285	V/µs	min	B
Rise-and-Fall Time	G = 2, V_O = 0.5V Step	4.3				ns	typ	C
	G = 2, V_O = 2VStep	4.8				ns	typ	C
Harmonic Distortion	G = 2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–65	–60	–59	–59	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–84	–62	–61	–61	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–65	–64	–63	–63	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–74	–70	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	3.7	4.1	4.2	4.4	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	9.4	11	12	12.5	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	17	18	18.5	19	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.04				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.07				deg	typ	C
All Hostile Crosstalk	2 Channels, f = 5MHz 3rd-Channel Measured	70				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	355	**160**	155	153	kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	±1.0	**±3.4**	±4.0	±4.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	±5	**±12**	±13.5	±14	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±25	±30	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	±5	**±13**	±14.5	±16	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±25	±30	nA°/C	max	B
INPUT								
Least Positive Input Voltage(5)		1.25	**1.32**	1.35	1.38	V	max	A
Most Positive Input Voltage(5)		3.75	**3.68**	3.65	3.62	V	min	A
Common-Mode Refection Ratio (CMRR)	V_{CM} = V_S/2	58	**51**	50	50	dB	min	A
Noninverting Input Impedance		50 || 1				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	4.5				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	R_L = 1kΩ to V_S/2	4.10	**3.9**	3.9	3.8	V	min	A
Least Positive Output Voltage	R_L = 1kΩ to V_S/2	0.9	**1.1**	1.1	1.2	V	max	A
Current Output, Sourcing	V_O = V_S/2	80	**65**	60	55	mA	min	A
Current Output, Sinking	V_O = V_S/2	70	**55**	50	45	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz					Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0 (all channels)	–300				µA	typ	C
Off Isolation	F = 5.0MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2					mV	typ	C
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2					mV	typ	C
Enable Voltage		3.4	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V/Channel	80	**120**	130	135	µA	max	A
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Max Single-Supply Operating Voltage Range			**12**	12	12	V	max	A
Min Single-Supply Operating Voltage Range		2.8				V	min	C
Max Quiescent Current	V_S = +5V/per Channel	1.44	**1.55**	1.55	1.55	mA	max	A
Min Quiescent Current	V_S = +5V/per Channel	1.44	**1.30**	1.20	1.15	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	65				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA} Junction-to-Ambient								
D SO-14		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications. (2) Junction temperature = ambient at low temperature limit, junction temperature = ambient +1°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

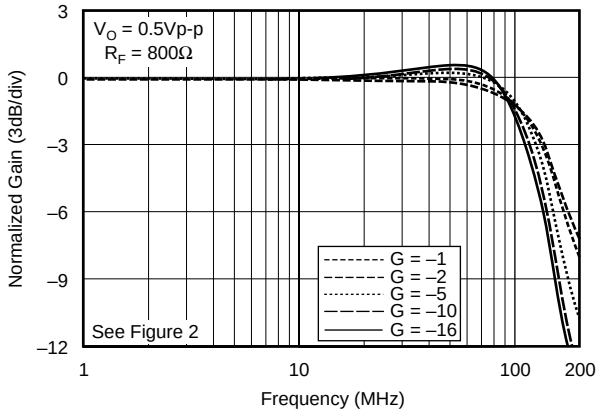
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

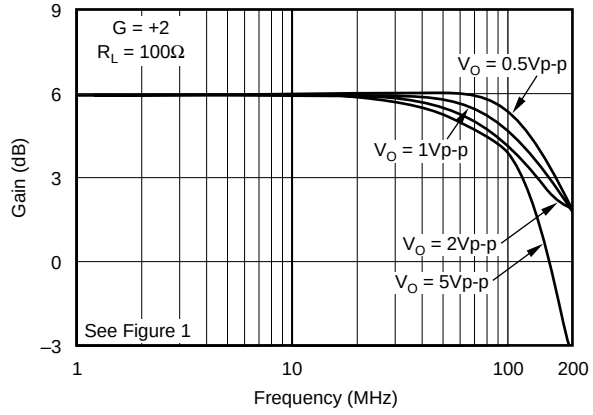
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



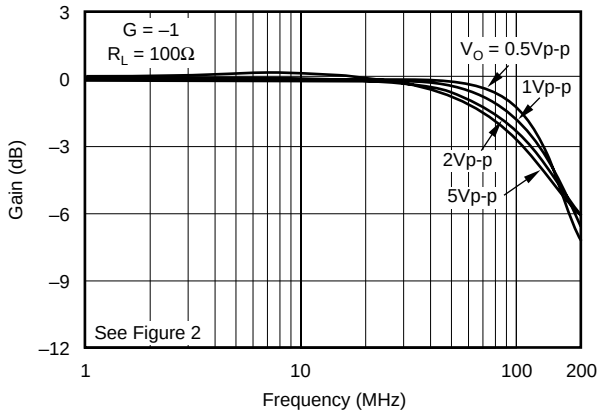
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



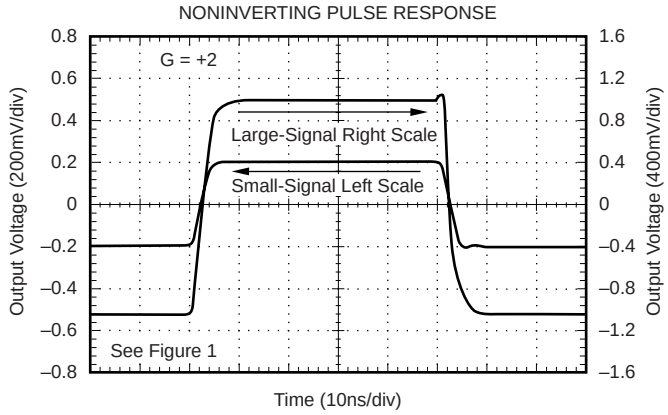
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



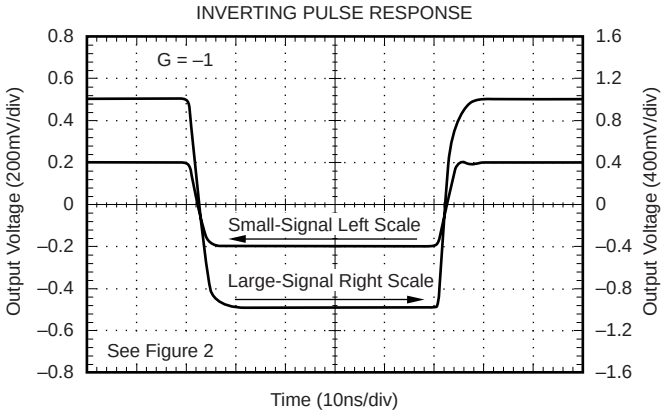
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



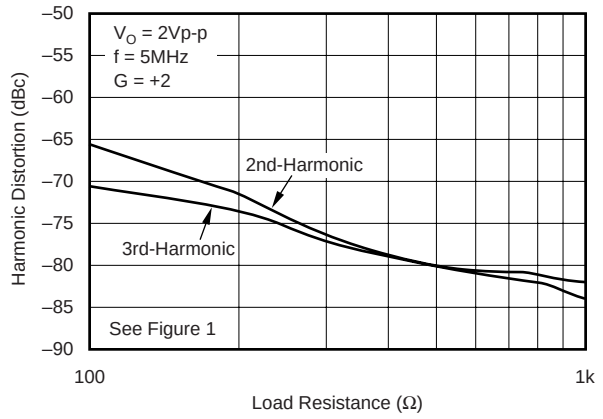
INVERTING PULSE RESPONSE



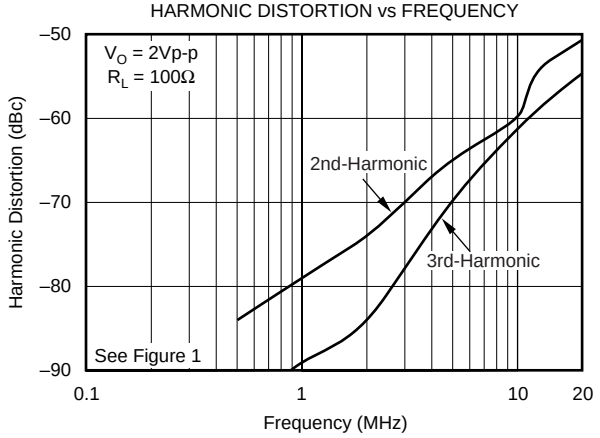
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

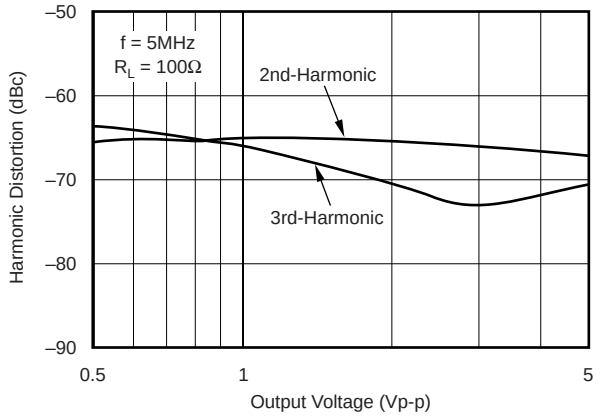
HARMONIC DISTORTION vs LOAD RESISTANCE



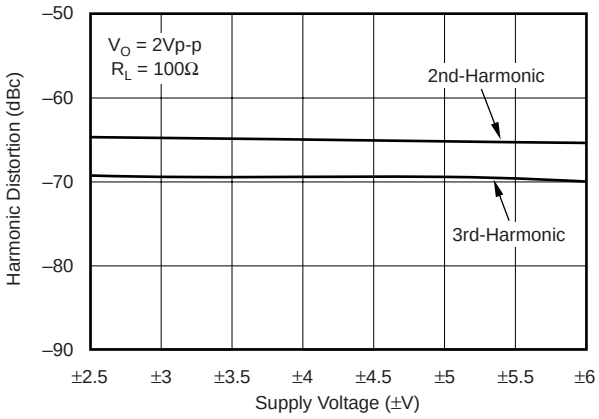
HARMONIC DISTORTION vs FREQUENCY



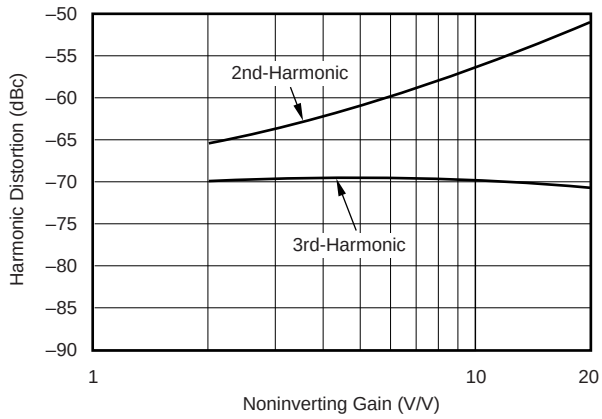
HARMONIC DISTORTION vs OUTPUT VOLTAGE



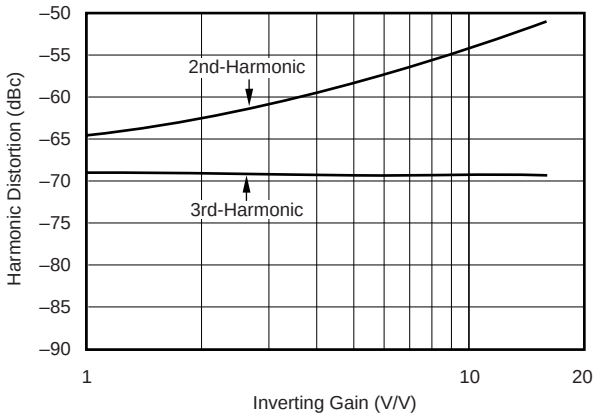
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



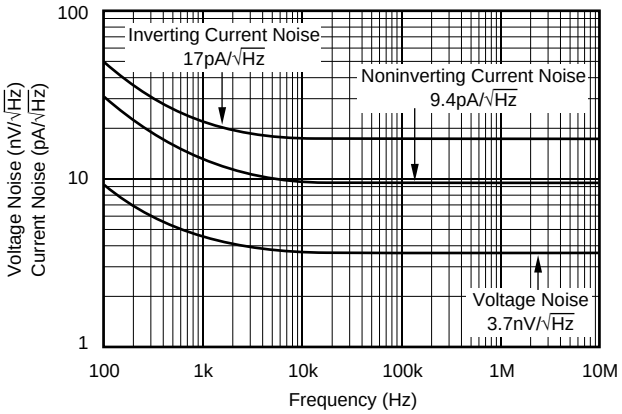
HARMONIC DISTORTION vs INVERTING GAIN



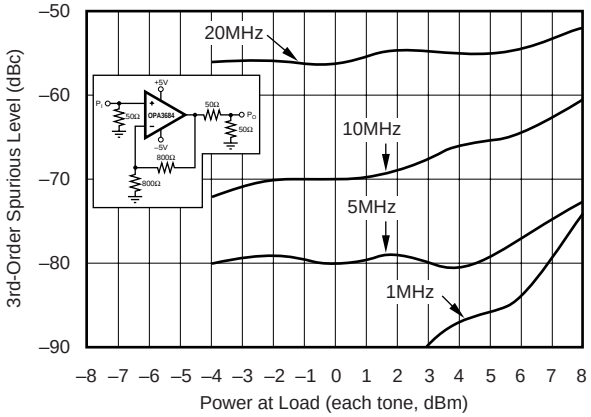
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

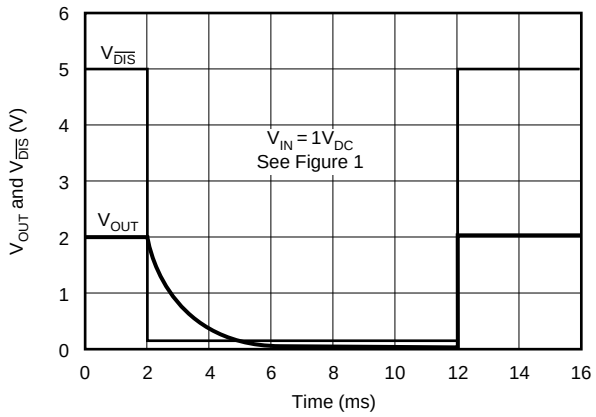
INPUT VOLTAGE AND CURRENT NOISE DENSITY



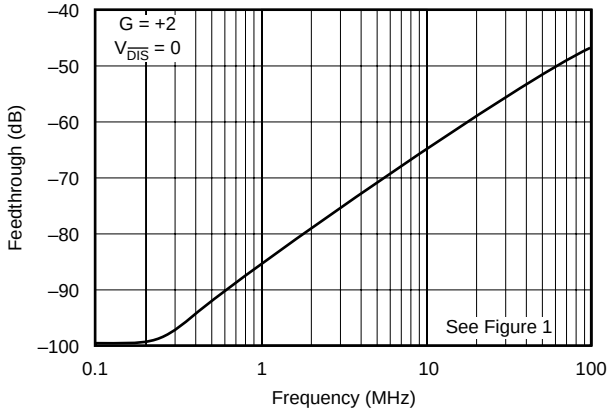
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



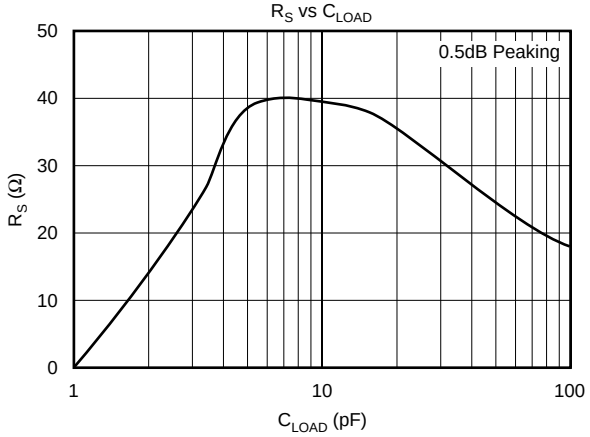
DISABLE TIME



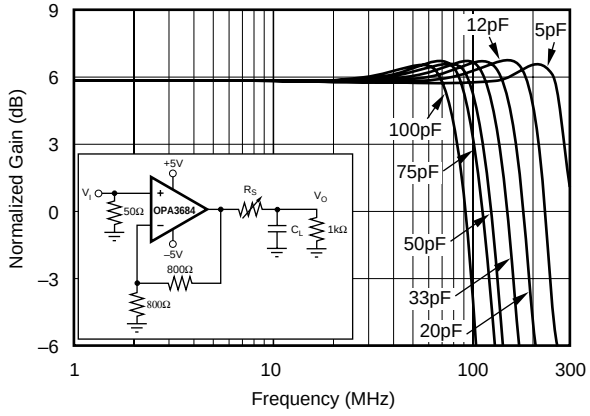
DISABLED FEEDTHROUGH



R_S vs C_{LOAD}



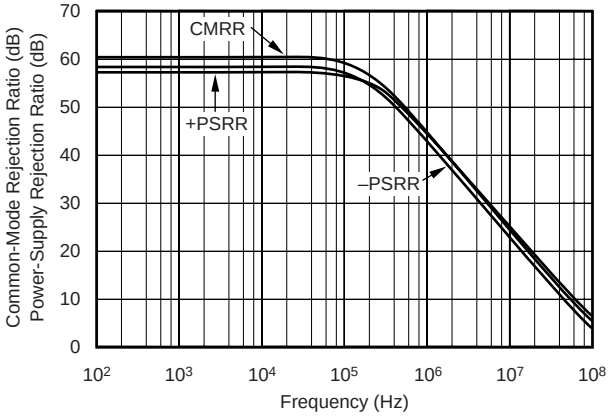
SMALL-SIGNAL BANDWIDTH vs C_{LOAD}



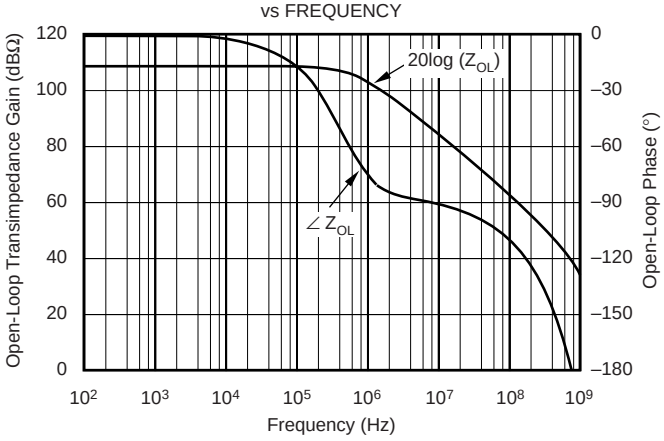
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

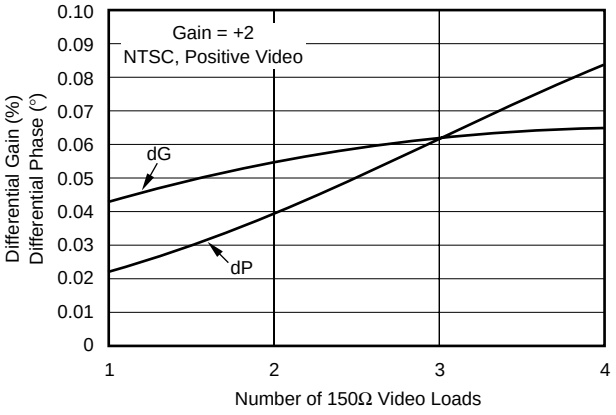
CMRR and PSRR vs FREQUENCY



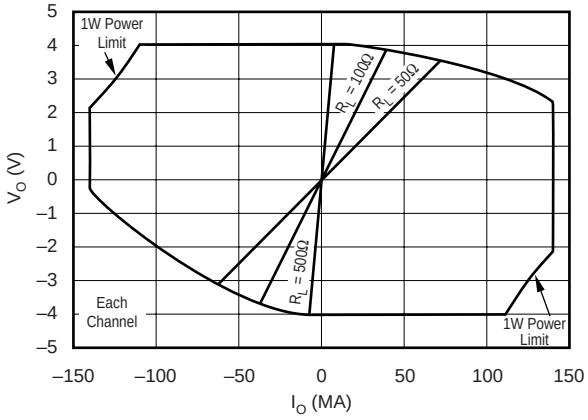
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE vs FREQUENCY



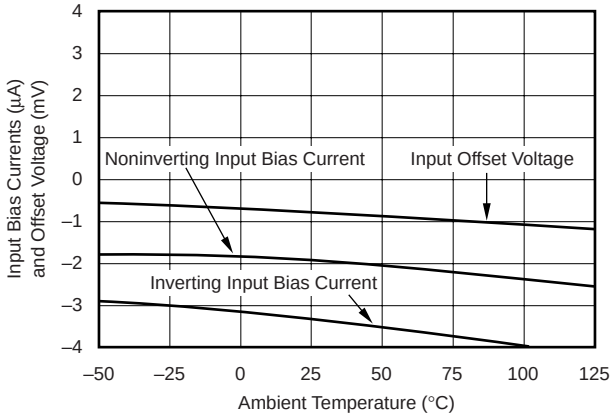
COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



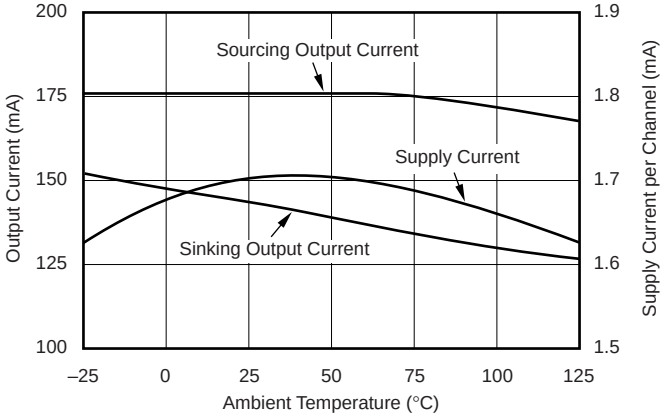
OUTPUT CURRENT AND VOLTAGE LIMITATIONS



TYPICAL DC DRIFT OVER AMBIENT TEMPERATURE



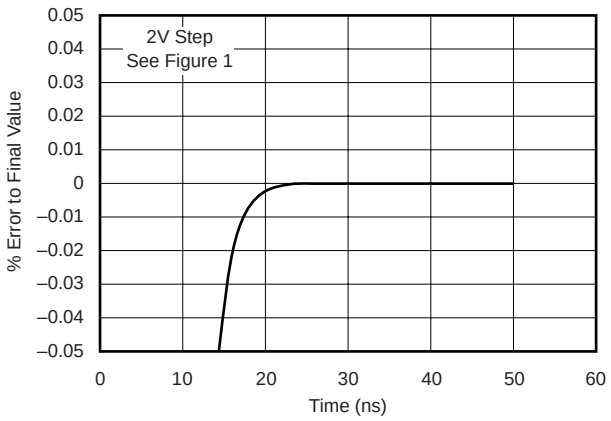
SUPPLY AND OUTPUT CURRENT vs AMBIENT TEMPERATURE



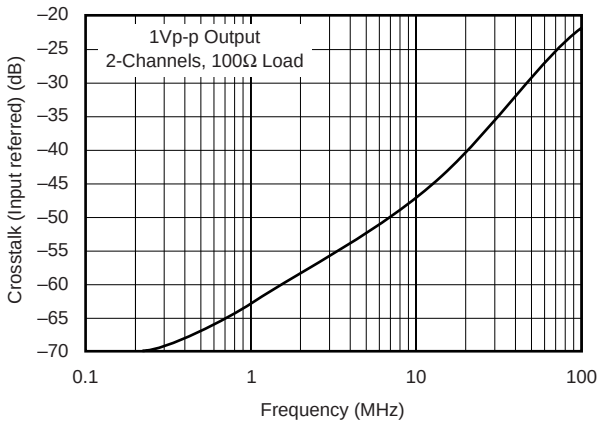
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 800Ω, and R_L = 100Ω, unless otherwise noted.

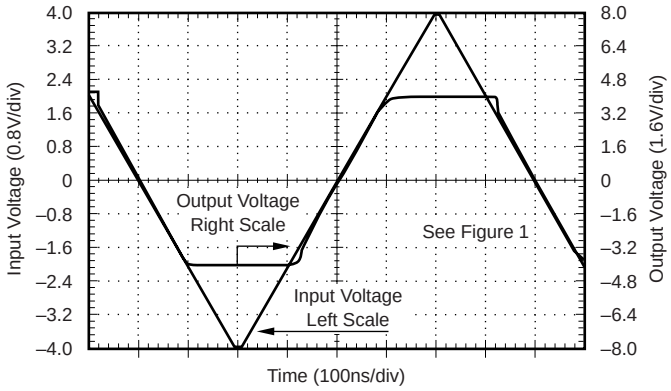
SETTLING TIME



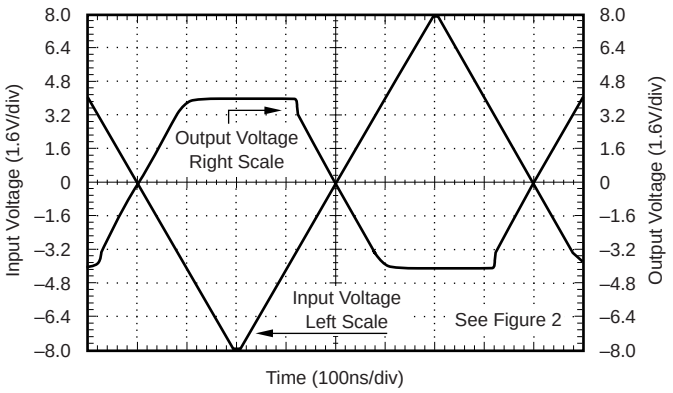
ALL HOSTILE CROSSTALK



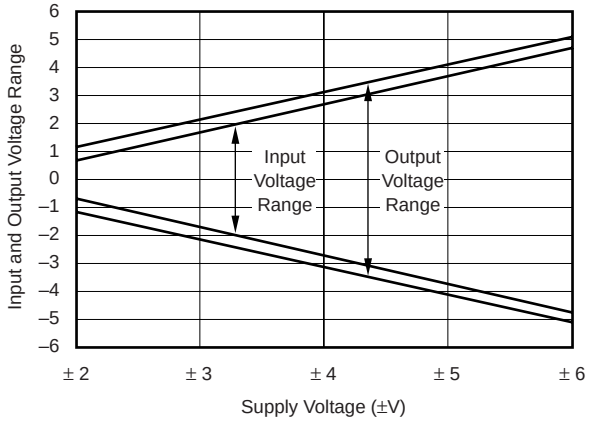
NONINVERTING OVERDRIVE RECOVERY



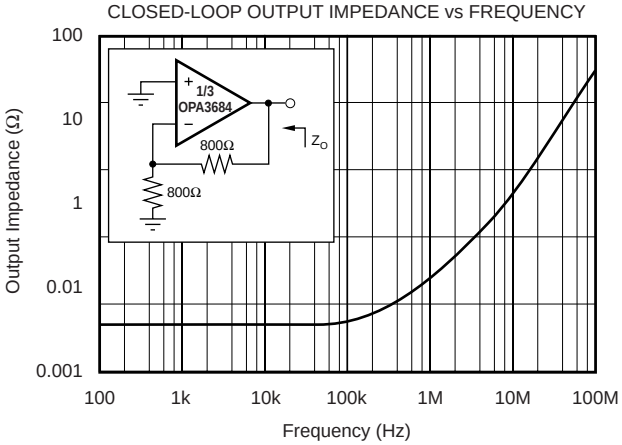
INVERTING OVERDRIVE RECOVERY



INPUT AND OUTPUT VOLTAGE RANGE
vs SUPPLY VOLTAGE



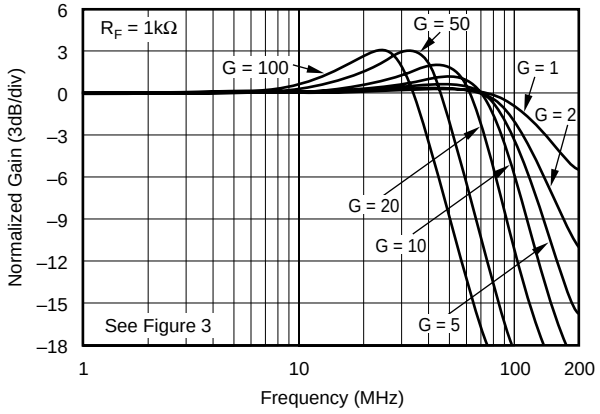
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



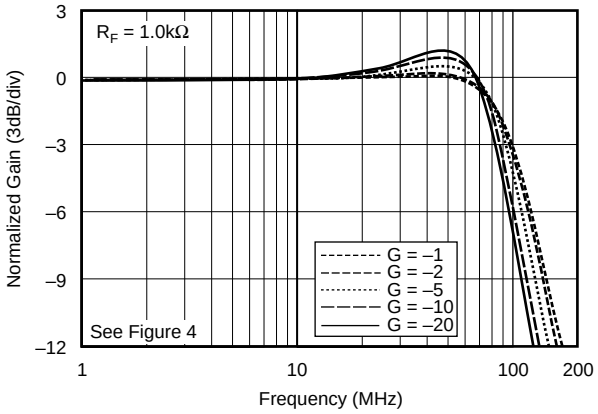
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2, R_F = 1kΩ, and R_L = 100Ω, unless otherwise noted.

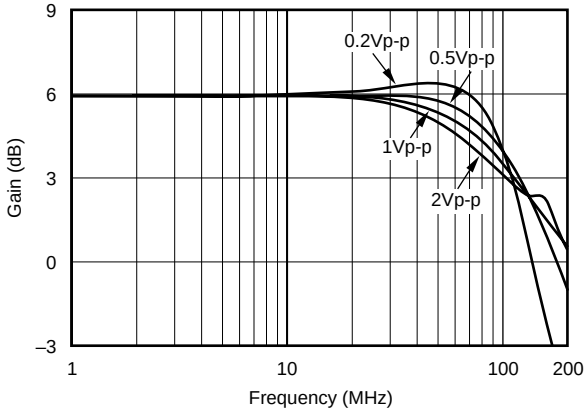
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



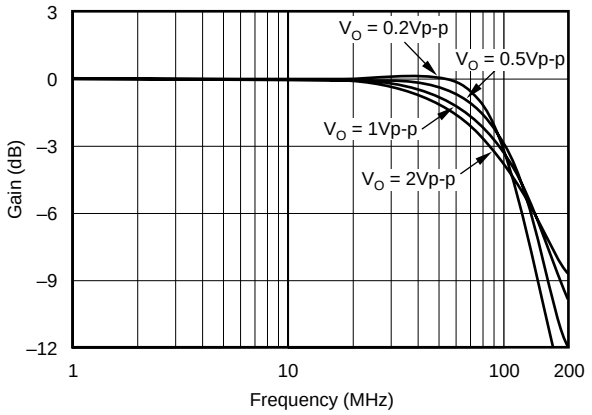
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



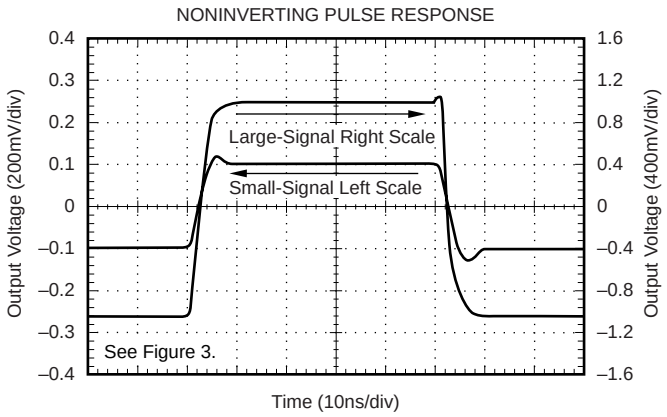
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



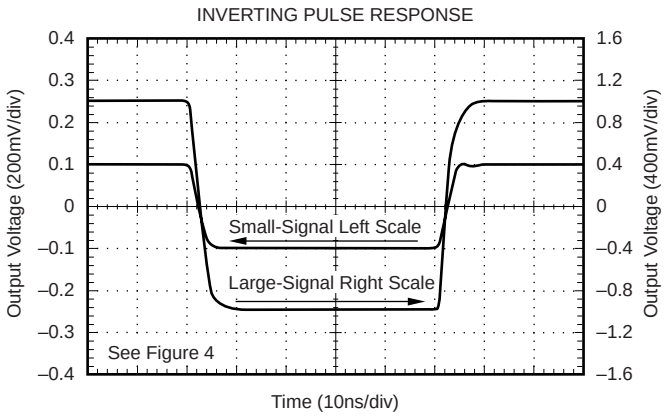
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



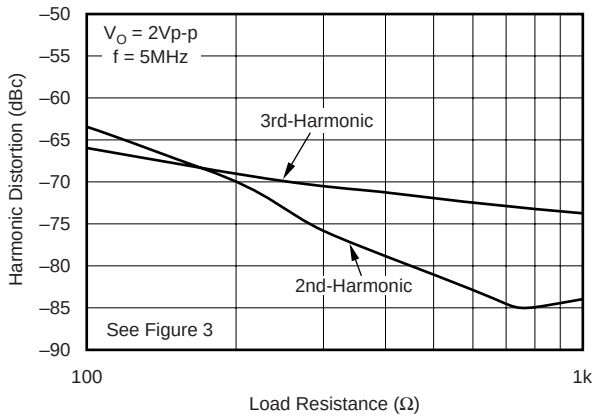
INVERTING PULSE RESPONSE



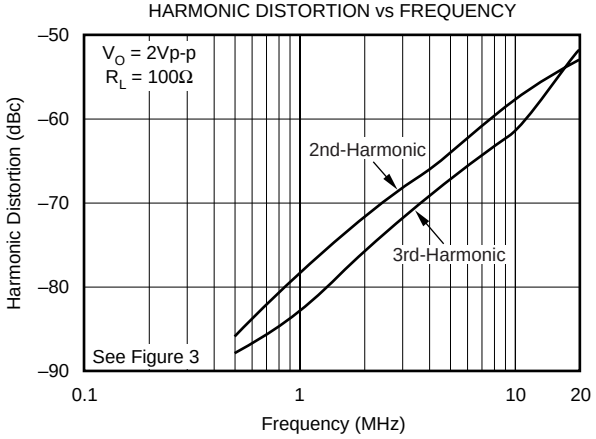
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

At T_A = +25°C, G = +2, R_F = 1kΩ, and R_L = 100Ω, unless otherwise noted.

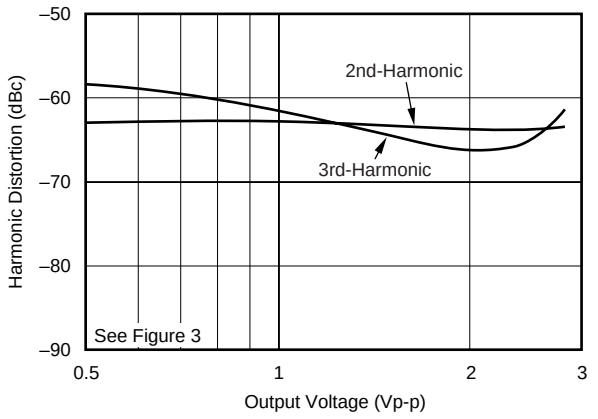
HARMONIC DISTORTION vs LOAD RESISTANCE



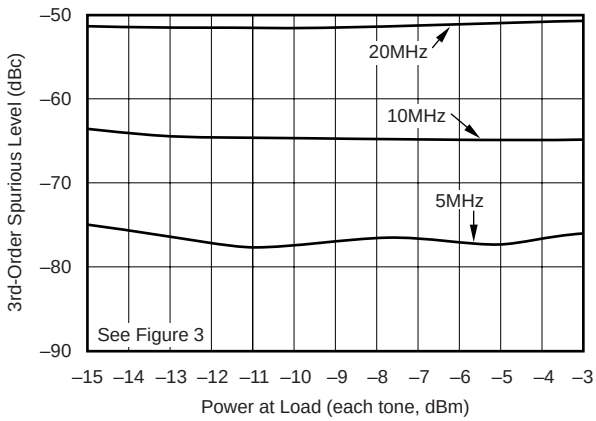
HARMONIC DISTORTION vs FREQUENCY



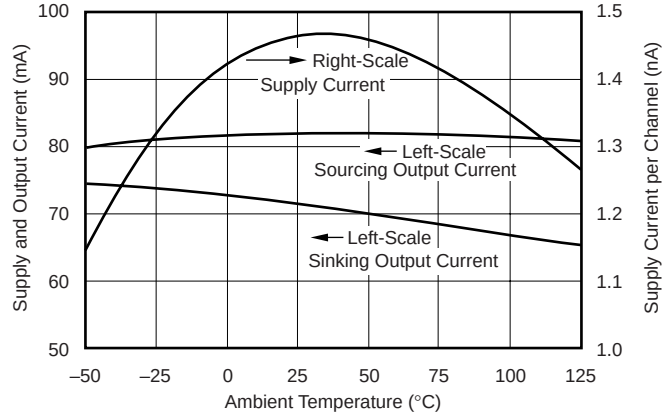
HARMONIC DISTORTION vs OUTPUT VOLTAGE



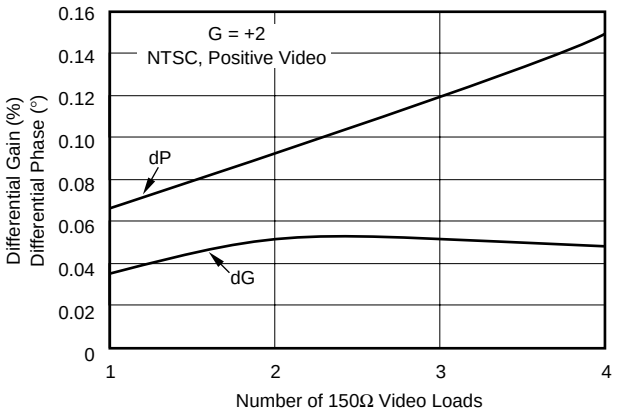
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



SUPPLY AND OUTPUT CURRENT
vs AMBIENT TEMPERATURE



COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



APPLICATIONS INFORMATION

LOW-POWER, CURRENT-FEEDBACK OPERATION

The triple-channel OPA3684 gives a new level of performance in low-power, current-feedback op amps. Using a new input stage buffer architecture, the OPA3684 CFB_{PLUS} amplifier holds nearly constant AC performance over a wide gain range. This closed-loop internal buffer gives a very low and linearized impedance at the inverting node, isolating the amplifier's AC performance from gain element variations. This allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current-feedback performance of gain bandwidth independence. This low-power amplifier also delivers exceptional output power—it's ±4V swing on ±5V supplies with > 100mA output drive gives excellent performance into standard video loads or doubly-terminated 50Ω cables. Single +5V supply operation is also supported with similar bandwidths but with reduced output power capability. For lower quiescent power in a CFB_{PLUS} amplifier, consider the OPA683 family; while for higher output power, consider the OPA691 family.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit used as the basis of the ±5V Electrical and Typical Characteristics for each channel. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 1600Ω = 94Ω. Gain changes are most easily accomplished by simply resetting the R_G value, holding R_F constant at its recommended value of 800Ω.

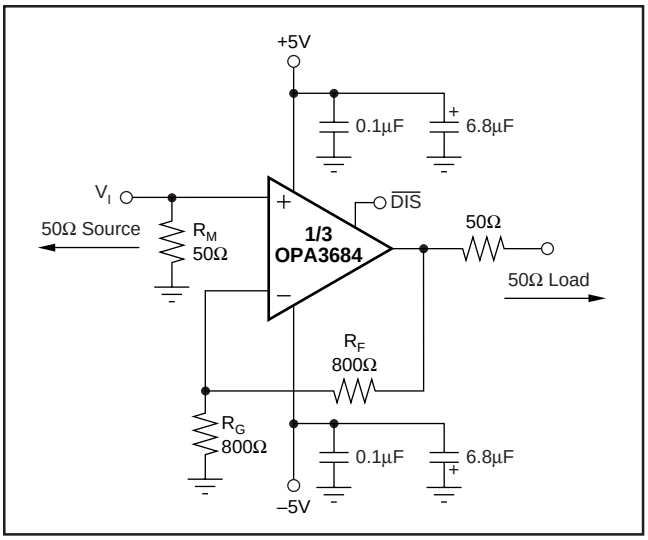


FIGURE 1. DC-Coupled, G = +2V/V, Bipolar Supply Specifications and Test Circuit.

Figure 2 shows the DC-coupled, gain of –1V/V, dual power-supply circuit used as the basis of the Inverting Typical Characteristics for each channel. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is typically higher and the distortion performance is slightly improved. An additional input resistor, R_M, is included in Figure 2 to set the input impedance equal to 50Ω. The parallel combination of R_M and R_G set the input impedance. As the desired gain increases for the inverting configuration, R_G is adjusted to achieved the desired gain, while R_M is also adjusted to hold a 50Ω input match. A point will be reached where R_G will equal 50Ω, R_M is removed, and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, increasing R_F will increase the gain. This will, however, quickly reduce the achievable bandwidth as the feedback resistor increases from its recommended value of 800Ω. If the source does not require an input match to 50Ω, either adjust R_M to get the desired load, or remove it and let the R_G resistor alone provide the input load.

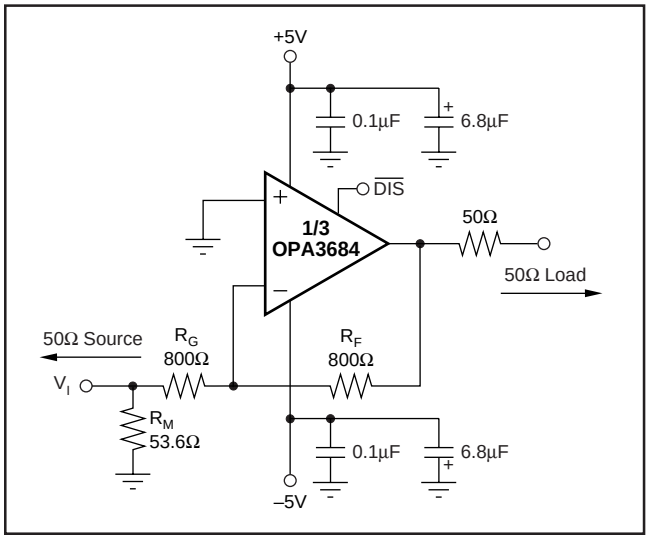


FIGURE 2. DC-Coupled, G = –1V/V, Bipolar Supply Specifications and Test Circuit.

These circuits show ±5V operation. The same circuits can be applied with bipolar supplies from ±2.5V to ±6V. Internal supply independent biasing gives nearly the same performance for the OPA3684 over this wide range of supplies. Generally, the optimum feedback resistor value (for nominally flat frequency response at G = +2) will increase in value as the total supply voltage across the OPA3684 is reduced.

See Figure 3 for the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis for the +5V only Electrical and Typical Characteristics for each channel. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 10kΩ resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.25V of either supply pin, giving a 2.5Vp-p input signal range centered between the supply pins. The input impedance of Figure 3 is set to give a 50Ω input match. If the source does not require a 50Ω match, remove this and drive

directly into the blocking capacitor. The source will then see the 5kΩ load of the biasing network as a load. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the noninverting input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar ±5V supply condition to re-optimize for a flat frequency response in +5V only, gain of +2, operation. On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 70mA output current—easily giving a 3Vp-p output swing into 100Ω (8dBm maximum at the matched 50Ω load). The circuit of Figure 3 shows a blocking capacitor driving into a 50Ω output resistor, then into a 50Ω load. Alternatively, the blocking capacitor could be removed if the load is tied to a supply midpoint or to ground if the DC current then required by the load is acceptable.

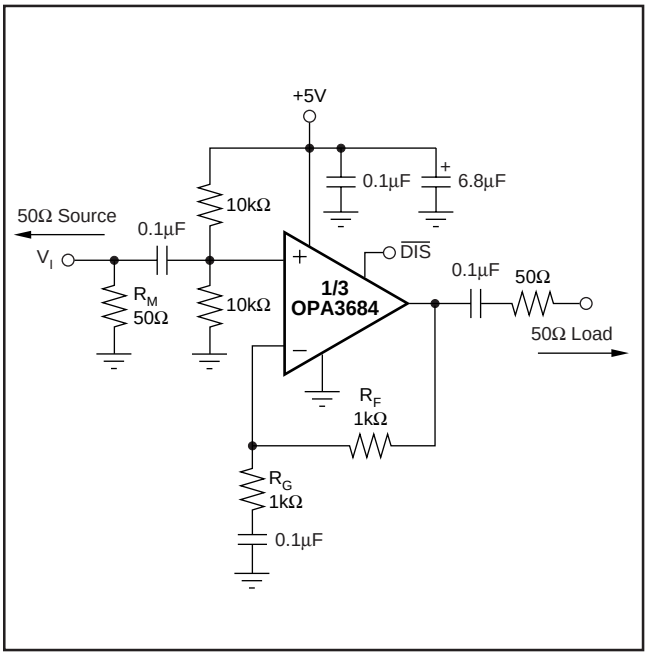


FIGURE 3. AC-Coupled, G = +2V/V, Single-Supply Specifications and Test Circuit.

Figure 4 shows the AC-coupled, single +5V supply, gain of –1V/V circuit configuration used as a basis for the inverting +5V only Typical Characteristics for each channel. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.1µF capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC-blocked by the input capacitor, will also appear at the output pin. One advantage to inverting operation is that since there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages is possible. To retain a 1Vp-p output capability, operation down to a 3V supply is allowed. At a +3V supply, the input stage is saturated, but for the inverting configuration of a current-feedback amplifier, wideband operation is retained even under this condition.

The circuits of Figure 3 and 4 show single-supply operation at +5V. These same circuits may be used up to single supplies of +12V with minimal change in the performance of the OPA3684.

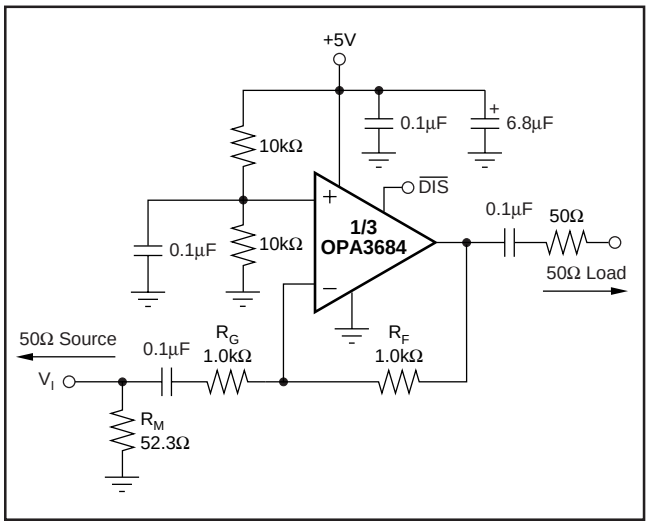


FIGURE 4. AC-Coupled, G = –1V/V, Single-Supply Specifications and Test Circuit.

LOW-POWER, VIDEO LINE DRIVER APPLICATIONS

For low-power, video line driving, the OPA3684 provides the output current and linearity to support 3 channels of either single video lines, or up to 4 video lines in parallel on each output. Figure 5 shows a typical ±5V supply video line driver application where only one channel is shown and only a single line is being driven. The improved 2nd-harmonic distortion of the CFB_{PLUS} architecture, along with the OPA3684's high output current and voltage, gives exceptional differential gain and phase performance for a low-power solution. As the Typical Characteristics show, a single video load shows a dG/dP of 0.04%/0.02°. Multiple loads may be driven on each output, with minimal x-talk, while the dG/dP is still < 0.1%/0.1° for up to 4 parallel video loads. The slew rate and gain of 2 bandwidth are also suitable to moderate resolution RGB applications.

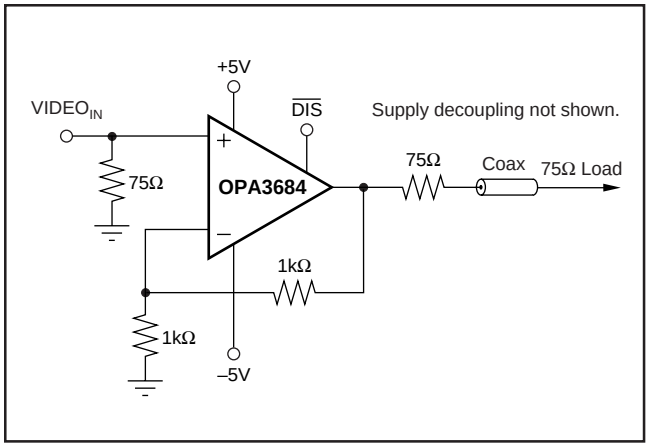


FIGURE 5. Noninverting Differential I/O Amplifier.

LOW-POWER RGB MUX/LINE DRIVER

Using the shutdown feature, two OPA3684s can provide an easy low-power way to select one of two possible RGB sources for moderate resolution monitors. Figure 6 shows a recommended circuit where each of the color outputs are combined in a way that provides a net gain of 1 to the matched 75Ω load with a 75Ω output impedance. This brings the two outputs for each color together through a 78.7Ω resistor with a slightly > 2 gain provided by the amplifiers.

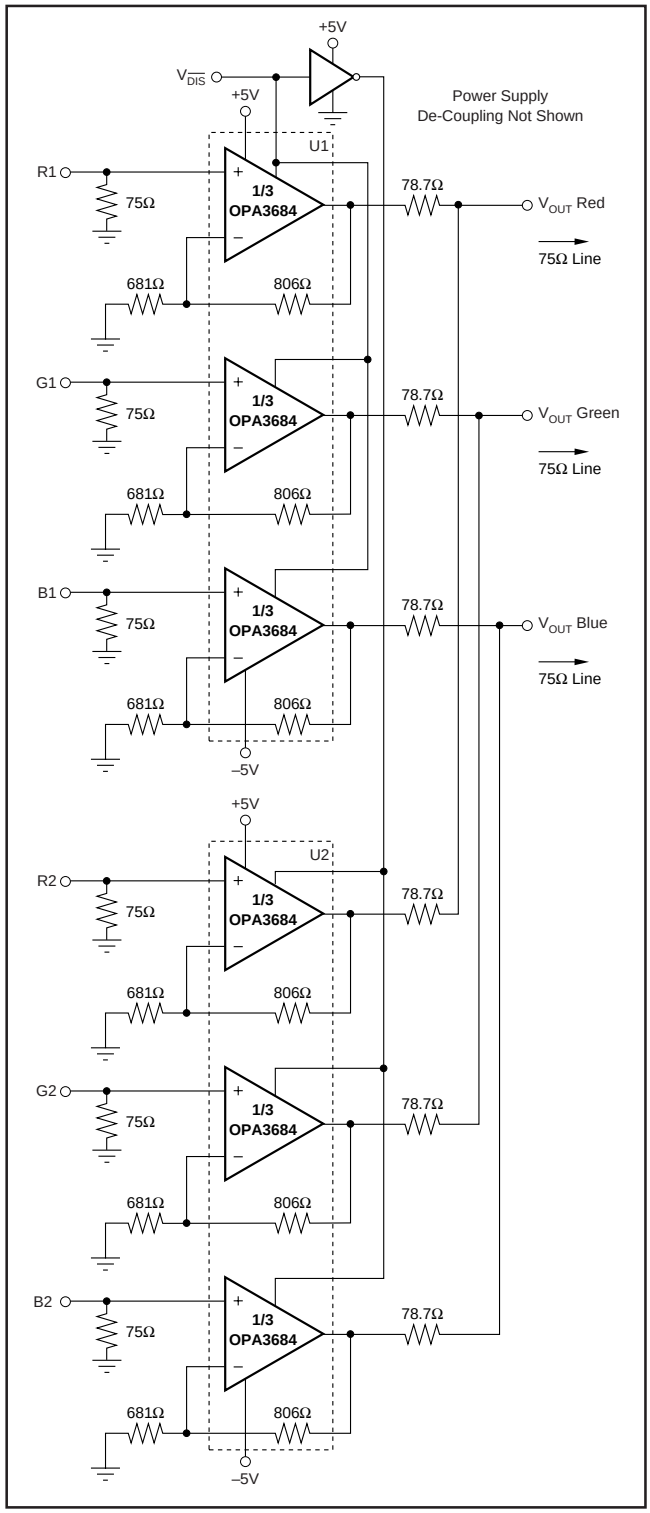


FIGURE 6. Wideband 2x1 RGB Multiplexer.

When one channel is shutdown, the feedback network is still present, slightly attenuating the signal and combining in parallel with the 78.7Ω to give a 75Ω source impedance.

Since the OPA3684 does not disable quickly, this approach is not suitable for pixel-by-pixel multiplexing—however, it does provide an easy way to switch between two possible RGB sources. The output swing provided by the active channel will divide back through the inactive channel feedback to appear at the inverting input of the OFF channel. To retain good pulse fidelity, or low distortion, this divided down output signal at the inverting inputs of the OFF channels, plus the OFF channel input signals, should not exceed 0.7Vp-p. As the signal across the buffers of the inactive channels exceeds 0.7Vp-p, diodes across the inputs begin to turn on causing a nonlinear load to the active channel. This will degrade signal purity under those conditions.

LOW-POWER, FLEXIBLE GAIN, DIFFERENTIAL RECEIVER

The 3 channels available in the OPA3684 can be applied to a very flexible differential to single-ended receiver. Since the bandwidth does not depend on the gain setting, the gain setting element of Figure 7 (R_G) can be adjusted over a wide range with minimal impact on resulting bandwidth. Frequency-response shaping elements may be included in R_G as well to provide line equalization or filtering in the final output signal.

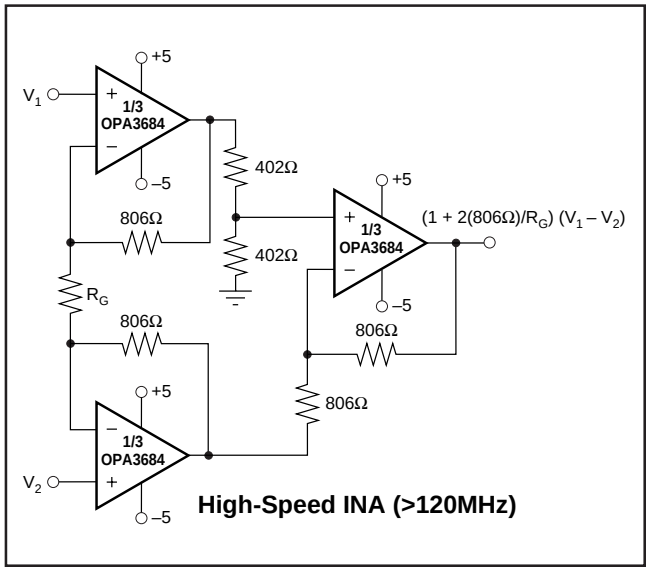


FIGURE 7. Low-Power, Wide Gain Range, Differential Receiver.

The first two amplifiers provide the differential gain function with a common-mode gain of 1. The second amplifier performs the differencing function to remove the common-mode (referencing the output to ground if the 402Ω resistor is grounded) and providing a differential gain of 1. The resistors have been scaled to provide the same output loading on each first stage amplifier. Typical bandwidths for the circuit of Figure 7 exceed 120MHz.

WIDEBAND PGA FOR ADC DRIVING

Using the 3 channels of the OPA3684, and the shutdown feature, can give an easy to use PGA function—which can be applied to driving an ADC. Since the bandwidth does not vary with gain for the CFB_{PLUS} OPA3684, each channel can be set up to a desired gain setting, with each of the noninverting inputs driven with the same input signal. Selecting one of the 3 channels passes on the input with the gain setting provided by the selected channel. Figure 8 shows an example where the channels are set to gains of 2, 5, and 10. Again, the output signal will be divided down back to the inverting inputs of the inactive channels. To retain good pulse fidelity, or low distortion, this divided down output signal at the inverting inputs of the OFF channels, plus the OFF channel input signals, should not exceed 0.7Vp-p. As the signal across the buffers of the inactive channels exceeds 0.7Vp-p, diodes across the inputs begin to turn on causing a nonlinear load to the active channel. This will degrade signal fidelity under those conditions.

VIDEO DAC RECONSTRUCTION FILTER

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. The triple channel OPA3684 can be used as a very effective video Digital-to-Analog Converter (DAC) reconstruction filter and line driver. Figure 9 shows an example of this where the delay-equalized filter compensates for the DAC's sin(x)/x response, and minimizes aliasing artifacts. It is shown here as a single +5V design expecting a 13.5MSPS DAC sampling rate, and giving a 5.5MHz cutoff frequency.

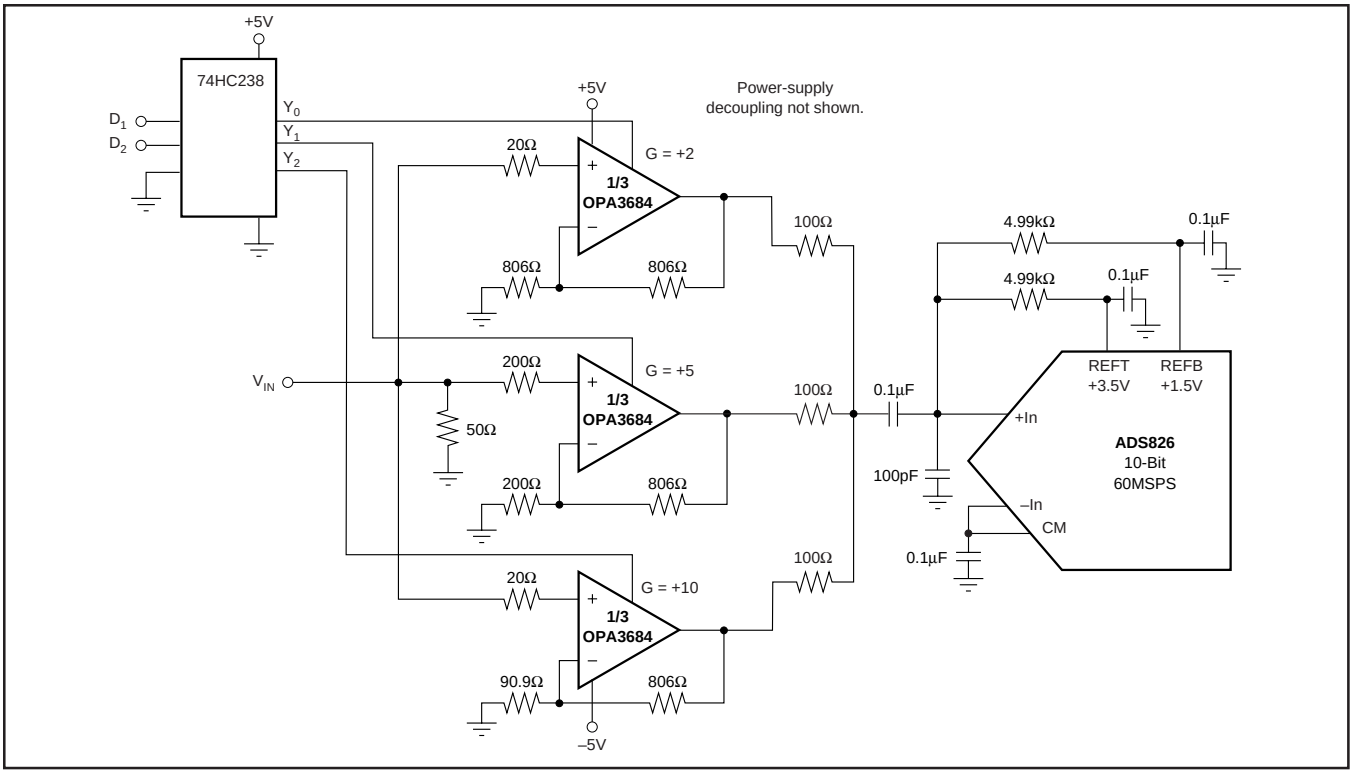


FIGURE 8. Wideband PGA for ADC Driving.

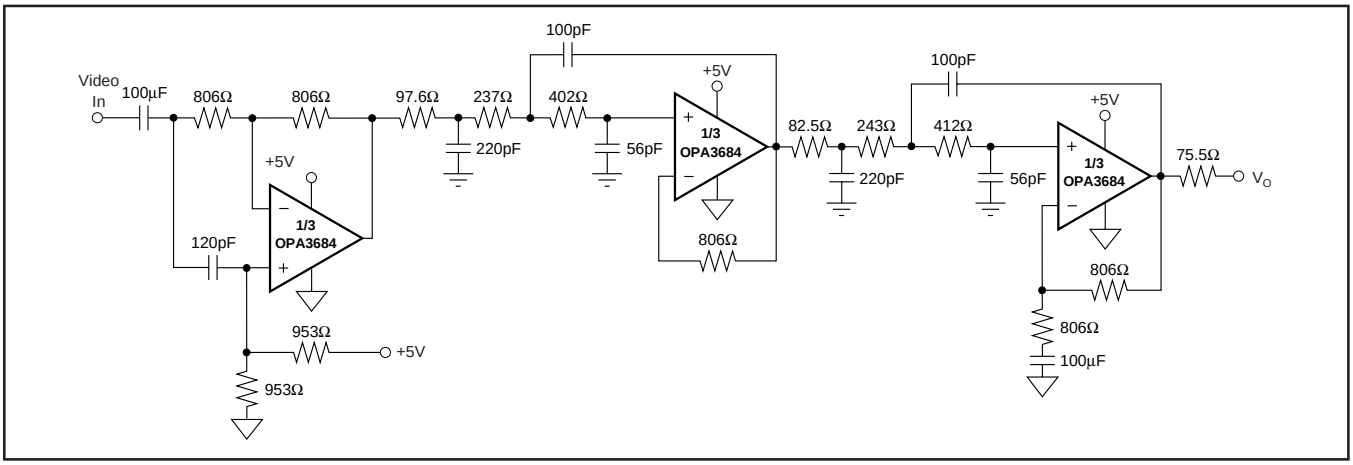


FIGURE 9. Composite Video Filter.

The first stage buffers the video DAC output to the first 3rd-order filter section. This stage also provides group delay equalization while the 2nd and 3rd stages each give a 3rd-order low-pass response with sin(x)/x equalization. Figure 10 shows the frequency response for the filter of Figure 9.

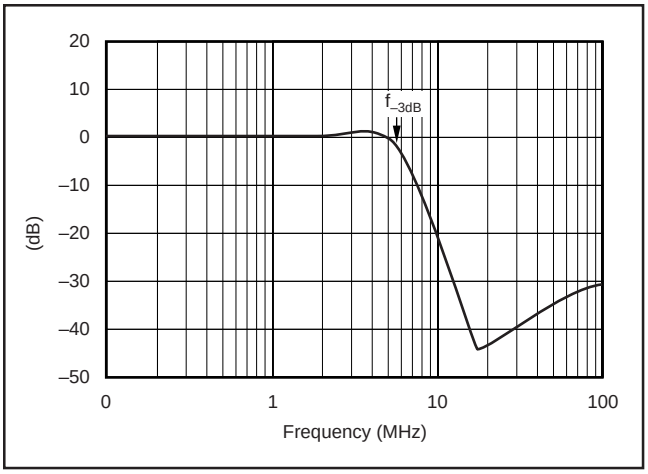


FIGURE 10. Video Filter Frequency Response.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA3684 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3684ID	SO-14	DEM-OPA-SO-3B	SBOU018
OPA3684IDBQ	SSOP-16	DEM-OPA-SSOP-3B	SBOU019

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA3684 product folder.

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful in predicting the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. Check the TI web site (www.ti.com) for SPICE macromodels within the OPA3684 product folder. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting distortion or dG/dP characteristics. Most of these models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

Any current-feedback op amp like the OPA3684 can hold high bandwidth over signal-gain settings with the proper adjustment of the external resistor values. A low-power part like the OPA3684 typically shows a larger change in bandwidth due to the significant contribution of the inverting input impedance to loop-gain changes as the signal gain is changed. Figure 11 shows a simplified analysis circuit for any current-feedback amplifier.

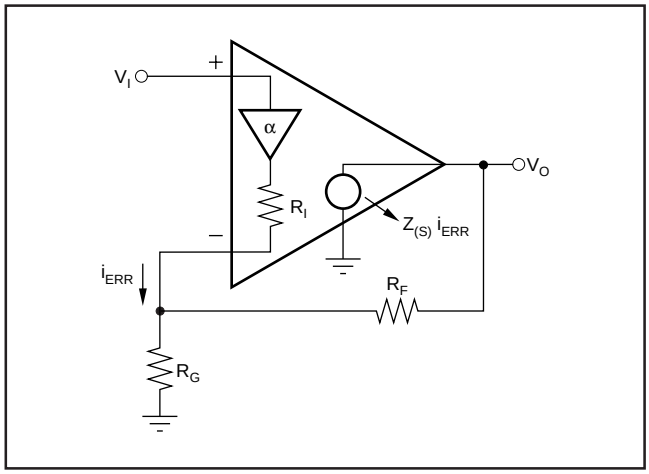


FIGURE 11. Current-Feedback Transfer Function Analysis Circuit.

The key elements of this current-feedback op amp model are:

$\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \Rightarrow$ Buffer output impedance

$i_{ERR} \Rightarrow$ Feedback error current signal

$Z_{(S)} \Rightarrow$ Frequency-dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$ and $CMRR = -20 \cdot \log(1 - \alpha)$. The closed-loop input stage buffer used in the OPA3684 gives a buffer gain more closely approaching 1.00 and this shows up in a slightly higher CMRR than previous current-feedback op amps.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA3684 reduces this element to approximately 4.0Ω using the local loop gain of the input buffer stage. This significant reduction in output impedance, on very low power, contributes significantly to extending the bandwidth at higher gains.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent

transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 14 gives Equation 1:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F + R_I\, NG}{Z_{(S)}}} \quad (1)$$

$$\left[NG = \left(1+\frac{R_F}{R_G}\right)\right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation.

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain} \quad (2)$$

If $20 \bullet \log(R_F + NG \bullet R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA3684 is internally compensated to give a maximally flat frequency response for R_F = 800Ω at NG = 2 on ±5V supplies. That optimum value goes to 1.0kΩ on a single +5V supply. Normally, with a current-feedback amplifier, it is possible to adjust the feedback resistor to hold this bandwidth up as the gain is increased. The CFB_{PLUS} architecture has reduced the contribution of the inverting input impedance to provide exceptional bandwidth to higher gains without adjusting the feedback resistor value. The Typical Characteristics show the small-signal bandwidth over gain with a fixed feedback resistor.

Putting a closed-loop buffer between the noninverting and inverting inputs does bring some added considerations. Since the voltage at the inverting output node is now the output of a locally closed-loop buffer, parasitic external capacitance on this node can cause frequency response peaking for the transfer function from the noninverting input voltage to the inverting node voltage. While it is always important to keep the inverting node capacitance low for any current-feedback op amp, it is critically important for the OPA3684. External layout capacitance in excess of 2pF will start to peak the frequency response. This peaking can be easily reduced by increasing the feedback resistor value—but it is preferable, from a noise and dynamic range standpoint, to keep that capacitance low, allowing a close to nominal 800Ω feedback resistor for flat frequency response. Very high parasitic capacitance values on the inverting node (> 5pF) can possibly cause input stage oscillation that cannot be filtered by a feedback element adjustment.

At very high gains, 2nd-order effects in the inverting output impedance cause the overall response to peak up. If desired, it is possible to retain a flat frequency response at higher gains by adjusting the feedback resistor to higher values as the gain is increased. Since the exact value of feedback that will give a flat frequency response depends strongly in inverting and output node parasitic capacitance values, it is best to experiment in the specific board with increasing values until the desired flatness (or pulse response shape) is obtained. In general, increasing R_F (and adjusting R_G to the desired gain) will move towards flattening the response, while decreasing it will extend the bandwidth at the cost of some peaking.

OUTPUT CURRENT AND VOLTAGE

The OPA3684 provides output voltage and current capabilities that can support the needs of driving doubly-terminated 50Ω lines. For a 100Ω load at the gain of +2 (see Figure 1), the total load is the parallel combination of the 100Ω load and the 1.6kΩ total feedback network impedance. This 94Ω load will require no more than 40mA output current to support the ±3.8V minimum output voltage swing specified for 100Ω loads. This is well under the specified minimum +110mA/–90mA output current specifications over the full temperature range.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* curve in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3684's output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}'s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the

available output voltage and current will always be greater than that shown in the over temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series-matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to a power-supply pin will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small-series resistor in the power-supply leads. This will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short-circuit while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. This slight drop in available swing is more if multiple channels are driving heavy loads simultaneously. Always place the 0.1μF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins. An alternative approach is to place the 5Ω inside the loop at each output of the amplifiers. This will provide some short-circuit protection, but hurts the phase margin under capacitive load conditions.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common load conditions, for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA3684 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S *vs* C_{LOAD} and the resulting frequency response at the load. The 1kΩ resistor shown in parallel with the load capacitor is a measurement path and may be omitted. Parasitic capacitive loads greater than 5pF can begin to degrade the performance of the OPA3684. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3684 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA3684 provides very low distortion in a low-power part. The CFB_{PLUS} architecture also gives two significant areas of distortion improvement. First, in operating regions where the 2nd-harmonic distortion due to output stage nonlinearities is very low (frequencies < 1MHz, low output swings into light loads) the linearization at the inverting node provided by the CFB_{PLUS} design gives 2nd-harmonic distortions that extend into the –90dBc region. Previous current-feedback amplifiers have been limited to approximately –85dBc due to the nonlinearities at the inverting input. The second area of distortion improvement comes in a distortion performance that is largely gain independent. To the extent that the distortion at a particular output power is output-stage dependent, 3rd-harmonics particularly (and to a lesser extend 2nd-harmonic distortion) are constant as the gain is increased. This is due to the constant loop-gain versus signal gain provided by the CFB_{PLUS} design. As shown in the Typical Characteristic curves, while the 3rd-harmonic is constant with gain, the 2nd-harmonic degrades at higher gains. This is largely due to board parasitic issues. Slightly imbalanced load return currents through the ground plane will couple into the gain resistor to cause a portion of the 2nd-harmonic distortion. At high gains, this imbalance has more gain to the output giving reduced 2nd-harmonic distortion. Differential stages using two of the channels together can reduce this 2nd-harmonic issue enormously by getting back to an essentially gain independent distortion.

Relative to alternative amplifiers with < 2mA/ch supply current, the OPA3684 holds much lower distortion at higher frequencies (> 5MHz) and to higher gains. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a lower 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. A low-power part like the OPA3684 includes quiescent boost circuits to provide the large-signal bandwidth in the Electrical Characteristics. These act to increase the bias in a very linear fashion only when high slew rate or output power is required. This also acts to actually reduce the distortion slightly at higher output power levels. The Typical Characteristic curves show the 2nd-harmonic holding constant from 500mVp-p to 5Vp-p outputs while the 3rd-harmonics actually decrease with increasing output power.

The OPA3684 has an extremely low 3rd-order harmonic distortion, particularly for light loads and at lower frequencies. This also gives low 2-tone, 3rd-order intermodulation distortion as shown in the Typical Characteristic curves. Since the OPA3684 includes internal power boost circuits to retain good full-power performance at high frequencies and outputs, it does not show a classical 2-tone, 3rd-order intermodulation intercept characteristic. Instead, it holds relatively low and constant 3rd-order intermodulation spurious levels over power. The Typical Characteristic curves show this spurious level as a dBc below the carrier at fixed center frequencies swept over single-tone power at a matched 50Ω load. These spurious levels drop significantly (> 12dB) for lighter loads than the 100Ω used in the *2-Tone, 3rd-Order Intermodulation Distortion* curve. Converter inputs for instance will see < –82dBc 3rd-order spurious to 10MHz for full-scale inputs. For even lower 3rd-order intermodulation distortion to much higher frequencies, consider the OPA3691 triple or OPA691 and OPA685 single-channel current-feedback amplifiers.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA3684 offers an excellent balance between voltage and current noise terms to achieve low output noise in a low-power amplifier. The inverting current noise (17pA/$\sqrt{Hz}$) is comparable to most other current-feedback op amps while the input voltage noise (3.7nV/$\sqrt{Hz}$) is lower than any unity-gain stable, comparable slew rate, voltage-feedback op amp. This low input voltage noise was achieved at the price of higher noninverting input current noise (9.4pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 200Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

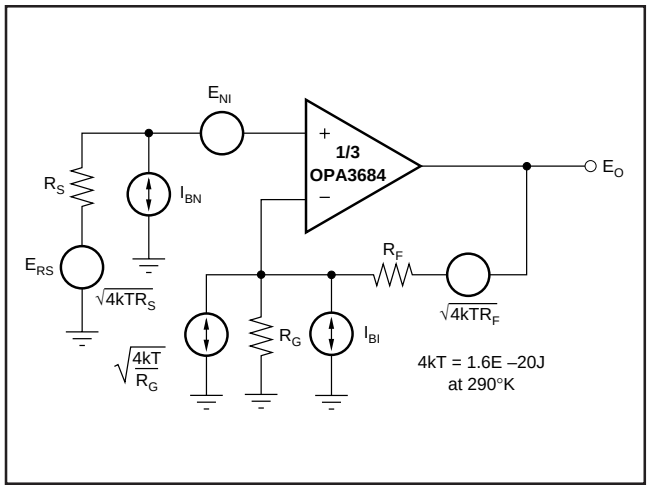


FIGURE 12. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms presented in Figure 12.

(3)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 4.

(4)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA3684 circuit and component values presented in Figure 1 will give a total output spot noise voltage of 16.3nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 8.1nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 3.7nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. As the gain is increased, this fixed output noise power term contributes less to the total output noise and the total input referred voltage noise given by Equation 3 will approach just the 3.7nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 in the circuit of Figure 1, adjusting only the gain resistor to 42.1Ω, will give a total input referred noise of 3.9nV/$\sqrt{Hz}$. A more complete description of op amp noise analysis can be found in the Texas Instruments application note, AB-103, *Noise Analysis for High-Speed Op Amps* (SBOA066), located at www.ti.com.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA3684 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Specifications show an input offset voltage comparable to high slew rate voltage-feedback amplifiers. The two input bias currents, however, are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \bullet V_{OS(MAX)}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$

where NG = noninverting signal gain

$= \pm(2 \bullet 3.9mV) \pm (12\mu A \bullet 25\Omega \bullet 2) \pm (800\Omega \bullet 17\mu A)$

$= \pm 7.8mV + 0.6mV \pm 13.6mV$

$= \pm 22mV$

While the last term, the inverting bias current error, is dominant in this low-gain circuit, the input offset voltage will become the dominant DC error term as the gain exceeds 5V/V. Where improved DC precision is required in a high-speed amplifier, consider the OPA656 unity gain stable and OPA657 high-gain bandwidth JFET input op amps.

DISABLE OPERATION

The OPA3684 provides an optional disable feature on each channel that may be used to reduce system power when channel operation is not required. If the $V_{\overline{DIS}}$ control pin is left unconnected, each channel of the OPA3684 will operate normally. To disable, the control pin must be asserted low. Figure 13 shows a simplified internal circuit for the disable control feature.

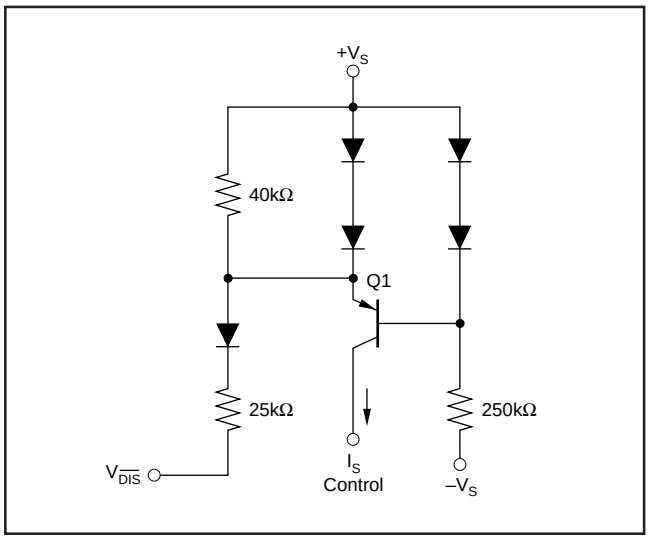


FIGURE 13. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 250kΩ resistor while the emitter current through the 40kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 40kΩ resistor eventually turning on these two diodes (≈ 30μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 13.

When disabled, the output and input nodes go to a high impedance state. If the OPA3684 is operating in a gain of +1 (with a 800Ω feedback resistor still required for stability), this will show a very high impedance (1.7pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

Each channel of the OPA3684 provides very high power gain on low quiescent current levels. When disabled, internal high impedance nodes discharge slowly which, with the exceptional power gain provided, give a self powering characteristic that leads to a slow turn off characteristic. Typical full turn-off times to rated 100μA disabled supply current are 4ms. Turn-on times are very fast—less than 40ns.

The circuit of Figure 13 will control the disable feature using standard 5V CMOS or TTL level signals when the OPA3684 is operated on ±5V or single +5V supplies. Since this circuit is really a current mode control, disable operation for a single +12V supply should be implemented using an open collector logic family.

THERMAL ANALYSIS

The OPA3684 will not require external heatsinking for most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA3684IDBQ (SSOP-16 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with all channels driving a grounded 100Ω load.

$P_D = 10V \bullet 5.6mA + 3 \bullet (5^2 / (4 \bullet (100\Omega \,||\, 1.6k\Omega))) = 255mW$
Maximum $T_J = +85°C + (0.255W \bullet 100°C/W) = 111°C$.

This maximum operating junction temperature is well below most system level targets. Most applications will be lower than this since an absolute worst-case output stage power was assumed in this calculation with all 3 channels running maximum output power simultaneously.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA3684 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.01µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) **Careful selection and placement of external components will preserve the high-frequency performance of the OPA3684.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. The quad amplifier pinout allows each output and inverting input to be connected by the feedback element with virtually no trace length. Other network components, such as noninverting input termination resistors, should also be placed close to the package. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the peaking at higher gains, while decreasing it will give a more peaked frequency response at lower gains. The 800Ω feedback resistor used in the Typical Characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 800Ω feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S *vs* C_{LOAD}. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA3684 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion, see the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3684 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA3684 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S *vs* C_{LOAD}. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is LOW, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high-speed part like the OPA3684 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3684 onto the board.

INPUT AND ESD PROTECTION

The OPA3684 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum 13V across the supply pins is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 14.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3684), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

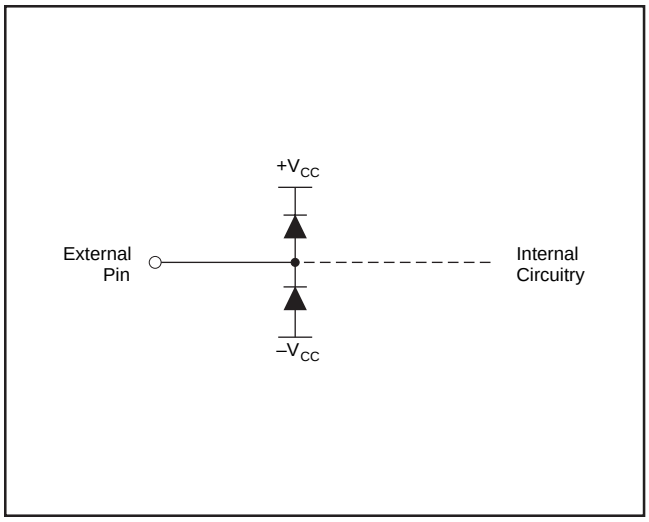


FIGURE 14. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/08	C	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.
		3, 4	Electrical Characteristics, Power Supply	Added minimum supply voltage.
6/06	B	16	Design-In Tools	Demonstration fixture numbers changed.
		23	Applications Information	Added Revision History table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3684ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3684	Samples
OPA3684IDBQT	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 3684	Samples
OPA3684IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3684	Samples
OPA3684IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3684	Samples
OPA3684IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3684	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

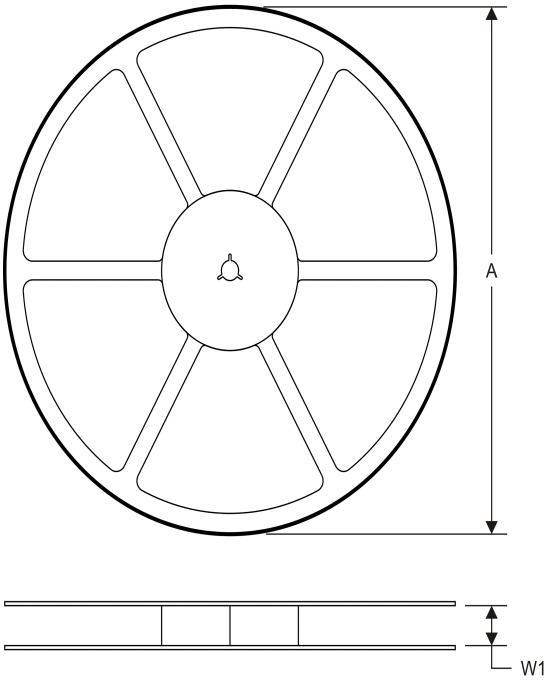
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

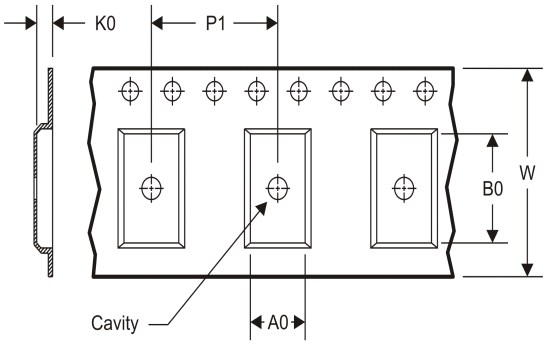
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



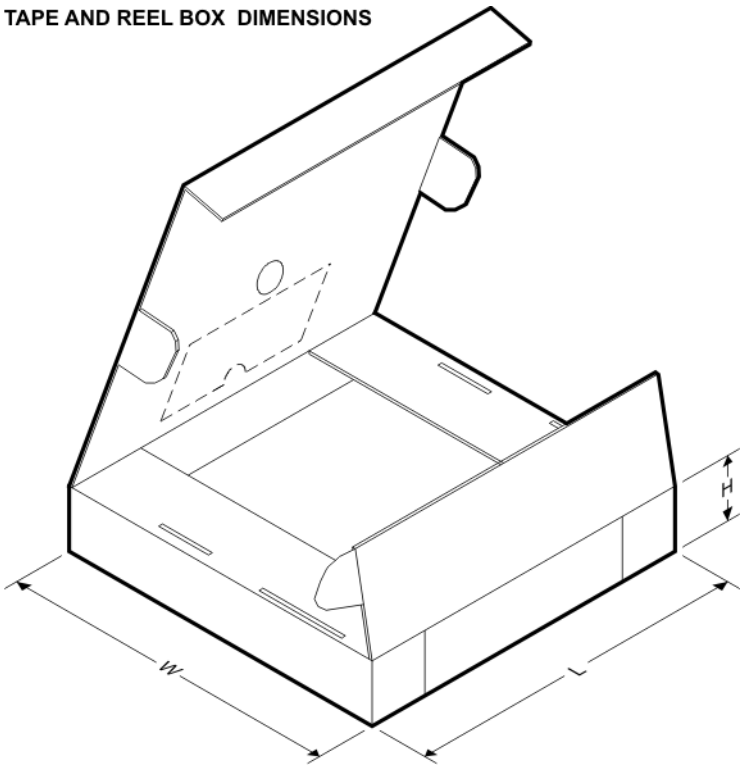
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3684IDBQT	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA3684IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

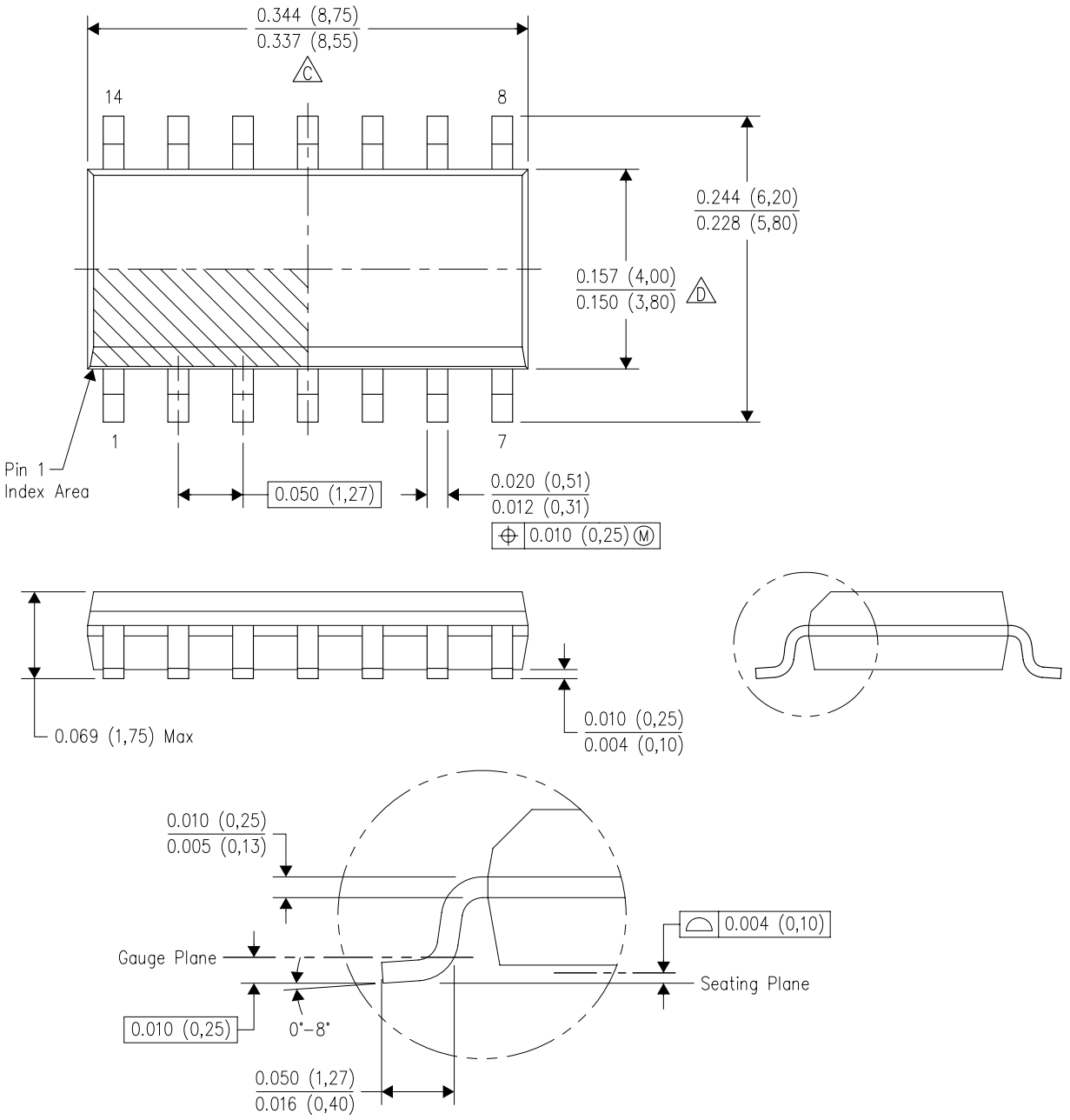
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3684IDBQT	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA3684IDR	SOIC	D	14	2500	367.0	367.0	38.0

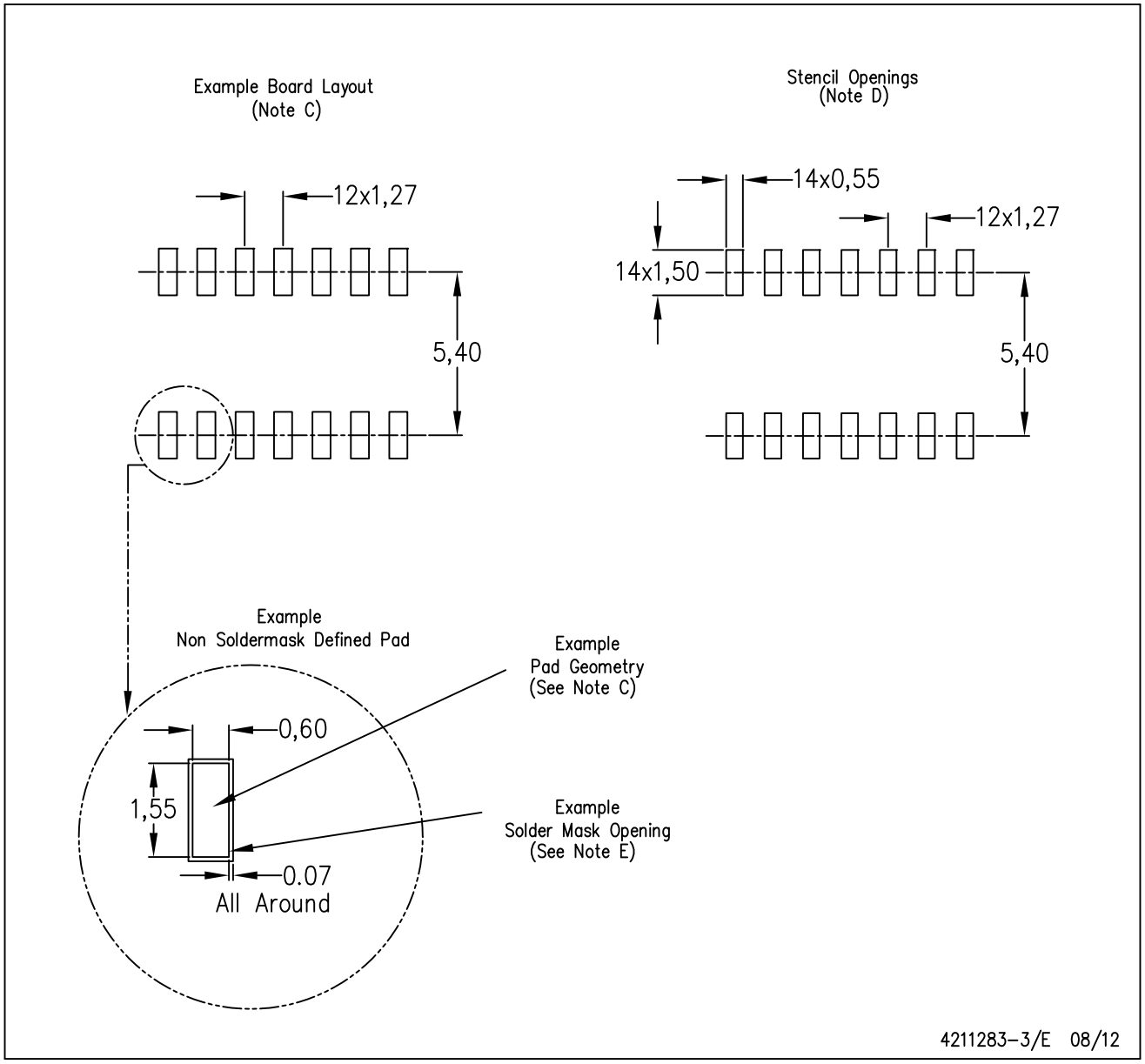
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

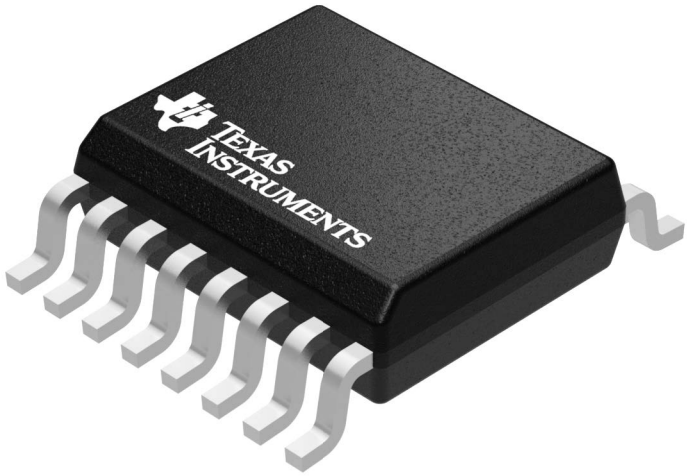


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

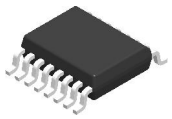
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

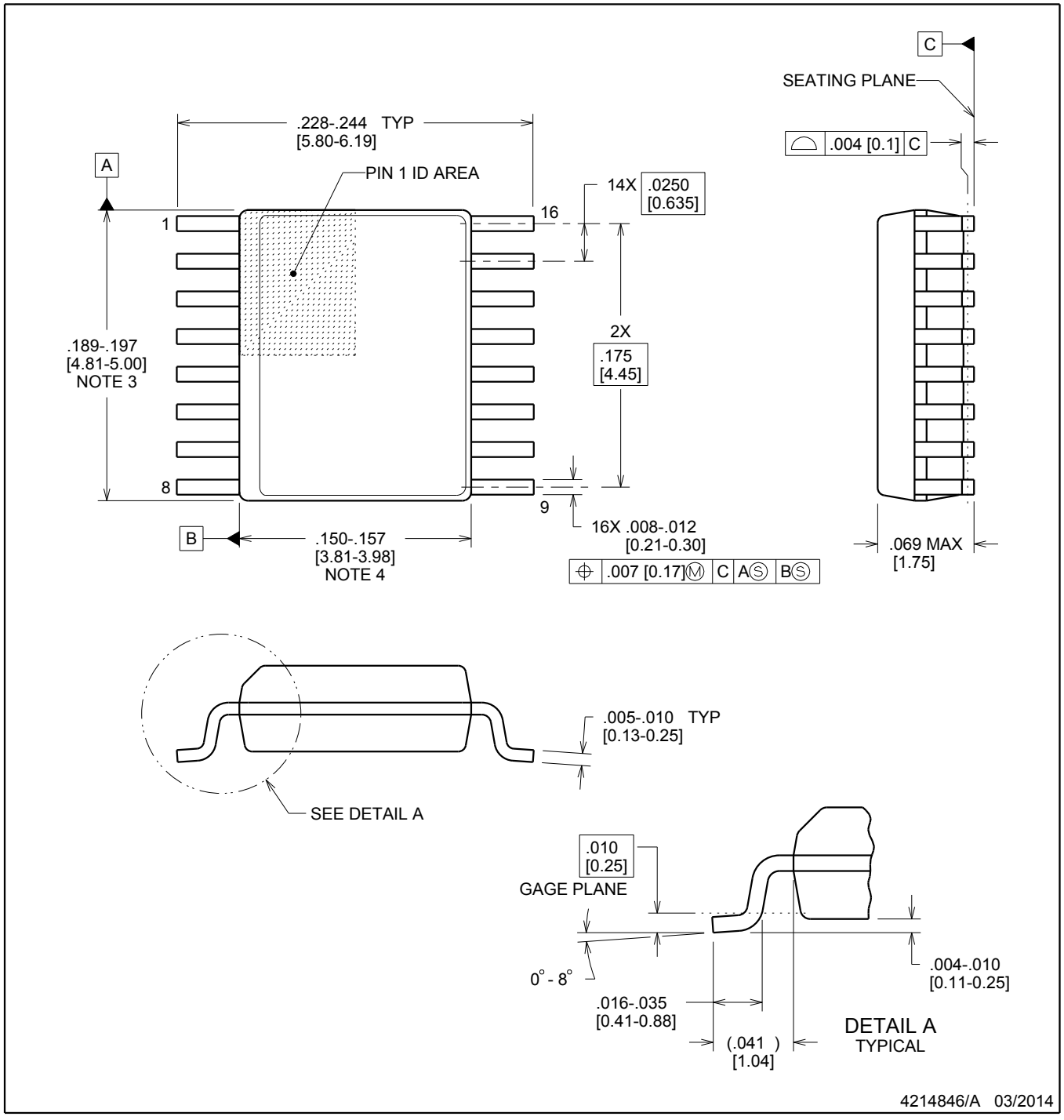


PACKAGE OUTLINE

DBQ0016A

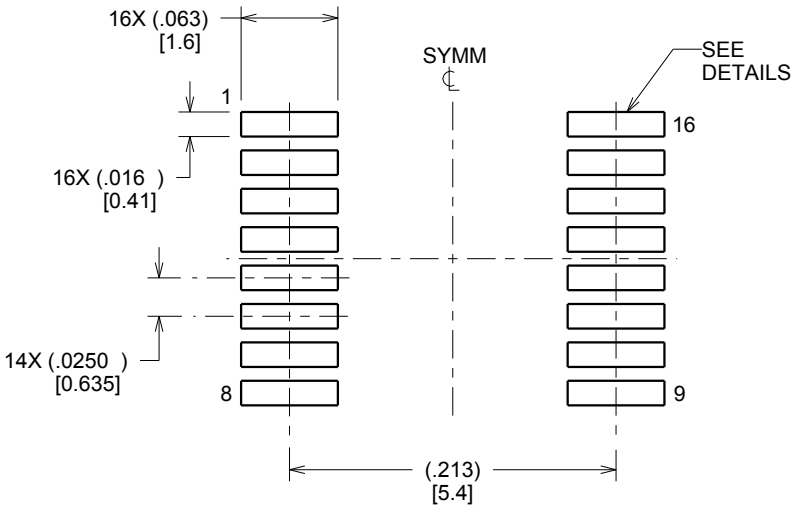
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

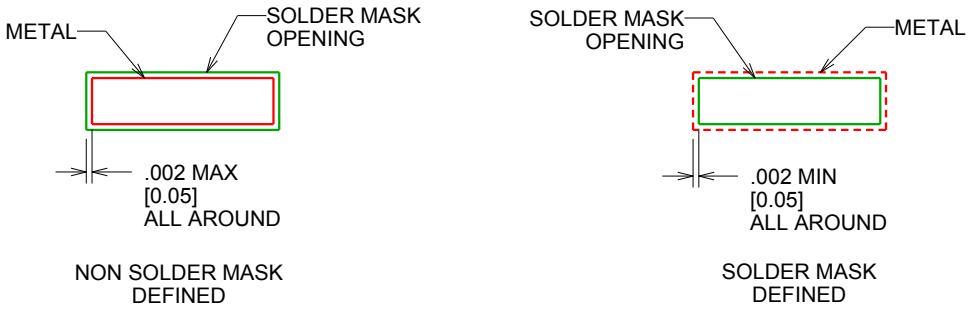


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

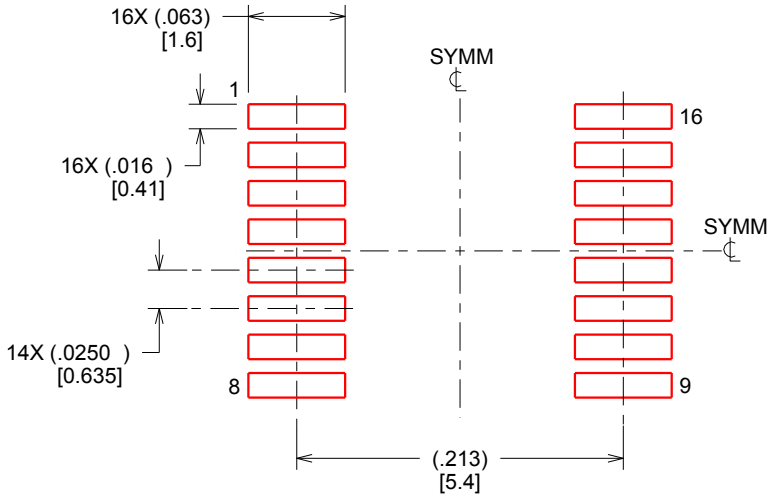
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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